Online Homework System

Assignment Worksheet
1/9/23 - 1:34:57 PM MST

Name: _____ **Class:**

Class #: _____ **Section #:** _____

Instructor: Ross Taylor **Assignment:** Introduction to Diodes and the P-N Junction

Question 1: (1 point)

Active Components vs. Passive Components

In a previous course, you worked with a group of electrical components that we refer to as **Passive Components** -- components that behave according to simple mathematical relationships in response to changes in the rest of the circuitry. For example, unless you push it beyond its limits, a resistor will always behave very nearly as predicted by

V=IR

A capacitor will always respond very nearly as predicted by

$$i_C = C\frac{\mathrm{d}V}{\mathrm{d}t}$$

An inductor will always respond very nearly as predicted by

$$v_L = L\frac{\mathrm{d}I}{\mathrm{d}t}$$

Both the capacitor and inductor, as predicted by their basic formulas, will generate exponential charging functions when placed in series with a resistor and powered by a fixed voltage source.

By the way, the "very nearly" caveats in the preceding description is an important indication that, by developing these formulas, we are creating simplified mathematical models of real devices. Real devices do other things that we don't include in our models. For example, the resistance of a resistor changes with temperature, and temperature changes with current, something Ohm's Law by itself doesn't account for. Capacitors usually have a small leakage current which means the total current for charging a capacitor will be slightly greater than what is predicted by the model. Inductors are plagued by residual magnetism which means they don't respond instantaneously to changes in the circuit as predicted by our mathematical model. However, the formulas we use to model the activity of these passive components is usually good enough for the work we're doing.

Active Components, on the other hand, behave differently for different conditions in a circuit. The diode is the simplest of the active components. Carry out the following investigation to see how it responds differently to different circuit conditions.

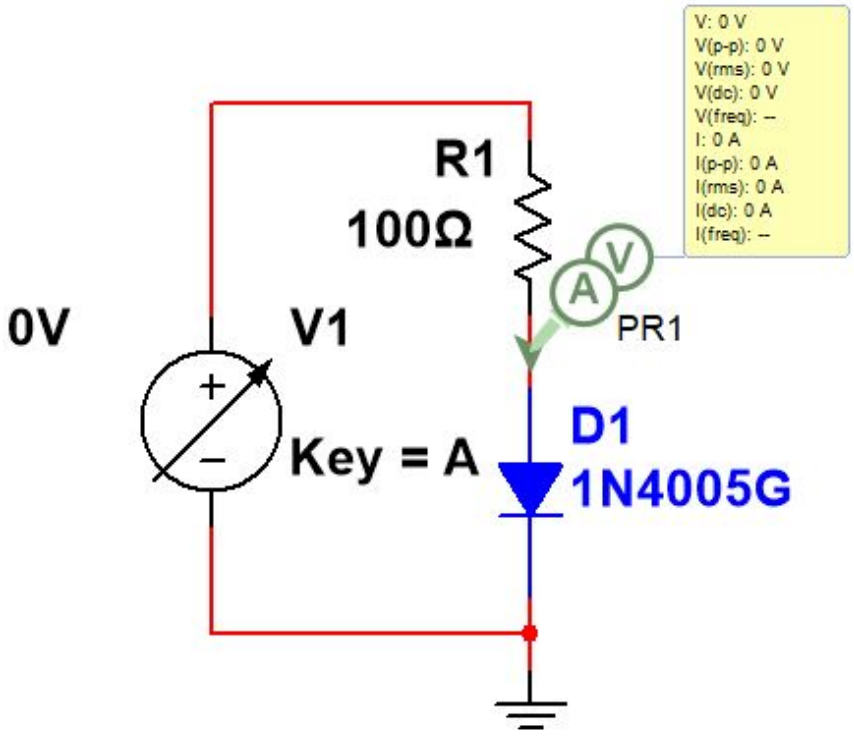
Using Multisim, build the following simple circuit. The diode is found under "Diodes -> DIODE->1N4005G". Make sure it's pointing the right way.

The variable DC source is found under "Sources->SIGNAL_VOLTAGE_SOURCES->DC_INTERACTIVE_VOLTAGE".

Change the settings of the DC voltage source. It should be set to

- Maximum value: 5.0 V
- Minimum value: -5.0 V
- Increment: 0.5%

As shown, place a voltage and current probe, pointing downwards, between the resistor and the diode.



Set the DC voltage to each of the values in the following table, and record the corresponding diode current and voltage. Subtract the diode voltage from the DC supply to get the resistor voltage, or, alternatively, put a differential voltage probe across the resistor. For consistency clarity, and proper grading, record your values in the units indicated at the tops of each of the columns. If the numbers shown are in the micro or nano ranges, record them as zero to simplify analysis.

V_{Supply}, V_{DC}	V_{Diode}, V	I, mA	V_{R1}, V
0.00	_____	_____	_____
0.35	_____	_____	_____
3.00	_____	_____	_____
5.00	_____	_____	_____
-3.00	_____	_____	_____
-5.00	_____	_____	_____

Answer the following questions using this table of data.

The diode responds the same way to positive and negative voltages.

(a) True
(b) False

The supply voltage must be greater than 0.7 V, and in the correct orientation, before current will flow.

(a) True
(b) False

When current is flowing, the diode voltage, rounded to one digit after the decimal place, is approximately _____ V

When current is flowing, the current is controlled by (i.e. directly related to)

(a) the diode voltage

(b) the resistor voltage

(c) the source voltage

When current is not flowing, the diode voltage is equal to

(a) zero

(b) the source voltage

(c) the resistor voltage

When current is not flowing, the resistor voltage is equal to

(a) zero

(b) the source voltage

(c) the diode voltage

You should be able to verify your answer to the last question using Ohm's Law, written here specifically for the resistor:

$$\Delta V_R = I_R R$$

One very significant thing you should note is that the voltage across the resistor tells you instantly whether there is current flowing or not.

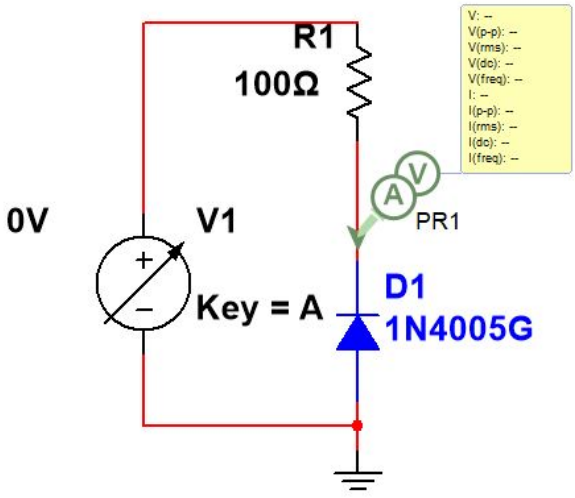
- If the voltage across the resistor is zero, the current in the circuit is zero
- If the voltage across the resistor is not zero, current is flowing in the circuit.

Whenever you approach a circuit, keep this simple application of Ohm's Law in mind, and you will have a very useful analytic and troubleshooting tool at your disposal.

What you have seen in the exercise you've completed is that the diode, as an Active Component, responds differently to a positive (forward biasing) voltage than it does to a negative (reverse biasing) voltage. It also responds differently to a small forward-biasing voltage than it does to a large forward-biasing voltage. Clearly, this behaviour is considerably different from what you have seen in Passive Components in the past.

Biasing

In the previous paragraph, you were introduced to two new terms: **Forward Biasing** and **Reverse Biasing.** In the exercise we just completed, these terms directly correlated to Positive and Negative voltages. However, the correlation is only due to the orientation of the diode in the circuit. **Biasing** simply refers to the external circuitry that sets up the electrical conditions of a circuit element. For a diode, it usually involves a DC power supply and resistors. Modify your circuit so that the diode is the other way around, as shown in the following schematic:



Adjust the input supply to the voltages in the following table, and record the diode voltage, the current, and the resistor voltage for each. You'll notice that, if the current flows in the opposite direction to the probe orientation, it will be negative. Also, if the positive indicator of a potential difference (voltage) is below the negative indicator, the voltage is negative. (For single point probes, the reference is ground, or zero.)

V_{Supply}, V_{DC}	V_{Diode}, V	I, mA	V_{R1}, V
0.00	_____	_____	_____
3.00	_____	_____	_____
5.00	_____	_____	_____

-0.35	_____	_____	_____
-3.00	_____	_____	_____
-5.00	_____	_____	_____

When the magnitude of the voltage is greater than 0.7 V and its polarity is suitable, current will flow in the direction indicated by the "arrow" in the diode symbol.

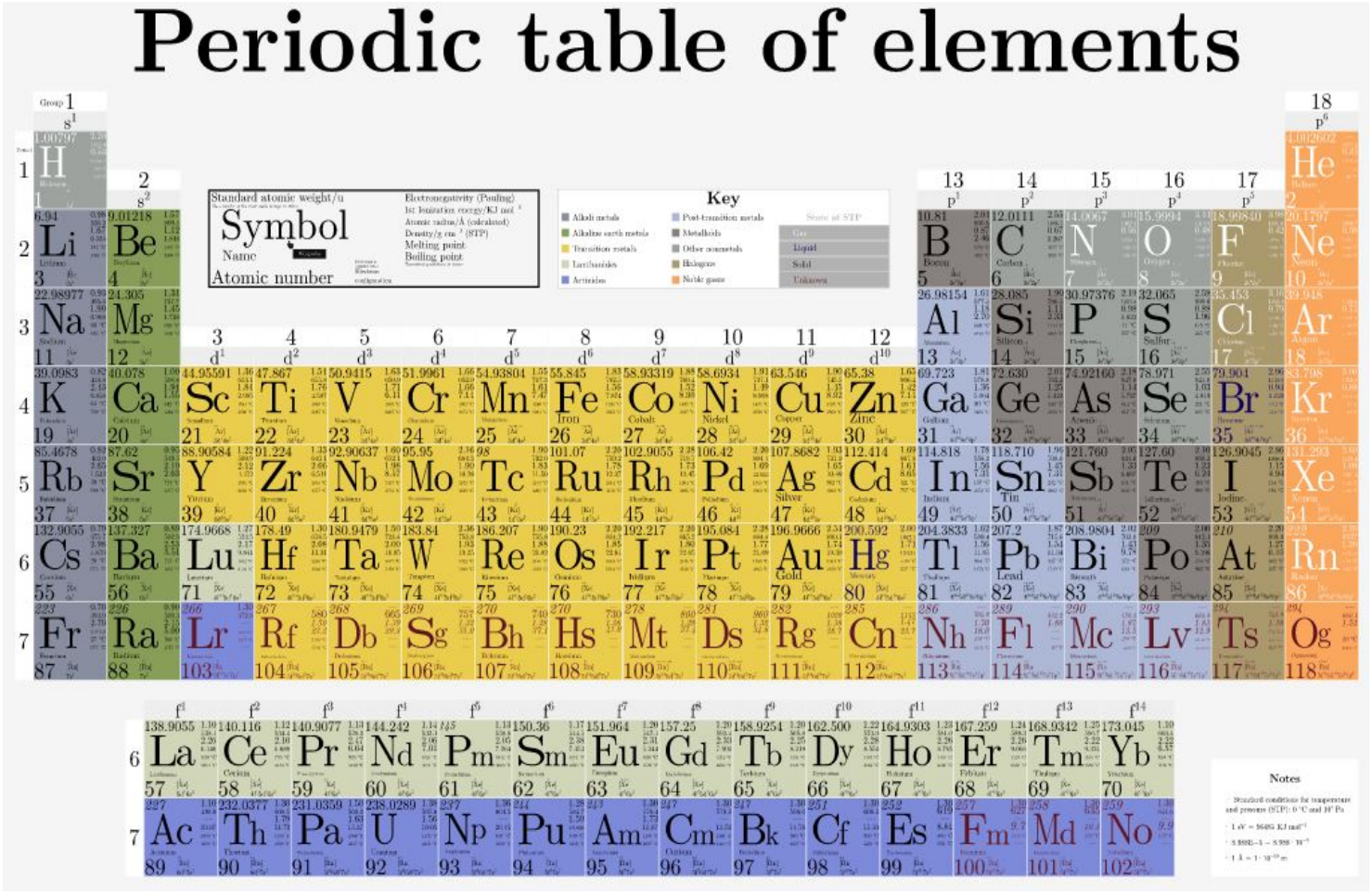
(a) True
(b) False

Now that you have investigated the functional behaviour of the diode, you will learn why the diode behaves as it does, and will learn how to use appropriate models to predict diode behaviour in any electronic circuit.

Question 2: (1 point)

Insulators, Conductors, and Semiconductors

On a Periodic Table of the Elements, materials fall into three general categories. Most of the left and central part of the periodic table consists of metals, which conduct electricity and react with non-metals to form Ionic Bonds. On the right side are the non-metals, which do not readily conduct electricity. Most of these react to form Ionic Bonds with metals, but also form Covalent Bonds with other non-metals. There is one family of non-metals which almost never enter into any chemical reactions -- the Ideal (or Noble) Gases.



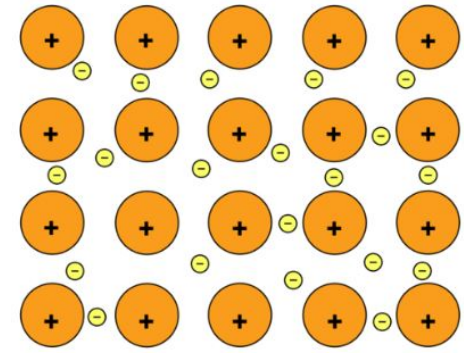
"File:Periodic table CSCJ.svg" (https://commons.wikimedia.org/w/index.php?curid=79660841) by Dolgoruki.es (https://commons.wikimedia.org/w/index.php?title=User:Dolgoruki.es&action=edit&redlink=1) is licensed under CC BY-SA 4.0 (https://creativecommons.org/licenses/by-sa/4.0?ref=ccsearch&atype=rich)

The nature of each element is largely determined by the outermost electrons as they position themselves around the nucleus. These outermost electrons are called the Valence Electrons, and for most elements, there are eight possible locations for valence electrons in what is called the Valence Shell. The remainder of the electrons, combined with the nucleus, form the core of the atom.

Metals typically have fewer than four valence electrons in their Valence Shell. If they have one valence electron, the core charge will be +1; two valence electrons means a core charge of +2; three valence electrons means a core charge of +3.

Non-metals typically have more than four valence electrons in their Valence Shell. If they have seven valence electrons, the core charge will be +7; six valence electrons means a core charge of +6; five valence electrons means a core charge of +5.

Metals, with their small core charges, have a weak attraction for their valence electrons, and so those electrons are relatively free to move as an electrical current when a voltage is applied across the material. In fact, these electrons are officially referred to as "Free Electrons".



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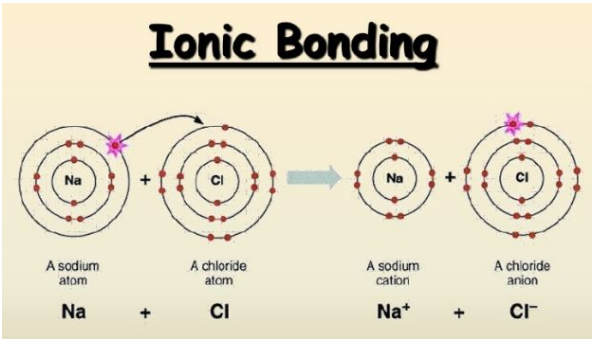
Also, these loosely-attracted valence electrons can be stripped away, leaving a positive ion which will be attracted to negative ions in an Ionic Bond. Ionic bonded compounds are typically non-conductive, because what used to be a free electron in the metal has now been bound to the non-metal atom. The strong attractions between the positive ions and negative ions often result in regularly-defined crystal structures. However, when dissolved in water, the ions become detached from each other, and can move as charged particles in the water, making the solution conductive.



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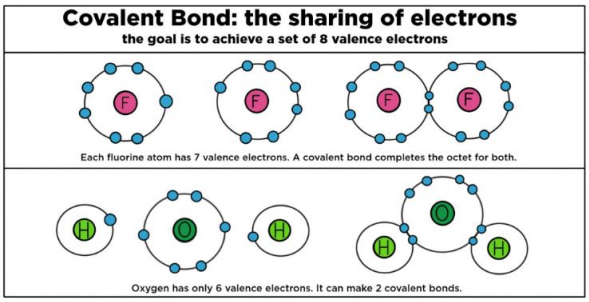
Non-metals with their large core charges, have a strong attraction for their valence electrons, so those electrons are not free to move in a current. As a result, non-metals make good insulators. When non-metals react with other non-metals, they form Covalent Bonds, in which they share pairs of valence electrons. Using the Quantum Mechanical model of atoms to explain this, valence electrons occupy orbitals that can be: empty, contain one electron, or contain two electrons. The most stable condition is for all the orbitals to be filled -- i.e. containing two electrons, as is the natural case for the Ideal Gases, and which explains why they do not readily enter into chemical reactions. Covalent bonds result in atoms with single electrons in their orbitals sharing those electrons with other similar atoms so that both atoms now have full orbitals. The shared orbitals bind the atoms together tightly. The electrons in these new compound orbitals are not free to move through the material, so covalently-bonded compounds are, under normal conditions, non-conductive. They continue to be non-conductive when dissolved in water.



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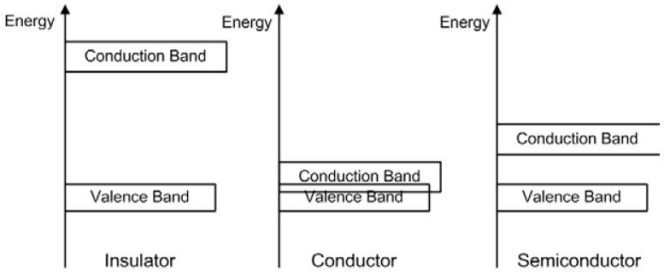
You'll notice in the previous discussion statements like "under normal conditions" and "do not readily conduct". The fact of the matter is that, given sufficient energy, any electron can be dislodged and can become a Free Electron until it loses its energy and is pulled back into either its original location or another similar location. In other words, any material can be made to conduct if the electrical field is strong enough to dislodge it or if it absorbs sufficient energy from, say, a photon striking it.

Up to this point, we've discussed Conductors and Insulators. The real point of this discussion was to get to Semiconductors. In a small band of the periodic table between the conductors and insulators, you'll find a group of elements called the semiconductors. The two most common of these, silicon and germanium, each have four valence electrons, which puts them in the middle between the metals (<4) and the non-metals (>4). Thus, they exhibit characteristics which are neither metallic nor non-metallic. They conduct more readily than non-metals,

but they enter into covalent bonds with non-metals. However, their electrons are not as tightly bound into covalent bonds as with typical non-metals, and can be relatively easily become free electrons. The differences between Insulators, Conductors, and Semiconductors can be pictured using an Energy Diagram.

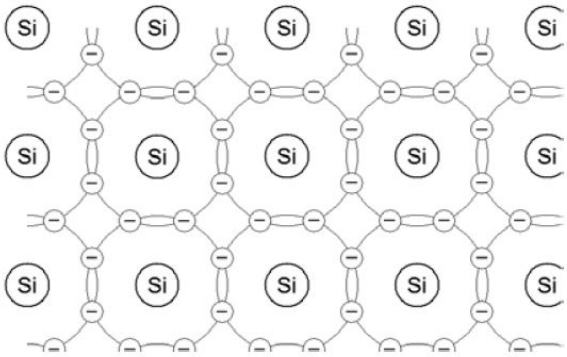


A lot of energy is required to make an insulator conduct, i.e. to move its electrons out of the valence band into the conduction band as free electrons. Almost no energy is required to move the electrons in a conductor, as there are already free electrons in the conduction band. Semiconductors lie halfway between these extremes.

Doped Semiconductor Materials

Silicon is the most commonly-used semiconductor material, so we'll focus on it as we move toward an understanding of how the diode works. Silicon has four valence electrons, and is therefore Tetravalent.

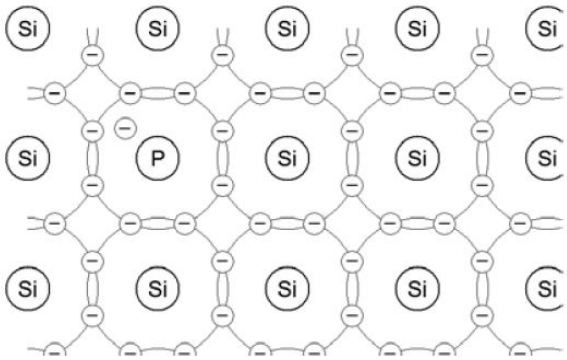
In one of its natural conditions, silicon bonds covalently into a tetrahedral crystal structure. A Lewis Diagram shows a flattened version of the bonds that take place.



Pure silicon is also called "Intrinsic silicon", because it contains no other material than silicon atoms. This is not only very difficult to achieve, but it also doesn't bring us any closer to the answer as to how a diode works. It is much more likely that a crystal of silicon will contain some impurities, and will therefore be "Extrinsic silicon". If the bulk of the impurity added to the silicon crystal is the same element, we refer to the result as "Doped silicon".

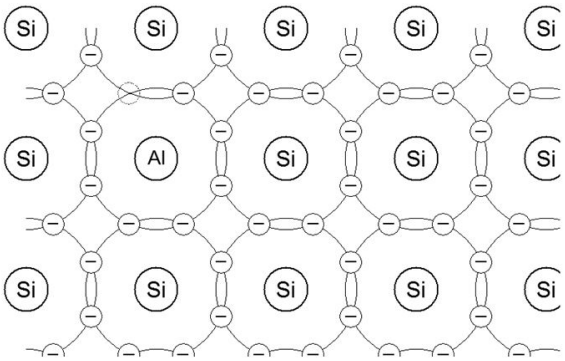
N-Type silicon

If a very small amount of a five-valence electron, or Pentavalent, dopant is introduced into a silicon crystal, the Pentavalent atoms will be forced into the crystal lattice structure of the silicon crystal, but only four of the electrons will be accepted into the covalent bonds. That leaves the fifth one as a Free Electron, and, just in metal, this electron will be able to move in a current, making this doped crystal a conductor. Since the pentavalent dopand has donated a negatively charged Carrier, the new material is referred toas N-Type Material. The Pentavalent Dopant is referred to as a Donor. The following Lewis Diagram shows a single phosphorus atom trapped in a silicon crystal, and its resulting Free Electron.



P-Type silicon

If a very small amount of a three-valence electron, or Trivalent, dopant is introduced into a silicon crystal, the Trivalent atoms forced into the crystal will not be able to contribute an electron to all four of the surrounding silicon atoms, so there will be an orbital with only one electron in it. This orbital has an electrical attraction to any available electrons which may temporarily "fall in", so these are referred to as Holes. If a source of electrons is connected to one end of the crystal and a positive potential is connected to the other end, electrons will migrate from hole to hole through the crystal, again resulting in a current. Although the Holes are stationary, they appear to be moving in the opposite direction to the flow of electrons, so this is referred to as Hole Current. The Trivalent Dopant provide places for electrons to fall into so it is called an Acceptor.



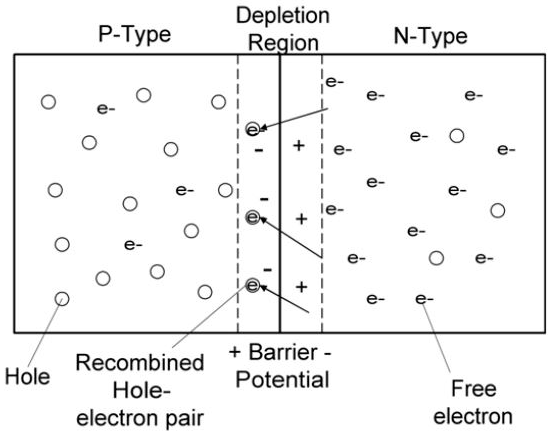
In each of these types of material, it is still possible for electrons in covalent bonds to be ejected by sufficient incoming energy, but this small amount of current is only noticeable if there is little other current. Consequently, the main form of current is referred to as Majority Current, and the current from the valence electrons is called Minority Current. Let's summarize this by filling in the following table.

	N-Type	P-Type
Dopant	_____	_____
Dopant Type	_____	_____
Majority Carrier	_____	_____
Minority Carrier	_____	_____

So, now we have two new conductive materials. That still doesn't answer the question of how the diode works. The "magic" happens when we combine these two materials.

The P-N Junction

Normally, when we connect two conductors together, we expect to just have a longer conductor. However, when we bond P-Material to N-Material, we observe some very interesting behaviour. Here's a block diagram to help with understanding what happens.



- Right at the connection point, or P-N Junction, the free electrons in the N-Type material are "pulled into" the holes in the P-Type material, in a process called "Recombination". That means, at the junction there are no charge carriers, therefore the P-N Junction in its natural state is a non-conductor.
- A net positive charge collects on the N-Type side and a net negative charge collects on the P-Type side of the barrier. This results in a potential difference (voltage) referred to as the Barrier Potential.

What an unexpected result! Connecting two conductors together has created a non-conductor!

Let's investigate the Barrier Potential a bit more. For silicon junctions, this barrier potential is between 0.5 V and 0.8 V. Not very big! In fact, a potential this small is easy to overcome. Recall, from your Basic Electricity course, that in a circuit with two voltage sources in series, current will flow in the direction dictated by the larger source. In other words, the bigger source overcomes the potential from the smaller

source, and drives current "backwards" through it.

In essence, that's what happens to the P-N Junction when we connect an opposing external voltage source to it. To do this, we apply the positive side of the source to the P-Type material and the negative side to the N-Type material. The negative side of the power supply drives electrons into the N-Type side of the junction, and the positive side of the power supply pulls electrons out of the holes in the P-Type material. With carriers on both sides of the junction, it turns back into a conductor, and current flows.

Forward Biasing is the term used to describe applying an external power supply greater than the barrier potential to a P-N Junction with positive to the P-Type material and negative to the N-Type material. Forward Biasing results in a flow of current through the junction. The resistance of the junction will be very low.

Reverse Biasing is the opposite situation. If an external power supply is applied with the negative side to the P-Type material and positive to the N-Type material, the positive side of the supply draws electrons away from the barrier on the N-Type side, and the negative side of the supply drives electrons into the holes in the P-Type material,widening the barrier and preventing the flow of current. Since no current flows, the junction appears as an *open circuit* or a very high resistance, and the voltage across it will match the supply voltage. In other words, the reverse-biased P-N Junction has a barrier potential essentially equal to the supply voltage.

Reverse Breakdown will occur if the power supply voltage is increased beyond the maximum voltage the P-N Junction can withstand. At this point, the electrons cascade through the material as they would through a metal conductor, and the resistance becomes very low. (Reverse Breakdown occurs at different voltages for each device, depending on the way the device has been constructed.)

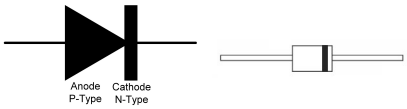
Thermal Destruction happens very quickly in either the forward or reverse direction if the resulting current is too great. Recall that $P=I^2R$. Even though the resistance is low, the squared current part of the calculation can result in a lot of power.

Circuit Biasing involves placing current-limiting devices, usually resistors, in series with the P-N Junction to limit the current and thereby prevent Thermal Destruction. **Don't put a P-N Junction directly across a power supply! You must limit the current using Circuit Biasing!**

The Diode

A single P-N junction, wired with connections to the P-Type and N-Type material, is called a ***Diode***. Diodes come a lots of different shapes and varieties. In your parts kit, you have Small Signal Diodes (used to control small currents, usually for logic or radio frequency applications), Rectifier Diodes (used for high-current and often high-voltage applications like power supplies), and Zener Diodes (designed with carefully-controlled Reverse Breakdown voltages for controlling voltages in regulated power supplies).

The symbol for a diode is shown below, along with a picture showing a typical diode and the way the polarity is indicated on the package.



Based upon what you've learned about the P-N Junction, answer the following questions:

To forward bias the diode, connect an external power supply and resistor with

(a) Negative to the Anode and Positive to the Cathode

(b) Positive to the Anode and Negative to the Cathode

If the power supply was wired up the opposite way to the correct answer above,

(a) The diode would experience Thermal Destruction

(b) Current would flow

(c) The diode would be reverse-biased

Online Homework System

Assignment Worksheet
1/9/23 - 1:35:48 PM MST

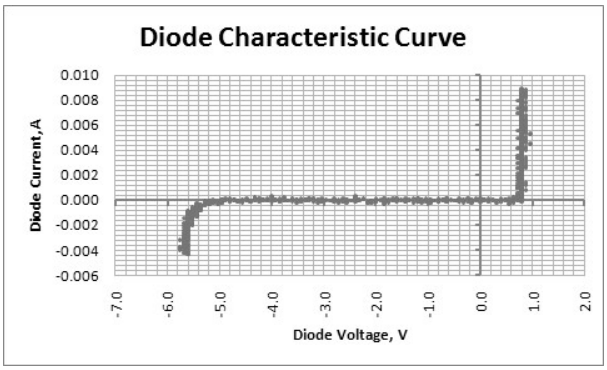
Name: _____ **Class:**

Class #: _____ **Section #:** _____

Instructor: Ross Taylor **Assignment:** Diode Models

Question 1: (1 point)

The behaviour of the diode in response to changing conditions in the biasing circuit is surprisingly complex, as shown in the oscilloscope X-Y trace below.



This particular diode is a Zener diode, designed with a specific Reverse Breakdown voltage of 5.6 V. Notice the following:

1. Between approximately -5 V and +0.6 V, the current is essentially zero. However, with higher resolution, we would actually see a small current, perhaps 500 nA, flowing because of the Minority Carriers in the silicon.
2. As we approach 0.7 V, the current increases in an approximately parabolic, or second order manner.
3. Beyond this point, the current increases rapidly with very little change in voltage. However, the voltage does increase slightly, indicating that the diode has an internal resistance. Since V=IR, the slope of this section would be 1/R.
4. Also, as we approach -5.6 V, the current increases in the opposite direction, again in an approximately parabolic manner.
5. Behond this point, the current again increases rapidly with very little change in voltage. Further analysis would indicate that the slope of this graph, again 1/R, would be quite similar to the slope at +0.7 V.

The condition described in #1 above is the off condition of the diode, where current is practically zero. Most of it would be in the Reverse Biased region, but there is a small section that is technically forward biased but not with a high enough voltage to overcome the Barrier Potential.

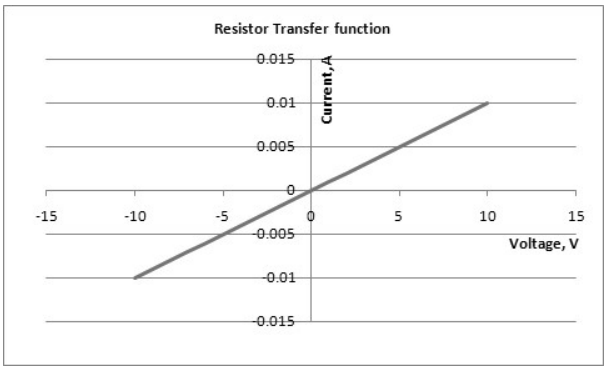
The condition described in #3 above is the Forward Biased region, where the voltage remains relatively constant at approximately the Barrier Potential.

The condition described in #5 above is the Reverse Breakdown region.

#2 is referred to as the Forward Knee, due to its rounded shape and sudden change in direction.

#4 is referred to as the Reverse Knee for the same reasons.

This is quite unlike what we would expect to see for a passive component, such as the resistor. This is the Characteristic "Curve" for a resistor:



In this case, a single expression describes the entire response of a resistor to a change in voltage:

$I = \frac{1}{R}V$, or simply Ohm's Law.

Modelling

To make sense of our world, we as humans "model" everything we see. A model is a simplified description of a system or situation that can be used to predict future outcomes or to help us respond and control the system or situation. Ohm's Law is a model of the behaviour of a resistor, and it is simplified in that it doesn't take into account the effect of temperature on resistance, it doesn't include the "skin" effect

of high frequency changes in voltage on the resistance, it doesn't take into account the inductance or capacitance of a physical resistive component, it doesn't account for changes in resistance due to humidity or radiation, and it doesn't tell us what happens if too much current is driven through the resistor.

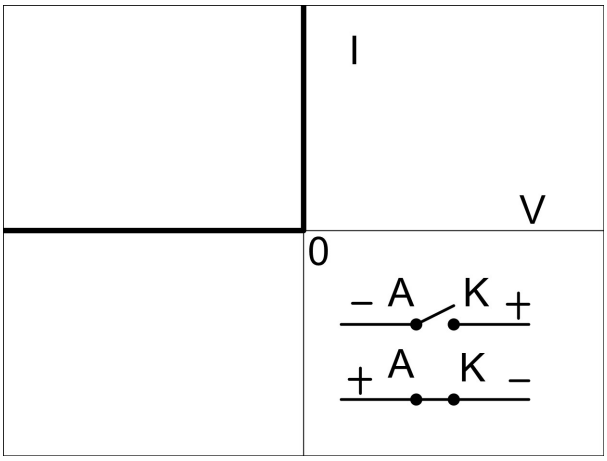
When it comes to diodes, our models typically ignore the parabolic regions at the Forward and Reverse Knees.

Then, depending on how accurately we need to model the device, we may ignore other features:

- We often don't include the Reverse Breakdown region, as we assume our circuit will be biased to avoid this.
- We often don't include the slope of the Forward bias region, treating the diode as if its dynamic internal resistance is zero.
- We may even overlook the fact that we need to overcome the Barrier Potential before the diode conducts.

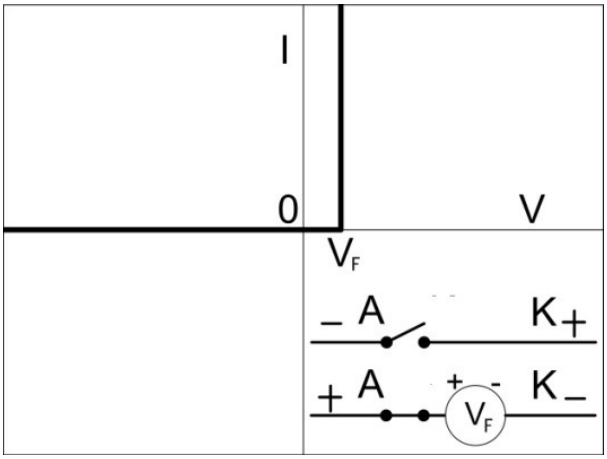
Ideal Model

This is the simplest model. It just says a diode conducts when forward biased and doesn't conduct when reverse biased -- a polarity-controlled switch, if you wish.



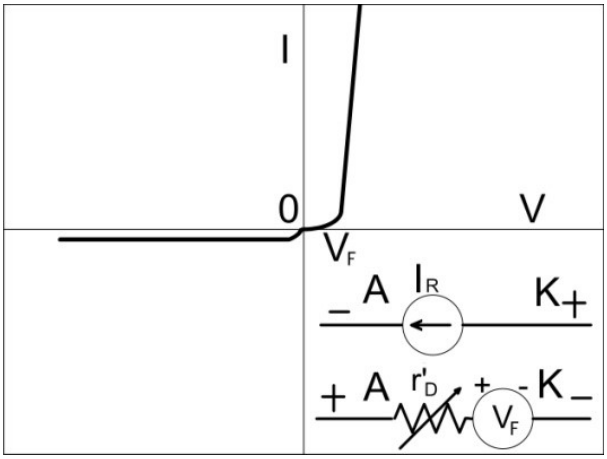
Practical Model

This one takes into account the Barrier Potential, which needs to be overcome before the diode can conduct. Otherwise, it behaves like a zero-ohm switch.



Complete Model

This one takes into account more of the actual characteristics, primarily the small internal resistance of the diode when it conducts and the small leakage current due to Minority Carriers. Although the Knees are shown as parabolas, we usually don't concern ourselves with that unless we have a good reason to.



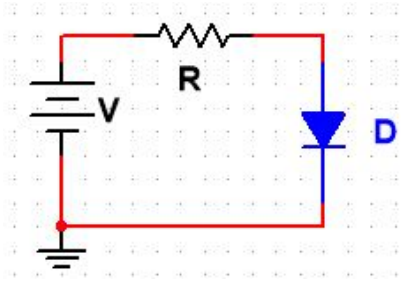
Applying Models

The question is: which model do I choose, when, and why?

In essence, it depends on how accurate the result needs to be and the circuit characteristics.

1. If all you care about is presence or absence of current (binary), use the Ideal Model.
2. If you're working with really large voltages, where 0.7 V is insignificant, and if the resistances are considerably greater than the diode's dynamic internal resistance, just use the Ideal Model.
3. If you're working with small voltages and reasonable-sized resistors (like most of what we do in this course), use the Practical Model.
4. If you're working with large currents in Forward Biasing or really big resistors in Reverse Biasing, you'll need the Complete Model to explain the otherwise-unexpected results you see.

Let's work with the following diagram.



Assume V is +6 V, the diode has a forward drop of 0.7 V, and R is 10 kΩ.

What current would the Ideal Model predict? _____ μA

What current would the Practical Model predict? _____ μA

What error does this represent? _____ %

Clearly, in this example, the Ideal Model is not providing us with an accurate answer.

Now, let's assume V is +100 V, and everything else is the same.

What current would the Ideal Model predict? _____ mA

What current would the Practical Model predict? _____ mA

What error does this represent? _____ %

In this example, the Ideal Model is adequate.

For the same basic circuit, but this time with a 22 Ω resistor, a power supply of +9.0 V, and a diode with a Barrier Potential of 0.7 V and an internal resistance of 8.3 Ω, let's compare what the Practical Model and Complete Model would predict.

What does the Practical Model say the voltage drop across the diode would be? _____ V

Using the Complete Model, determine the current in this circuit. _____ mA

Given that the Complete Model includes the Barrier Potential and the drop across the internal resistance in the diode's voltage drop, what is the voltage drop across the diode using this model? _____ V

What is the error introduced by using the Practical Model in this case? _____ %

Clearly, the Practical Model failed us in this example, as the high current results in a significant voltage drop across the internal resistance.

If a diode with a reverse leakage current of 500 nA is reverse biased in a series circuit with an 8.2 MΩ resistor, powered by a 12 V supply, what voltage would the Practical Model predict across the diode? _____ V

What voltage would the Complete Model predict across the diode? _____ V

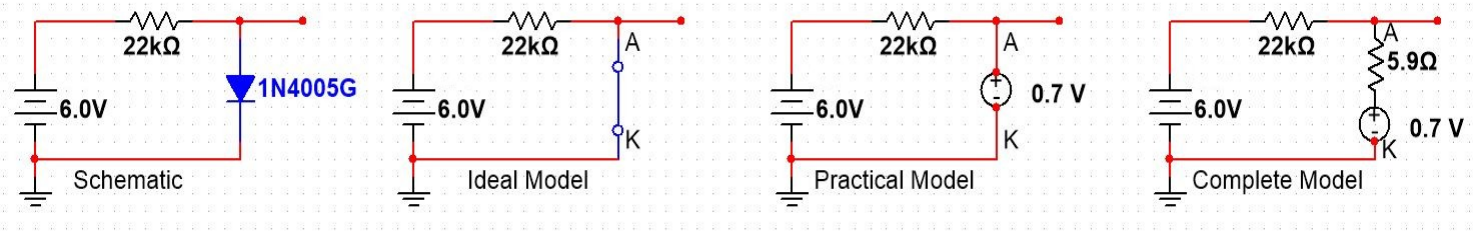
What is the error introduced by using the Practical Model in this case? _____ %

Again, with such a huge resistor in series, the leakage current becomes significant, and the Practical Model fails us.

Worked Examples -- Diode Model Comparisons

The following examples are provided as extra material for you to cover on your own time to help reinforce how to use the models, and, more importantly, to help you determine the conditions under which you may need to use a more accurate model. In each, the forward junction voltage is assumed to be 0.7 V, the internal resistance of the diode is assumed to be 5.9 Ω, and the reverse leakage current is assumed to be 500 nA. For each, the circuit current and the voltage across the diode (i.e. the voltage at the wire stub referenced to ground) are to be determined.

Worked Example 1:



Ideal Model:

- V_D is 0.0 V, since the closed switch is a short
- I = V_R/R = (6 - 0)/22 kΩ = 273 μA

Practical Model:

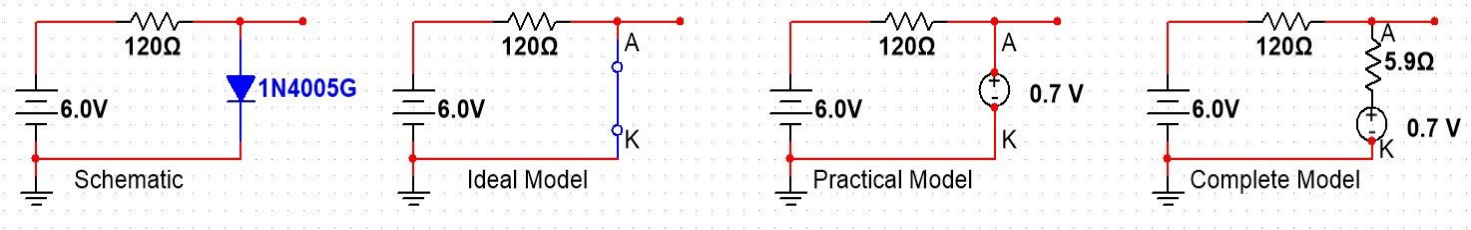
- V_D = 0.7 V
- I = V_R/R = (6 - 0.7)/22 kΩ = 241 μA

Complete Model:

- We'll have to start with the current, using KVL: I = (6.0 - 0.7)/(22 kΩ + 5.9 Ω) = 241 μA
- V_D = 0.7 + I * r'$_D$ = 0.701 V

Clearly, in this example, the Ideal Model is significantly incorrect, but the Practical and Complete models predict essentially the same result; so, for a situation in which the power supply is relatively small and the current is limited by a substantial series resistor, we don't need to use the Complete Model.

Worked Example 2:



Ideal Model:

- V_D is 0.0 V, since the closed switch is a short
- I = V_R/R = (6 - 0)/120 Ω = 50 mA

Practical Model:

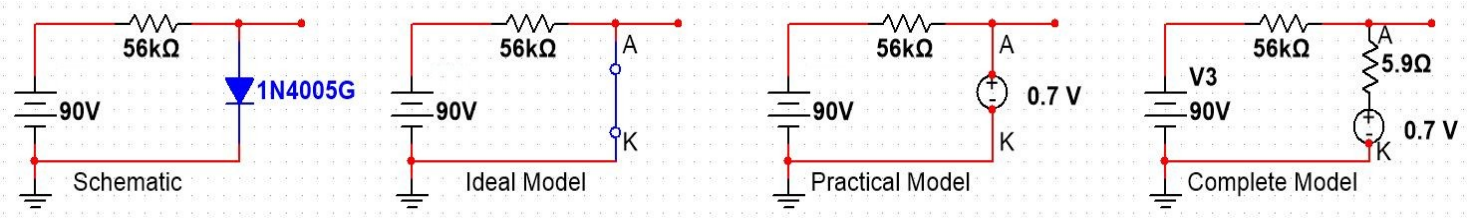
- V_D = 0.7 V
- I = V_R/R = (6 - 0.7)/120 Ω = 44.2 mA

Complete Model:

- We'll have to start with the current, using KVL: I = (6.0 - 0.7)/(120 Ω + 5.9 Ω) = 42.1 mA
- $V_D = 0.7 + I * r'_D = 0.948$ V

In this example, the Ideal Model is significantly incorrect as in the previous example. But now the Practical is also significantly incorrect, so a proper prediction can only be made using the Complete model. So, for a situation in which the current is quite high as allowed by a relatively small series resistor, we need to use the Complete Model.

Worked Example 3:



Ideal Model:

- V_D is 0.0 V, since the closed switch is a short
- $I = V_R/R = (90 - 0)/56$ kΩ = 1.61 mA

Practical Model:

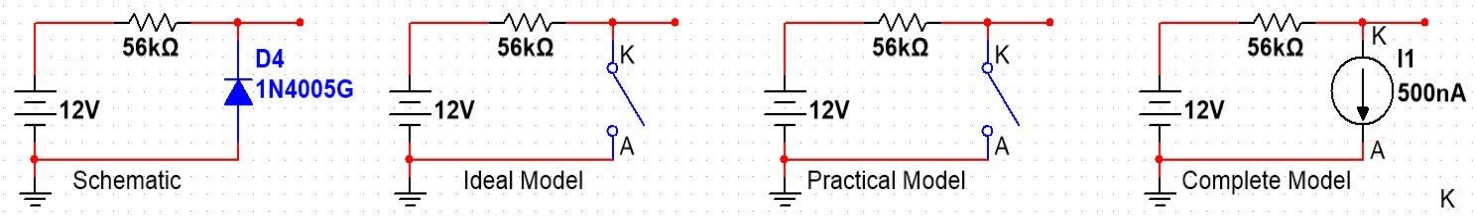
- $V_D = 0.7$ V
- $I = V_R/R = (90 - 0.7)/56$ kΩ = 1.59 mA

Complete Model:

- We'll have to start with the current, using KVL: I = (90 - 0.7)/(56 kΩ + 5.9 Ω) = 1.59 mA
- $V_D = 0.7 + I * r'_D = 0.709$ V

In this example, the currents predicted by all three models are practically the same, so the Ideal Model would be sufficient for current determination in a circuit where the supply voltage is considerably larger than the diode forward drop. The voltage across the diode is, of course, still significantly wrong, but the voltage across the resistor (90 V instead of 89.3 V) is not significantly incorrect.

Worked Example 4:



Ideal Model:

- I = 0 A because of the open circuit
- V_D = 12 V, since there is no current through the resistor, and therefore no voltage drop from the supply.

Practical Model:

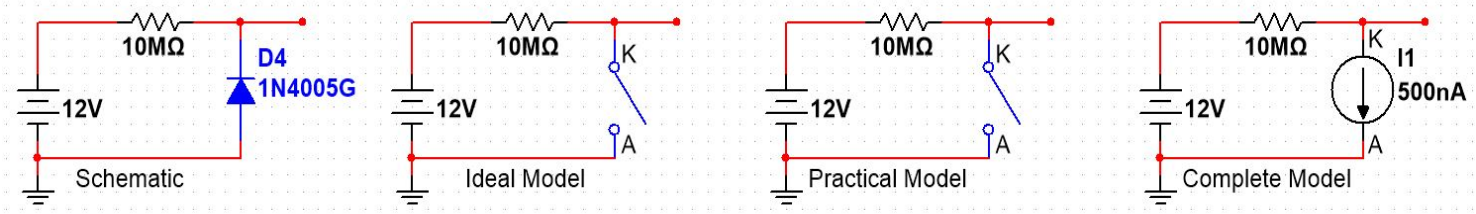
- I = 0 A because of the open circuit
- V_D = 12 V, since there is no current through the resistor, and therefore no voltage drop from the supply.

Complete Model:

- I = 500 nA
- $V_D = 12 - I * R = 12 - 500$ nA * 56 kΩ = 11.97 V

In this case, the Ideal and Practical models predict the same result, so the Ideal model is suitable. The Complete model also predicts almost the same result for the voltage, and 500 nA is pretty insignificant, so we don't need the extra complication of the Complete model in a situation where the diode is reverse-biased and in series with a "reasonably sized" resistor.

Worked Example 5:



Ideal Model:

- I = 0 A because of the open circuit
- V_D = 12 V, since there is no current through the resistor, and therefore no voltage drop from the supply.

Practical Model:

- I = 0 A because of the open circuit
- V_D = 12 V, since there is no current through the resistor, and therefore no voltage drop from the supply.

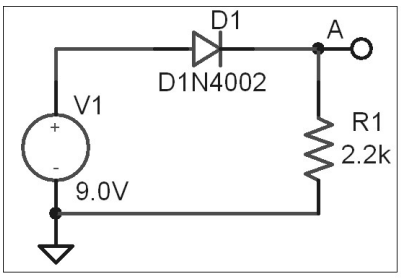
Complete Model:

- I = 500 nA
- V_D = 12 - I * R = 12 - 500 nA * 10 MΩ = 7.00 V

In this case, the Ideal and Practical models predict the same incorrect result, so the Complete model is the only one making accurate predictions. In this situation, the very large series resistor introduces a significant voltage drop even with a seemingly insignificant leakage current.

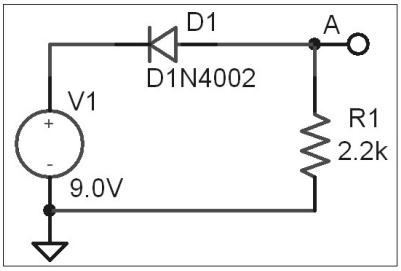
Using the Practical Model

Typically, in this course, we will use the Practical Model to predict our results. Here are some examples for you to practice and learn with. Assume the diode forward voltage drop is 0.7 V in each case. Some worked examples are provided below to help you establish the underlying concepts and the application of the model to replace the diode with standard electrical components.



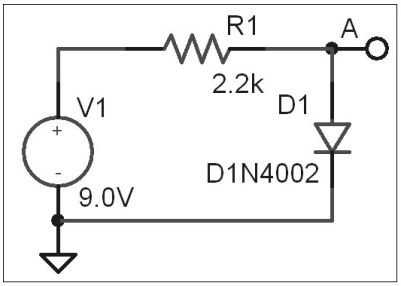
V_A = _____ V

I = _____ mA



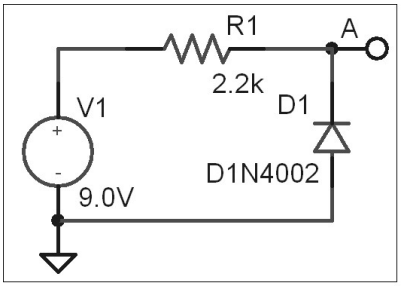
V_A = _____ V

I = _____ mA



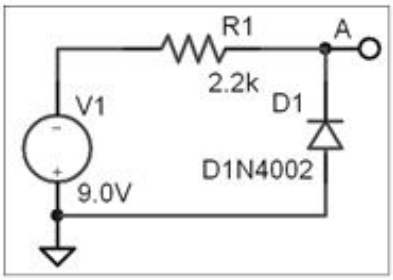
V_A = _____ V

I = _____ mA



V_A = _____ V

I = _____ mA



V_A = _____ V

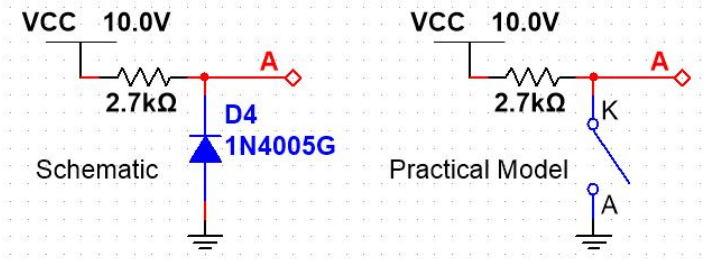
I = _____ mA

Notice that we still use Ohm's Law and Kirchhoff's Laws throughout. All we need to to is replace the diode with the appropriate model, and the basic laws of electricity apply.

Worked Examples

Determine the voltage at point A and the current through the diode in each of the circuits below. Assume the forward diode voltage drop for each diode is 0.7 V.

Worked Example 6:

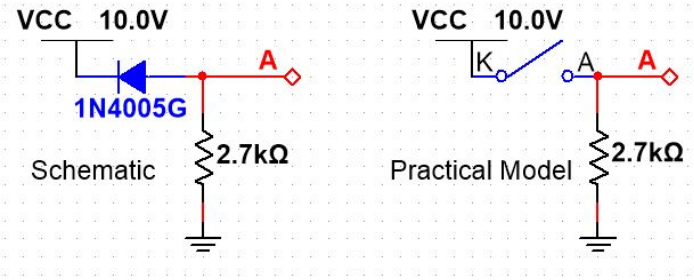


Since the diode is reverse biased (current is attempting to flow from VCC to ground, and encounters the Cathode as a "brick wall"), we choose the reverse biased model of the diode -- an open switch.

- The current through an open circuit is zero.
- The voltage at point A can be determined mathematically, as it will be equal to the source voltage minus the voltage drop across the resistor: $V_A = V_{CC} - I * R$ and, since I is zero, $V_A = 10.0\ V - 0*2.7\ k\Omega = 10.0\ V$.

(Don't forget this solution! We will end up using this version of KVL over and over again in this course! When given a current, we can only find voltage drops across resistors, not across active components, so we use KVL to find out what's left across the active component.)

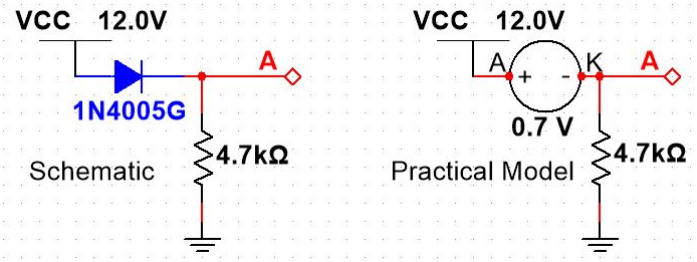
Worked Example 7:



Since the diode is reverse biased (current is attempting to flow from VCC to ground, and encounters the Cathode as a "brick wall"), we choose the reverse biased model of the diode -- an open switch.

- The current through an open circuit is zero.
- The voltage at point A can be determined mathematically, as it will be equal to the voltage drop across the resistor: $V_A = I * R$ and, since I is zero, $V_A = 0*2.7\ k\Omega = 0.0\ V$.

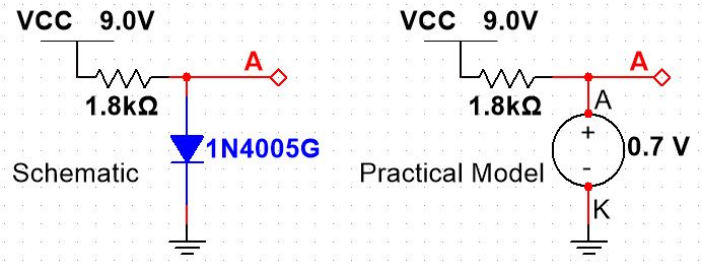
Worked Example 8:



Since the current attempting to flow from VCC to ground encounters the anode and can flow in the direction of the "arrow", the diode will be forward-biased. Therefore, we replace it with the Practical forward-biased model.

- The voltage at A, referenced to ground, is $V_{CC} - V_D = 12.0\ V - 0.7\ V = 11.3\ V$
- The current, determined using the resistor, is $I = \Delta V_R/R = (V_{CC} - V_D)/R = 11.3\ V/\ 4.7\ k\Omega = 2.40\ mA$

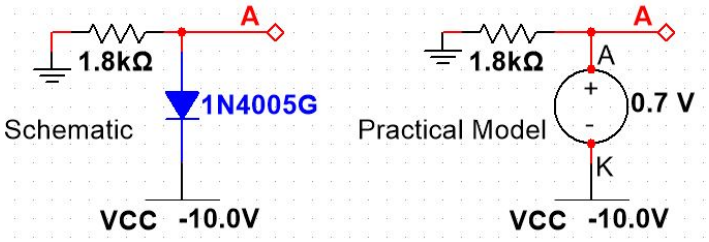
Worked Example 9:



Since the current attempting to flow from VCC to ground encounters the anode, the diode will be forward-biased. Therefore, we replace it with the Practical forward-biased model.

- The voltage at A, referenced to ground, is $V_D = 0.7\ V$.
- The current, determined using the resistor, is $I = \Delta V_R/R = (V_{CC} - V_D)/R = (9.0\ V - 0.7\ V)/1.8\ k\Omega = 4.61\ mA$

Worked Example 10:



Since the current attempting to flow from ground to the negative source, VCC, encounters the anode, the diode will be forward-biased. Therefore, we replace it with the Practical forward-biased model.

- The voltage at A, referenced to ground, is 0.7 V above VCC. From KVL, $V_A = V_{CC} + V_D$ = = -10.0 V + 0.7 V = -9.3 V
- The current, determined using the resistor, is I = $\Delta V_R/R$ = (0 - -9.3 V)/1.8 kΩ = 5.17 mA

There are lots more variations on this theme, but it always comes down to:

- Use KVL to determine the voltage at the point of interest
- Use Ohm's Law or KVL to determine the current using the voltage across a resistor.

Online Homework System

Assignment Worksheet
5/31/21 - 9:16:04 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA01 Semiconductor Theory Quiz

Question 1: (1 point)

A single crystal of pure silicon is considered to be _____

Question 2: (1 point)

Extrinsic semiconductor is formed by doping a region within a single crystal of pure semiconductor with atoms of a certain impurity element. The foregoing statement is:

(a) True
(b) False

Question 3: (1 point)

P-type semiconductor has been doped with which type of impurity? _____

Question 4: (1 point)

N-type semiconductor has an abundance of _____

Question 5: (1 point)

In P-type semiconductor, the majority carriers are _____

Question 6: (1 point)

Electrons form the minority carriers in which type of semiconductor material? _____

Question 7: (1 point)

Regarding available current carriers in semiconductor material:

(a) "Free" electrons and "free" holes both reside in the conduction band of quantum energy levels.

(b) "Free" electrons reside in the conduction band, but "free" holes reside in the valence band of quantum energy levels.

(c) "Free" electrons and "free" holes both reside in the valence band of quantum energy levels.

(d) "Free" electrons reside in the valence band, but "free" holes reside in the conduction band of quantum energy levels.

Question 8: (1 point)

A modern semiconductor junction between P-type and N-type silicon is formed when two different crystals of semiconductor material are physically bonded together. The foregoing statement is:

(a) True
(b) False

Question 9: (1 point)

At an unbiased semiconductor junction, after stabilization, the depletion region contains:

(a) positive ions on the P-side and negative ions on the N-side, and no available majority carriers

(b) acceptor atoms on the P-side and donor atoms on the N-side, complete with available majority carriers

(c) negative ions on the P-side and positive ions on the N-side, and no available majority carriers

(d) donor atoms on the P-side and acceptor atoms on the N-side, complete with available majority carriers

Question 10: (1 point)

The depletion region is caused by majority carriers from impurity atoms close to the junction on one side diffusing across the junction and recombining with opposite polarity majority carriers from impurity atoms near the junction on the other side. The foregoing statement is:

(a) True
(b) False

Question 11: (1 point)

The terms anode and cathode apply to a diode as follows:

(a) The anode is the terminal that connects to N-type semiconductor, and the cathode is the terminal that connects to P-type semiconductor.

(b) The anode is always the terminal that is biased by a negative voltage, and the cathode is always the terminal that is biased by a positive voltage.

(c) The anode is the terminal that connects to P-type semiconductor, and the cathode is the terminal that connects to N-type semiconductor.

(d) The anode is always the terminal that is biased by a positive voltage, and the cathode is always the terminal that is biased by a negative voltage.

Question 12: (1 point)

When a zener diode exhibits zener breakdown,

(a) it inevitably experiences catastrophic failure.

(b) its voltage and current are related by Ohm's law.

(c) its reverse voltage is more-or-less constant, but its reverse current must be determined by external circuitry.

(d) its reverse current is more-or-less constant, but its reverse voltage must be determined by external circuitry.

Question 13: (1 point)

When a diode is properly forward-biased,

(a) its forward current is more-or-less constant, but its forward voltage must be determined by external circuitry.

(b) its voltage and current are related by Ohm's law

(c) no current will flow, and the diode voltage will be equal to the supply voltage.

(d) its forward voltage is more-or-less constant, but its forward current must be determined by external circuitry.

Question 14: (1 point)

When a rectifier diode is reverse biased by a supply voltage less than its reverse breakdown,

(a) its reverse current is a more-or-less constant non-zero value, but its reverse voltage must be determined by external circuitry.

(b) its reverse voltage is less than the supply voltage, but its reverse current must be determined by external circuitry.

(c) its voltage and current are related by Ohm's law.

(d) its current will be effectively zero and its voltage will be equal to the supply voltage.

Question 15: (1 point)

The forward-biased voltage of an unknown diode has been measured as 1.86 V. Which type of diode is this likely to be?

(a) Schottky

(b) Germanium

(c) LED

(d) Silicon

Question 16: (1 point)

In a stable, unbiased semiconductor junction, the barrier potential:

(a) prevents any flow of carriers across the junction.

(b) accelerates both minority and majority carriers across the junction.

(c) prevents the flow of minority carriers across the junction but accelerates majority carriers across the junction.

(d) prevents the flow of majority carriers across the junction but accelerates minority carriers across the junction.

Question 17: (1 point)

Forward bias means a negative voltage is connected to P-type semiconductor and a positive voltage is connected to N-type semiconductor. The foregoing statement is

(a) True
(b) False

Question 18: (1 point)

If reverse bias is applied to a semiconductor junction, the depletion region gets wider. The foregoing statement is

(a) True
(b) False

Question 19: (1 point)

In a signal diode or rectifier diode, significant current normally flows only when:

(a) the diode is forward biased with a voltage greater than the barrier potential.

(b) the diode is reverse biased with a voltage less than the breakdown voltage.

(c) the diode is forward biased with any positive voltage.

(d) the diode is either forward or reverse biased.

Question 20: (1 point)

If a signal or rectifier diode is reverse biased, and is not experiencing breakdown:

(a) majority current will not flow, but minority current will flow, to a maximum of "reverse saturation current".

(b) neither majority nor minority current will flow at all.

(c) both majority and minority current will flow freely.

(d) minority current will not flow, but majority current will flow, to a maximum of "reverse saturation current".

Online Homework System

Assignment Worksheet
6/7/22 - 10:46:59 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Lab01 Diode Characteristics

Question 1: (10 points)

NOTE: Once you complete your Pre-Lab Assignment and move on to the Lab Activity, you will not be able to re-open the Pre-Lab for further editing! Do not go to the "NEXT" page (i.e. the Lab Activity) until you have completed the Pre-Lab!

Diode Check

Many Digital Multimeters (DMMs) have a "Diode Check" function available. In this setting, the meter attempts to drive a current through the diode, and measures the resulting voltage across the device. Current is driven from the meter's RED lead and returns on the meter's BLACK lead. If little current is detected, the meter reports "OPEN"; otherwise, it reports the voltage measured. Checking a diode involves observing what the meter reports for both Forward and Reverse biasing. You will have to physically reverse the meter leads to see these two conditions.

1. If a DMM is set to the "Diode" function, with the RED lead connected to the Anode of a silicon diode and the Black lead connected to the Cathode,

   (a) the meter will report "OPEN"

   (b) the meter will display approximately 0.7 V

Unfortunately, many DMMs have not been programmed to include LEDs as diodes, so even though the LED is good, the meter will report it as OPEN.

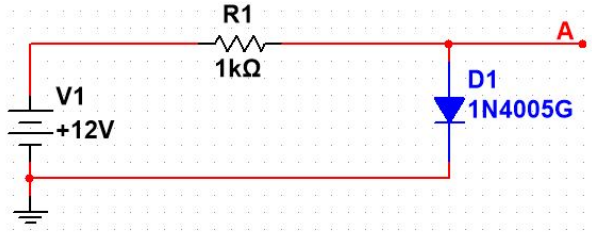
Some meters do not have a "Diode Check" function. These meters can be used to check diodes using the "OHMS" setting. Ohmmeters also work by attempting to drive a current through the attached device, then measuring the current through an internal reference resistor. Each scale setting for the meter will use a different combination of voltages and internal resistors to maximize the resolution of the result. Picking an appropriate range involves some consideration: too low a range, and the internal voltage might not be high enough to forward bias the diode; too high a range, and the internal resistor may limit the current to the point where the diode doesn't actually conduct. Typically, we set the meter to the 1 kΩ range to get reasonable results. Again, current is driven out of the RED lead and returns on the BLACK lead. Some resistance value will be displayed if a good diode is forward biased, but the meter will indicate OVERLIMIT (usually OL) if the diode is open or is reverse biased. Again, a good diode check involves checking the results for both Forward and Reverse biasing.

2. If the RED lead of an ohmmeter is connected to the Cathode of silicon diode and the BLACK lead is connected to the Anode,

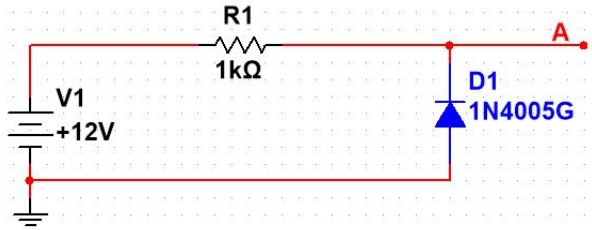
   (a) the meter will display some measurable resistance

   (b) the meter will report an overlimit (OL or OVLD)

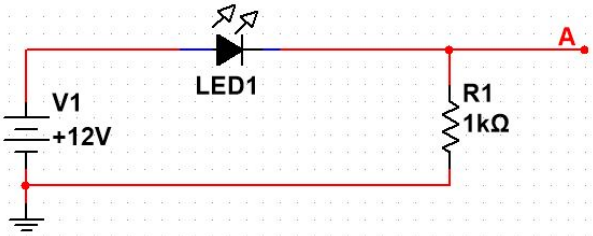
Determine the voltage expected at point A referenced to ground (i.e. V_A) for each of the following circuits. For regular diodes, assume a Barrier Potential of 0.7 V. For the Red LEDs (indicated by "light" arrows and an LED reference) assume a Barrier Potential of 1.8 V.

3. 

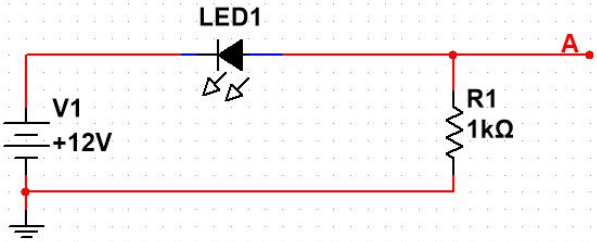
V_A = _____ V

4. 

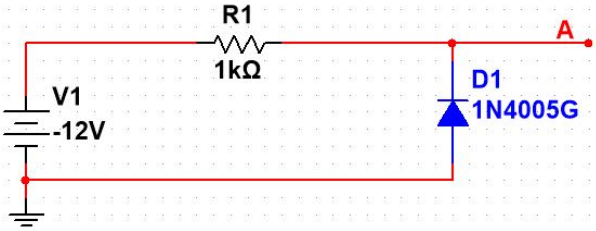
V_A = _____ V

5. 

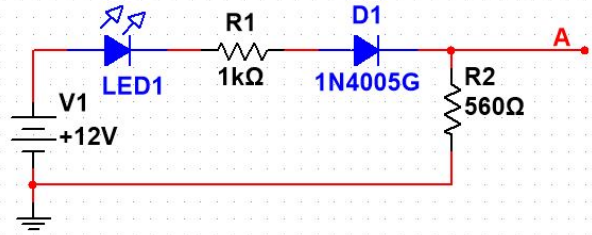
V_A = _____ V

6. 

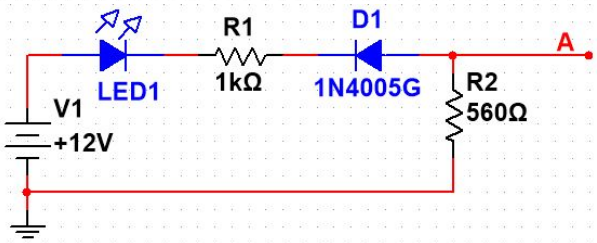
V_A = _____ V

7. 

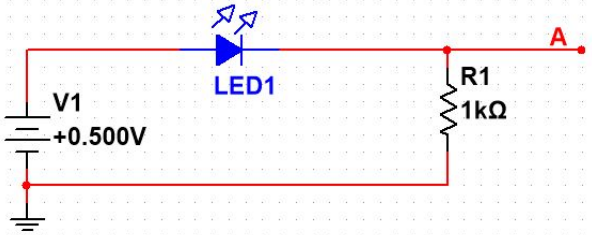
V_A = _____ V

8. 

V_A = _____ V

9. 

V_A = _____ V

10. 

V_A = _____ V

You have now finished the Pre-Lab.

You may wish to take a screenshot of your results to help you with the Lab Activity.

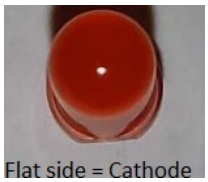
Move on to the Lab Activities. Do not click "submit" yet!

How Did I Do?

Question 2: (10 points)

Diode Checking

- Put a 1N400x diode ('x' could be anything from 1 to 7, depending on what has been selected for your kit) onto your breadboard to provide easy access to the anode and cathode leads.
- Set up your DMM for diode testing. (Note: You are expected to use the lab multimeter. However, on your own time, you may want to try the HT118A DMM. This involves turning the rotary switch to the setting for ohms, continuity, and diodes, then pressing the "Func." switch twice (until a diode schematic symbol appears on the screen)).
- The Cathode of the diode is indicated by a line drawn around the barrel of the diode.
- The Cathode of the LED is indicated by a flat side on the plastic ridge around the base of the LED.



1. Connect the DMM and the diode together so the DMM forward-biases the diode, and answer the following question:

When a "good" diode is connected to the diode checker so as to be forward biased, the display shows _____

2. Do what it takes to reverse-bias the diode with the DMM, and answer the following question:

When a "good" diode is connected to the diode checker so as to be reverse biased, the display shows _____

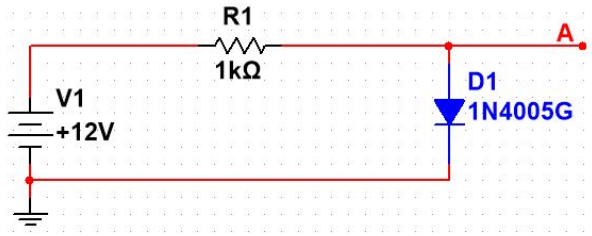
3. Replace the diode with a Red LED. When a "good" LED is forward biased by the diode checker, the display shows _____
4. When a "good" LED is reversed biased by the diode checker, the display shows _____

Diode Biasing Circuits

Using a power supply set to produce 12 VDC, build and test each of the circuits from the Pre-Lab, included here for your convenience.

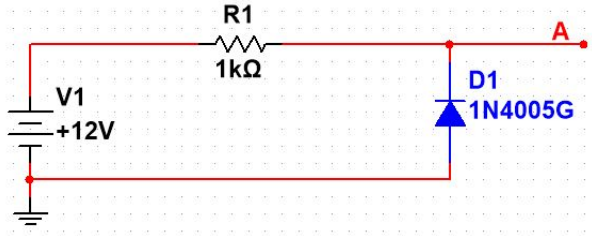
- Use your DMM to measure and record the voltage at point 'A' for each circuit, referenced to ground.

5.

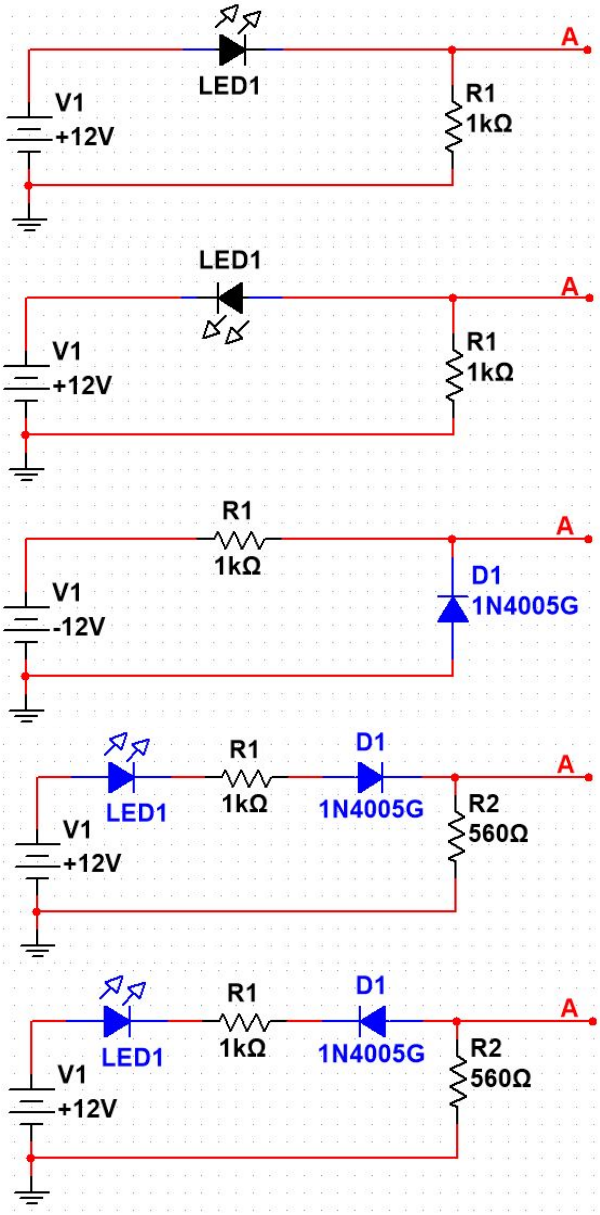


V_A = _____ V

6.



V_A = _____ V



7. V_A = _____ V
8. V_A = _____ V
9. V_A = _____ V
10. V_A = _____ V
11. V_A = _____ V

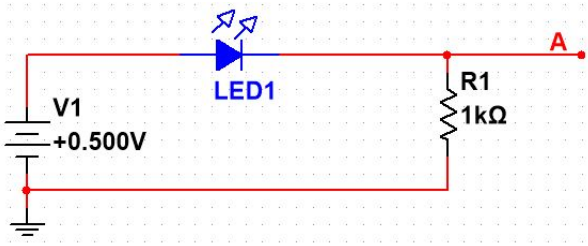
Using the resistors in the circuits, determine the current flowing in each circuit using $I = \frac{\Delta V_R}{R}$. Do NOT determine any of the currents using your understanding of Diode Models -- you need to use Empirical Data (measured values) in the lab to prove Theoretical Constructs (models), not the other way around.

5. I = _____ mA
6. I = _____ mA
7. I = _____ mA
8. I = _____ mA
9. I = _____ mA (Just submit the magnitude -- don't worry about polarity.)
10. I = _____ mA
11. I = _____ mA

Simulation

Use Multisim to create and analyze the remaining circuit.

- Use a "red_LED" from the "Diodes -> LED" group, as other digital indicators, etc., will not work as expected.
- Place a voltage probe at point 'A' to make a quick measurement of the voltage, referenced to ground.



12. V_A = _____ V; I = _____ mA (from a calculation using the voltage drop across R_1)

You have now completed this Lab. Click "Submit" to send out your work for grading.

Online Homework System

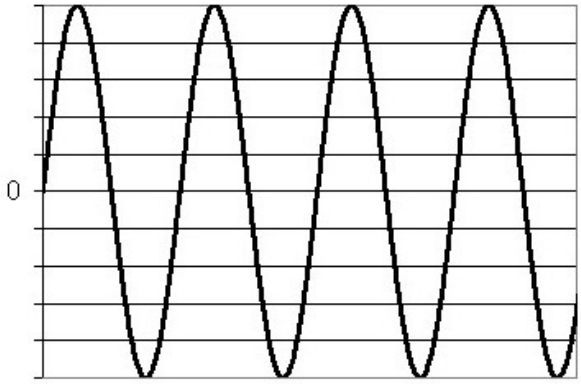
Assignment Worksheet
5/20/22 - 9:25:17 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Rectifier Circuits

Question 1: (1 point)

DC Power Supplies

Almost all electronic equipment runs on DC, but the power supplied across the world is almost universally AC, which has no DC component. The following oscilloscope trace shows a typical AC sinusoid, used in transmitting power.



For this signal, the Average Voltage, which corresponds roughly to the DC, is zero -- the signal spends as much time above the zero marker as it does below.

However, it's clear from experience that there is quite a bit of power available. How can that be, if P=IV, and V = 0? The answer is that power is based upon the Root Mean Squared Voltage (V_{RMS}), not the average voltage (V_{ave}). RMS is determined for a cycle of a signal by squaring each point, taking the average, then taking the square root of the result. Doing that accurately involves integrating the square of the signal, then taking the square root. For a sine wave, this produces the result

$$V_{RMS} = \frac{V_p}{\sqrt{2}}$$

Other waveforms have different results. For example, a triangle wave's $V_{RMS} = \frac{V_p}{\sqrt{3}}$. A square wave's $V_{RMS} = V_{\max}$, and a DC signal's $V_{RMS} = V_{ave} = V_{DC}$

So, all of these waveforms have power. If only we could find a way to harness that power as DC rather than AC.

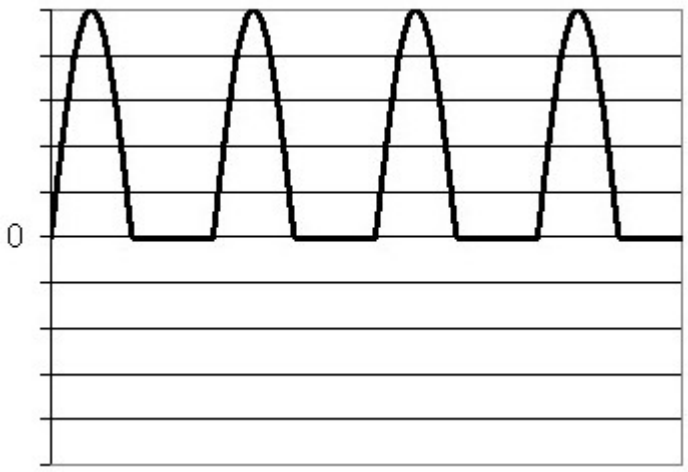
Question: DC can be isolated from AC power simply by filtering out the high frequency components using a Low Pass Filter, leaving only the DC, or 0 Hz, component.

(a) True
(b) False

Question 2: (1 point)

Half-Wave Rectification

That's where the diode comes into play. If we have a circuit that only conducts on the positive half wave of the sine wave, the average voltage would be positive, not zero, as shown in the following half-wave rectified signal.



In this case, the average (again, this corresponds to the DC component) is clearly positive, not zero. In fact, if you integrate the signal over one complete cycle, you arrive at

$$V_{ave} = \frac{V_p}{\pi}$$

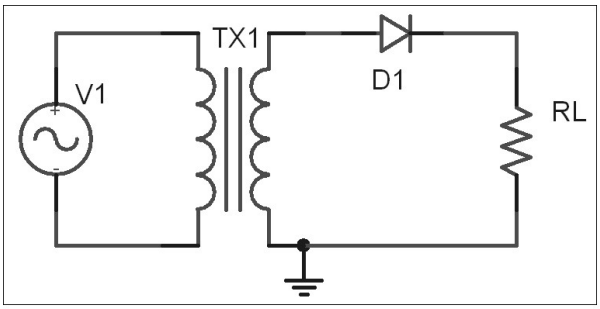
Also, if you perform an RMS analysis of this waveform, you discover that

$$V_{RMS} = \left| \frac{V_p}{2} \right|$$

Notice that this is smaller than the V_{RMS} for a sine wave by a factor of $\frac{1}{\sqrt{2}}$, which makes some sense, since part of the wave is missing.

The frequency of the half-wave rectified signal is the same as the frequency of the input signal -- it's just flat-lined for part of the cycle.

As indicated, we can use a diode to "cut off" half of the waveform. Typically, in our power supplies, we also use a transformer to reduce the amplitude of the original sine wave as well, as most of our working voltages are quite a bit smaller than the 120 V_{RMS} signal from our building wiring systems. Here's a typical Half-Wave Rectifier circuit:



The transformer steps down the voltage, then the diode allows current only when the incoming signal is positive with respect to ground. That current produces a voltage across the load resistor that's one diode drop below the input peak voltage.

Question: For the above circuit, V1 = 120 V_{AC} (that's shop talk for V_{RMS}) at 60 Hz, the transformer has a turns ratio of 8:1, the diode has a forward barrier potential of 0.7 V, and R_L = 220 Ω.

1. What is the peak voltage of the AC supply? _____ V_p
2. What is the peak voltage of the AC as seen at the secondary of the transformer? _____ V_p
3. Which peak will appear across the load resistor?

   (a) positive

   (b) negative

4. Using the practical model of the diode, what will the peak voltage of the signal across the load resistor be? _____ V_p
5. What is the frequency of the signal across the load? _____ Hz
6. What is the period, in milliseconds, of the signal across the load? _____ ms
7. What is the average voltage across the load? _____ V_{DC} (Notice the unit? Average voltage always corresponds to DC)

8. What is the RMS voltage across the load? _____ V_{RMS}
9. What power will the load resistor dissipate as heat? _____ mW

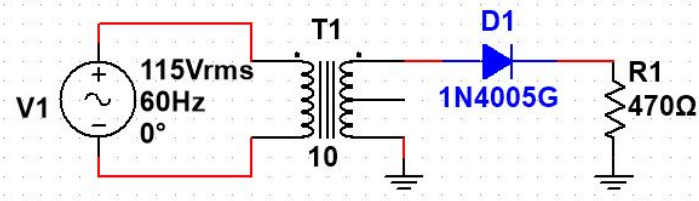
Notice one very important thing about units: all the voltages represent the same signal, but the numbers are very different. You MUST always include the appropriate subscript to indicate which measurement unit you mean -- V isn't going to cut it when working with AC signals! To help, though, the only subscripts you will use will be

- V_p
- $V_{p\text{-}p}$
- V_{DC}
- V_{RMS}

"V" by itself will refer to an instantaneous voltage, or, in some cases, to V_{RMS}.

Notice another thing: The numbers for V_{ave} and V_{RMS} are quite different. That means that our signal is not "pure DC", which is pretty obvious from the graph.

Here's a worked example for you to review on your own time.

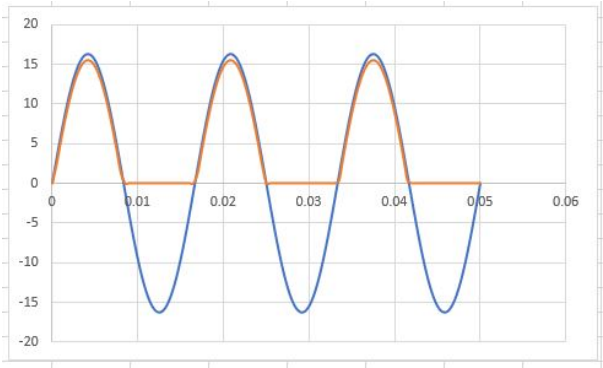


- Always start by converting the input signal to a peak voltage: $V_1 = 115 \cdot \sqrt{2}$ = 162.6 V_p

Take a look at the transformer: its turns ratio is 10:1; its secondary is centre-tapped, but we're using the entire secondary (if we were only using half of the secondary, the voltage would be half what the turns ratio predicts, but that's not an issue here -- just watch out for it!).

- So, the signal presented to the diode will be V1/10 = 16.2 V_p.
- From the diode's orientation, we see that it will conduct when the transformer signal is positive. So, for the positive half-cycle, we can replace the diode with a small voltage source, therefore the voltage presented to the load resistor will be the transformer voltage minus a diode drop. We'll assume 0.7 V, since we're not given any other information, so the positive peak voltage will be +15.6 V_p.

When the transformer signal is negative, the diode will be reverse biased, so we can replace it with an open switch. With no current possible through the load resistor, the voltage across it will be zero. This means we have a half-wave rectifier. The following plot compares the transformer output signal to the diode output signal:

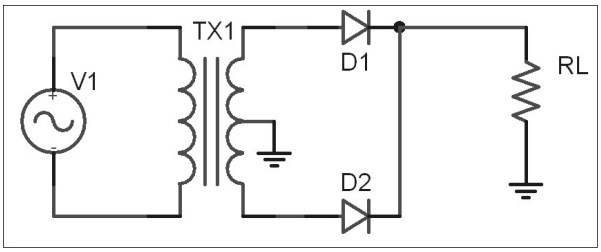


- The frequency of the rectified signal is the same as the input at 60 Hz, so the period of this signal is 1/(60 Hz) = 16.7 ms.
- The average voltage, since this is a halfwave signal, can be predicted using $V=V_p/\pi$ = +15.6 V_p/π = +4.95 V_{DC}
- The power-related voltage, again for a halfwave signal, can be predicted using $V=|V_p/2|$ = 15.6 $V_p/2$ = 7.78 V_{RMS}
- The power dissipated by the resistor can be determined from the RMS voltage: $P=V_{RMS}^2/R$ = (7.78 V_{RMS})^2/470 Ω = 129 mW

Question 3: (1 point)

Full Wave Rectifier -- Centre Tapped Transformer

The following circuit "rectifies" both the positive half-wave and the negative half-wave.



For this circuit, you need to remember that only half of the secondary's voltage appears at the output at any given time -- the other half of the secondary can't conduct when its diode is reverse-biased.

Your instructor will likely go through this diagram, explaining why it works as it does. In essence, it's just two half-wave rectifiers linked to the same load.

The average voltage is twice what we would expect from just one half-wave per original cycle:

$$V_{ave} = \frac{2\ V_p}{\pi}$$

The RMS voltage is back to what we would expect for a sine wave -- flipping the bottom half up has effectively done the same thing as squaring all the values in the sine wave calculation before taking the square root in the RMS calculation:

$$V_{RMS} = \frac{V_p}{\sqrt{2}}$$

The frequency of the resulting signal is now double the source signal's frequency, because there are two identical half-waves one after the other during one input cycle.

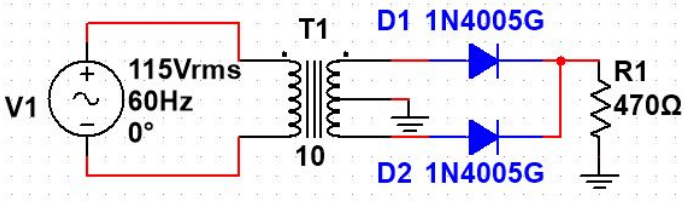
$$f_{FW} = 2\ f_{Source}$$

Question: Assume the same signal voltage, 120 V_{AC}, same transformer turns ratio, 8:1, same diode barrier potential, 0.7 V, and same resistor as before, 220 Ω.

1. What is the peak voltage at the output of the secondary of the transformer, given that the ground reference is in the middle of the secondary? _____ V_p
2. Using the practical diode model, what is the peak voltage across the load, referenced to ground? _____ V_p
3. What is the frequency of the signal across the load? _____ Hz
4. What is the period, in milliseconds, of the signal across the load? _____ ms
5. What is the average voltage across the load resistor? _____ V_{DC}
6. What is the RMS voltage across the load resistor? _____ V_{RMS}
7. What power will be dissipated by the load resistor? _____ mW

Unfortunately, because we used the same turns ratio in the transformer but split it in the middle, the resulting power is significantly lower. However, notice that the average and RMS voltages are much closer to each other, which indicates that this is closer to true DC, which is one of our goals.

Here's a worked example that carries on using the same components as in the previous worked example.

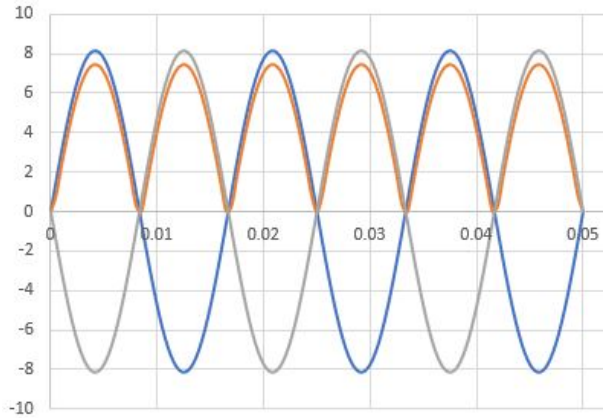


- The power source is 162.6 V_p
- The transformer output voltage, from top to bottom, is 16.3 V_p; however, with the centre-tap grounded, that means that, when the top of the transformer is positive, the bottom of the transformer will be equally negative; so the signals at the two terminals of the transformer will be two half-size sine waves, 180^o out of phase; therefore, the peak voltage presented to the diodes is 8.13 V_p.
- From the orientation of the diodes, current is supplied to the load resistor when the transformer voltage is positive; both diodes act as half-wave rectifiers, but with a 180^o phase shift between them, the result is a full-wave positive rectified signal with a peak

voltage down one diode drop (on each half wave) from the peak voltage; therefore, the peak voltage presented to the load resistor is 8.13 V_p - 0.7 V = +7.43 V_p.

- Since the second half of the original signal is now a positive half-wave, the period of the signal is half the original, or 8.33 ms; the frequency is therefore 1/T = 120 Hz.

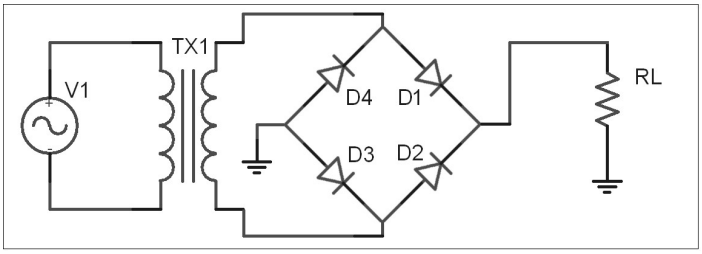
The resulting signal, compared to the signals at the two ends of the transformer referenced to ground, looks like this:



- The average voltage for a full-wave rectified signal can be predicted using $2V_p/\pi$ or 2*7.43 V_p/π = +4.73 V_{DC}
- The power-related voltage for a full-wave rectified signal is the same as for a sine wave, or $V_p/\sqrt{2}$ = 5.26 V_{RMS}
- The power dissipated by the resistor, based on the RMS voltage using $P=V_{RMS}^2/R$ will be 58.8 mW

Question 4: (1 point)

The most commonly used rectifier configuration requires four diodes in a "bridge" configuration, as shown below.



This configuration does not require a centre-tapped transformer (these are difficult to source). It also provides almost double the peak voltage seen with the centre-tapped transformer rectifier for the same turns ratio, and therefore provides almost four times the power.

Your instructor will explain how this circuit works. Mathematically, the calculations for average voltage, RMS voltage, and frequency are the same as for the centre-tapped transformer rectifier. However, the peak voltage across the load will be ***two*** diode drops down from the transformer secondary voltage.

Question: Using the same conditions and components as before -- 120 V_{AC} at 60 Hz, 8:1 transformer, barrier potential of 0.7 V, 220 Ω load resistor -- determine the following:

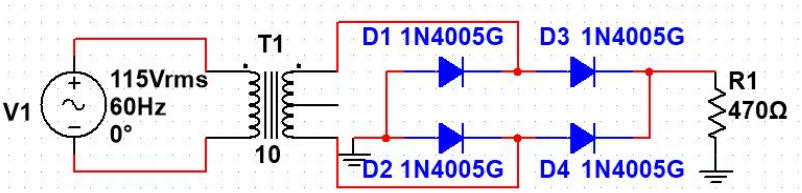
1. What is the peak voltage across the load resistor? _____ V_p
2. What is the frequency of the signal at the load? _____ Hz
3. What is the period of the signal at the load, in milliseconds? _____ ms
4. What is the average voltage across the load? _____ V_{DC}
5. What is the RMS voltage across the load? _____ V_{RMS}
6. What power will be dissipated as heat by the load resistor? _____ mW

As you can see, the power output for the same set of conditions is much higher for this rectifier than for either of the other configurations.

Also, the values for the Average and RMS voltages are much more similar than they were for the Half-Wave Rectifier, indicating that the output is closer to being true DC.

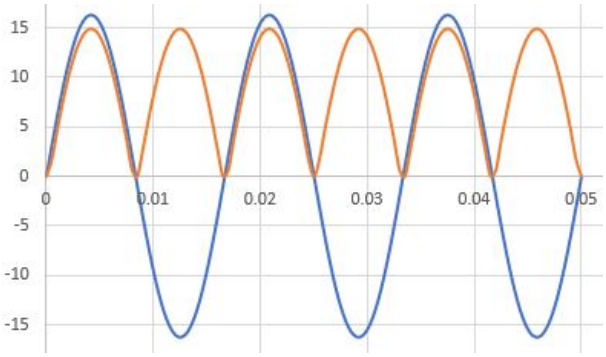
Worked Example

The following is a continuation of the examples used previously, with all components the same except the rectifier circuit.



- Since the current path always includes two diodes (D3 and D2 for the positive half-cycle, and D4 and D1 for the negative half-cycle), and since the orientation of the diodes is such that the current always flows through the resistor to ground, the peak voltage across the load is now the full secondary peak reduced by two diode drops: $V_R = (115 \cdot \sqrt{2}/10 - 2 \cdot 0.7 = 14.9\ V_p$.
- With the second half-cycle inverted, the result is a period of half a full cycle, or 8.33 ms; the frequency of the signal across the load is therefore 120 Hz.

The resulting signal, as compared to the signal across the secondary of the transformer, looks like this:



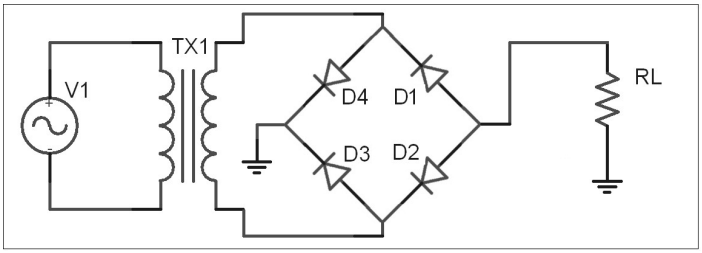
- The average voltage for a full-wave rectified signal can be predicted using $2*V_p/\pi$ = +9.46 V_{DC}
- The power-related voltage for a full-wave rectified signal can be predicted using $V_p/\sqrt{2}$ = 10.5 V_{RMS}
- The power dissipated by the resistor, from V_{RMS}^2/R = 235 mW

Question 5: (1 point)

Since the orientation of a diode determines whether it will conduct when the source is positive or when the source is negative, we can simply turn the diode or diodes around in a rectifier circuit if we want a negative voltage instead of a positive voltage. All the numeric values will have the same magnitude, but the Peak Voltage and the Average Voltage will be negative.

Be aware that the RMS voltage is ***never*** negative -- any negative signs are eliminated in the "squaring" portion of RMS. This makes sense, because power consumption by a load is never negative, and the purpose of determining the RMS voltage is for power calculations.

Question: Consider the Bridge Rectifier below. Use the same components and conditions as before: 120 V_{AC} at 60 Hz, 8:1 transformer, 0.7 V barrier potential, 220 Ω load resistor.



1. What is the peak voltage seen at the load? Include both the sign and the magnitude. _____ V_p
2. What is the frequency of the signal at the load? _____ Hz
3. What is the average voltage seen at the load? _____ V_{DC}
4. What is the RMS voltage at the load? _____ V_{RMS}

The other rectifier circuits can also be made negative following the same basic steps.

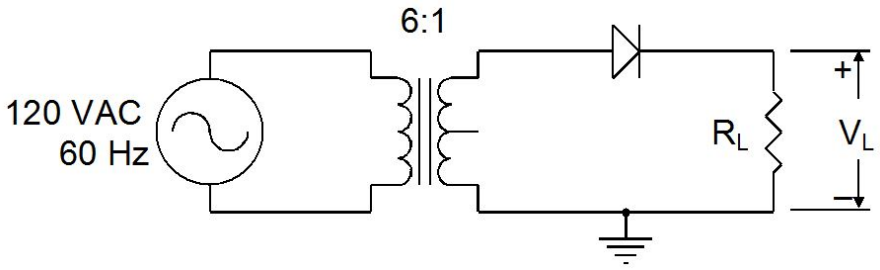
Online Homework System

Assignment Worksheet
5/31/21 - 9:16:52 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA02 Rectifiers Quiz

Question 1: (6 points)

For the circuit shown, determine the peak voltage across the load resistor, VL, if the forward diode drop is 0.7 V. Indicate the correct polarity of this voltage and the correct unit of measure.



_____ _____

Determine the root mean squared voltage across the load resistor, VL.

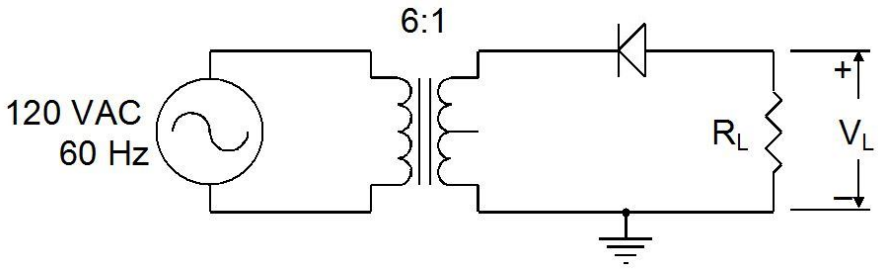
_____ _____

Determine the average voltage across the load resistor, VL.

_____ _____

Question 2: (6 points)

Answer the questions below for the circuit shown, if the forward diode drop is 0.7 V. Indicate the correct polarity and the correct unit of measure.



Determine the peak voltage across the load resistor, VL.

_____ _____

Determine the root mean squared voltage across the load resistor, VL.

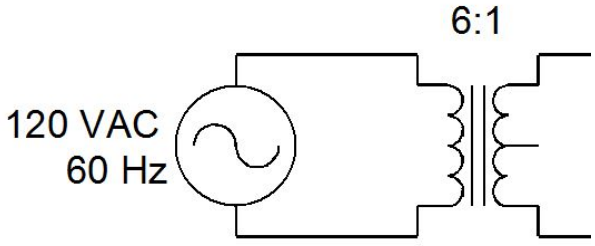
_____ _____

Determine the average voltage across the load resistor, VL.

_____ _____

Question 3: (2 points)

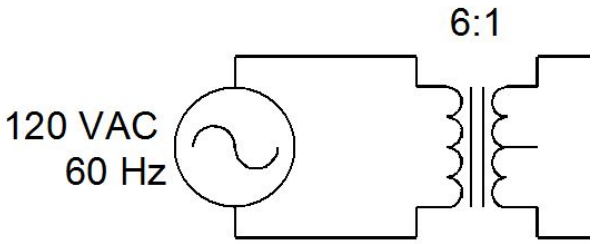
If the following AC source and transformer were to be used in a positive-output centre-tapped rectifier circuit using two diodes with forward voltages of 0.7 V, what would the peak voltage be across a load resistor connected to the two diode cathodes? Include the correct units of measure in your answer.



_____ _____

Question 4: (2 points)

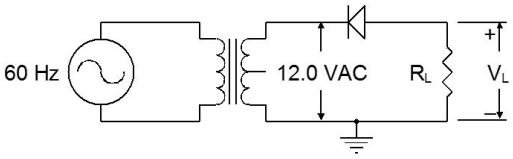
If the following AC source and transformer were to be used in a positive-output bridge rectifier circuit using four diodes with forward voltages of 0.7 V, what would the peak voltage be across a load resistor connected to the two diode cathodes? Include the correct units of measure in your answer.

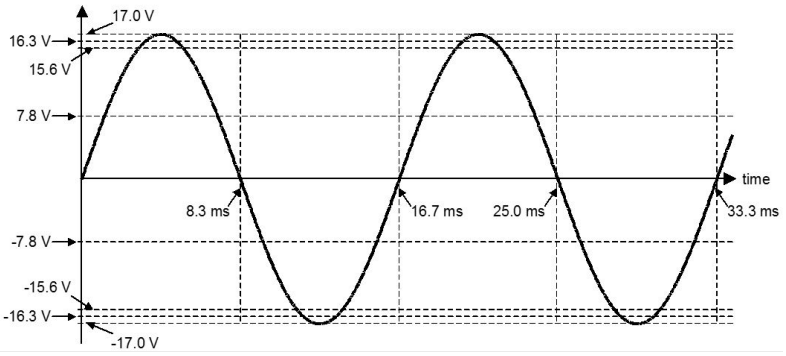


_____ _____

Question 5: (1 point)

The sine wave in the following picture represents the voltage across the secondary of the transformer. Given the circuit as shown and a diode voltage drop of 0.7 V, which of the voltages shown represents the peak output expected for this circuit?





(a) +17.0 V

(b) +16.3 V

(c) +15.6 V

(d) +7.8 V

(e) -7.8 V

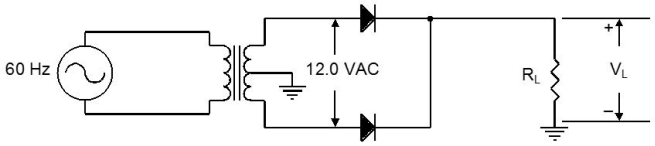
(f) -15.6 V

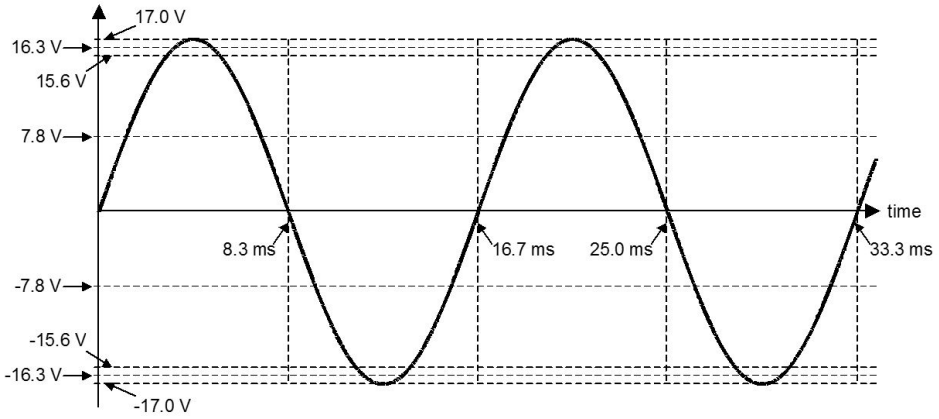
(g) -16.3 V

(h) -17.0 V

Question 6: (1 point)

The sine wave in the following picture represents the voltage across the secondary of the transformer. Given the circuit as shown and a diode voltage drop of 0.7 V, which of the voltages shown represents the peak output expected for this circuit?





(a) +17.0 V

(b) +16.3 V

(c) +15.6 V

(d) +7.8 V

(e) -7.8 V

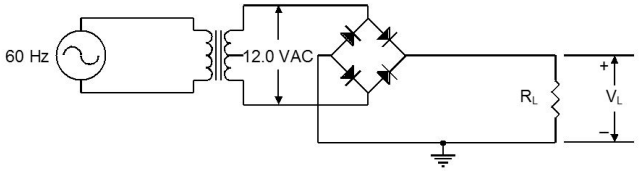
(f) -15.6 V

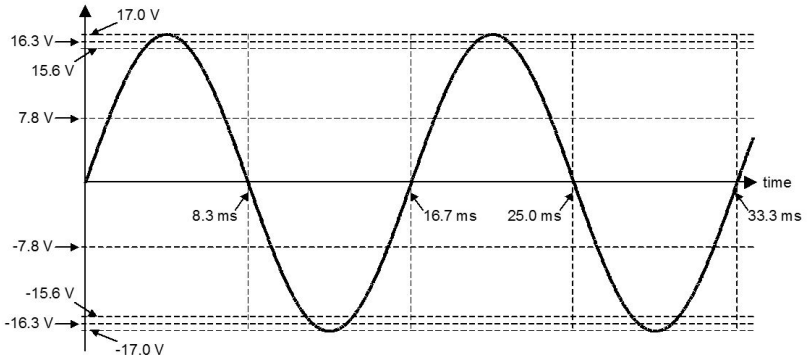
(g) -16.3 V

(h) -17.0 V

Question 7: (1 point)

The sine wave in the following picture represents the voltage across the secondary of the transformer. Given the circuit as shown and a diode voltage drop of 0.7 V, which of the voltages shown represents the peak output expected for this circuit?





(a) +17.0 V

(b) +16.3 V

(c) +15.6 V

(d) +7.8 V

(e) -7.8 V

(f) -15.6 V

(g) -16.3 V

(h) -17.0 V

Question 8: (1 point)

If the line supply frequency is 60 Hz, what is the expected frequency of a full-wave rectified output signal? _____ Hz

Online Homework System

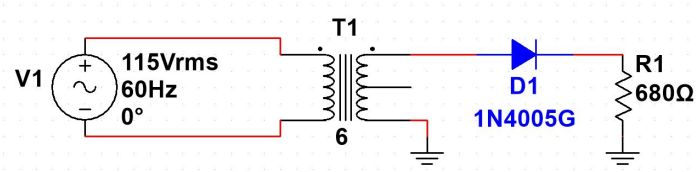
Assignment Worksheet
12/7/22 - 7:08:10 PM MST

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Lab02 Rectifier Circuits

Question 1: (10 points)

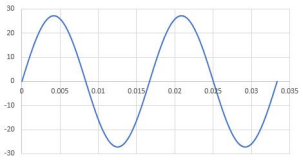
NOTE: Once you complete your Pre-Lab Assignment and move on to the Lab Activity, you will not be able to re-open the Pre-Lab for further editing! Do not go to the "NEXT" page until you have completed this one!

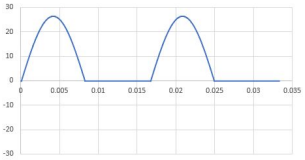
Use the following schematic to answer the questions below.

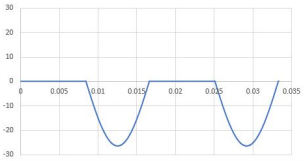


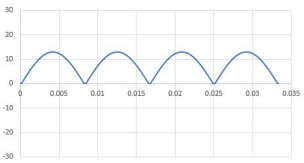
Assuming the transformer has a turns ratio of 6:1 and the diodes you will be using have a barrier potential of 0.7 V, determine the following:

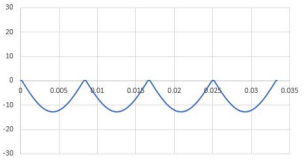
1. Peak voltage at the load (R1) _____ _____
2. Average voltage at the load _____ _____
3. RMS voltage at the load _____ _____
4. Frequency of signal at the load _____ _____
5. Period of signal at the load _____ ms
6. Select the waveform that best represents the signal at the load:

(a)


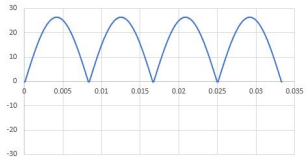
(b)


(c)


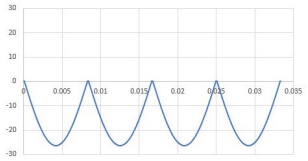
(d)


(e)


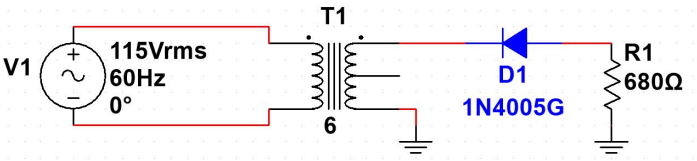
(f)



(g)



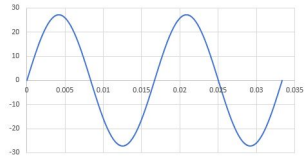
Use the following schematic to answer the questions below:



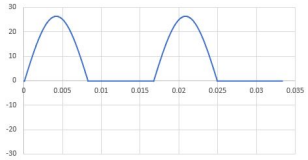
Assuming the transformer has a turns ratio of 6:1 and the diodes you will be using have a barrier potential of 0.7 V, determine the following:

1. Peak voltage at the load (R1) _____ _____
2. Average voltage at the load _____ _____
3. RMS voltage at the load _____ _____
4. Frequency of signal at the load _____ _____
5. Period of signal at the load _____ ms
6. Select the waveform that best represents the signal at the load:

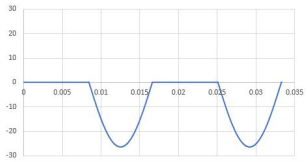
(a)



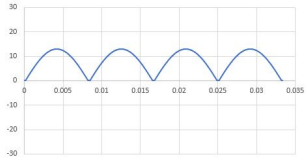
(b)



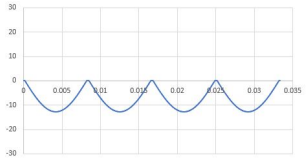
(c)



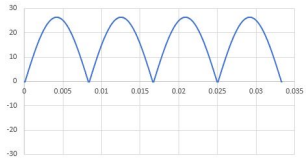
(d)



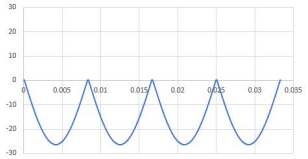
(e)



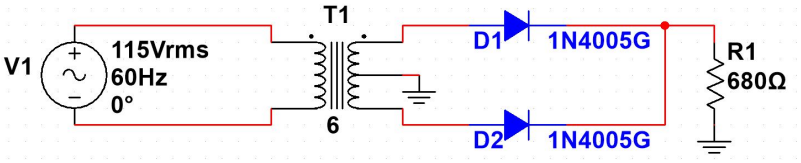
(f)



(g)



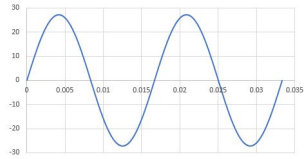
Use the schematic circuit below to answer the questions that follow.



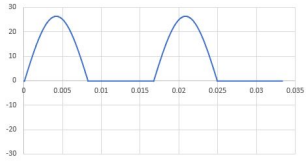
Assuming the transformer has a turns ratio of 6:1 for the entire secondary and the diodes you will be using have a barrier potential of 0.7 V, determine the following:

1. Peak voltage at the load (R1) _____ _____
2. Average voltage at the load _____ _____
3. RMS voltage at the load _____ _____
4. Frequency of signal at the load _____ _____
5. Period of signal at the load _____ ms
6. Select the waveform that best represents the signal at the load:

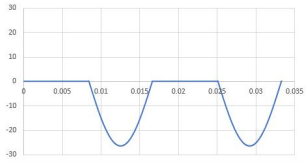
(a)



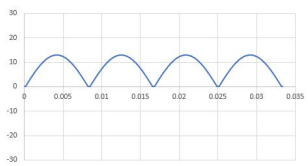
(b)



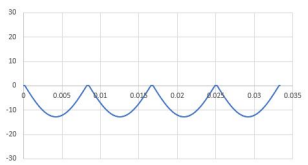
(c)



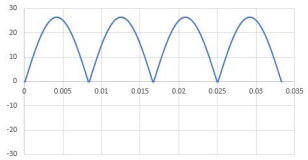
(d)



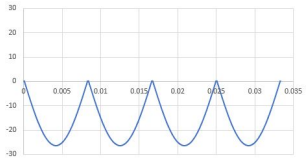
(e)



(f)



(g)



You have now finished the Pre-Lab.

You may wish to take a screenshot of your results to help you with the Lab Activity.

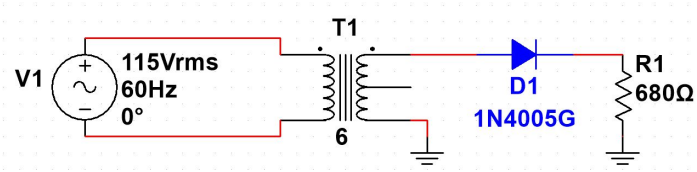
Move on to the Lab Activities. Do not click "submit" yet!

Question 2: (10 points)

In the classroom, you will be provided with a 6:1 centre-tapped transformer to do this lab and the next.

Build each of the circuits below, and test them as indicated.

Positive Half-Wave Rectifier



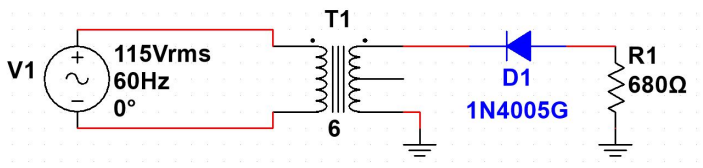
- Use oscilloscope Channel 1 to monitor the input signal at the anode of the diode.
- Use oscilloscope Channel 2 to monitor the output signal across the load resistor, R1.
- Maximize the display on the oscilloscope: signals should fill the screen vertically and show three to eight cycles.
-

1. Ask your instructor to grade your circuit setup and oscilloscope settings out of five marks. _____

Make the following measurements for the signal across the load resistor, using the measurement menu of the oscilloscope:

2. Frequency = _____ Hz
3. Period = _____ ms
4. Positive peak voltage = _____ _____
5. Average voltage = _____ _____
6. RMS voltage = _____ _____

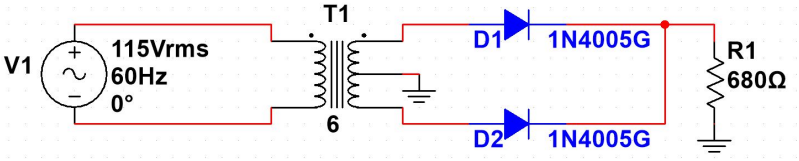
Negative Half-Wave Rectifier



Make the following measurements for the signal across the load resistor, R1, using the oscilloscope :

8. Frequency = _____ Hz
9. Period = _____ ms
10. Negative peak voltage = _____ _____
11. Average voltage = _____ _____
12. RMS voltage = _____ _____

Positive Full-Wave Centre-Tapped Transformer Rectifier



13. Use oscilloscope Channel 1 to monitor the input signal that appears at the anode of D1.
14. Use oscilloscope Channel 2 to monitor the output signal across the load resistor, R1.
15. Once you are satisfied that your circuit is working properly and that the oscilloscope display is maximized, ask your instructor to give you a grade out of three marks. _____

Make the following measurements for the signal across the load, R1, using the oscilloscope:

14. Frequency = _____ Hz
15. Period = _____ ms
16. Positive peak voltage = _____ _____
17. Average voltage = _____ _____
18. RMS voltage = _____ _____

Negative Full-Wave Centre-Tapped Transformer Rectifier

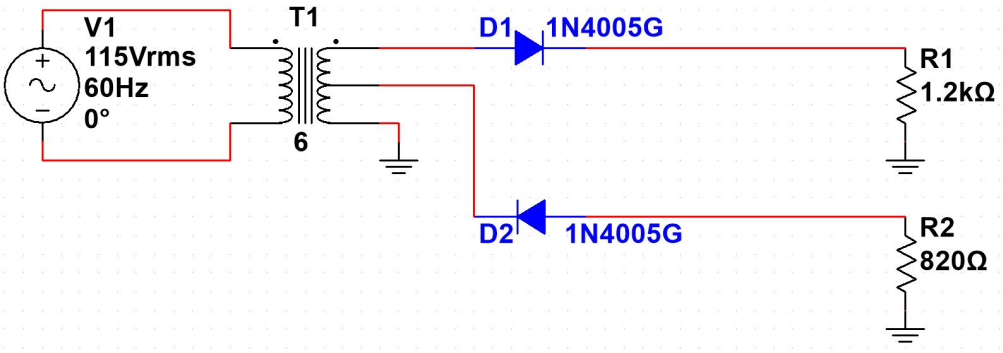
Reverse both the diodes in your previous circuit to make a negative full-wave centre-tapped transformer rectifier circuit.

Make the following measurements for the signal across the load resistor, R1, using the oscilloscope:

19. Frequency = _____ Hz
20. Period = _____ ms
21. Negative peak voltage = _____ _____
22. Average voltage = _____ _____
23. RMS voltage = _____ _____

Simulation: Dual Supply Rectifier

Using Multisim, build and test the following circuit.



Notes:

- V1 is "AC_POWER" -- make sure you change its characteristics to match the schematic
- T1 is "TS_VIRTUAL" -- change its turns ratio to "6" for 6:1

Use a Tektronix four-channel oscilloscope to view the signals at the following points:

Channel 1 -- voltage at the top of the transformer (i.e. anode of D1)

Channel 2 -- voltage across R1 (i.e. cathode of D1)

Channel 3 -- voltage at the centre-tap of T1 (i.e. cathode of D2)

Channel 4 -- voltage across R2 (i.e. anode of D2)

Observe Channels 1 and 2 with the other channels turned off, and verify for yourself that what you are seeing fits what the diode model would predict.

Measure and record the following, using the oscilloscope's Measurement menu:

24. For the top of the transformer: peak voltage = _____ V_p
25. Across R1: peak voltage = _____ V_p and average voltage = _____ V_{DC}

Observe Channels 3 and 4 with the other channels turned off, and verify for yourself that what you are seeing fits what the diode model would predict.

Measure and record the following, using the oscilloscope's Measurement menu:

26. For the centre tap of the transformer: peak voltage = _____ V_p
27. Across R2 (make sure you include the polarity): peak voltage = _____ V_p and average voltage = _____ V_{DC}

Set up the oscilloscope as follows:

- Maximize the signal for Channel 1
- Turn on all four channels
- Set the rest of the channels to the same settings as what you have for Channel 1, including the zero volt markers for all channels and the vertical scale
- Display about three cycles of the signal

28. For a grade out of four marks, take a screen-shot and upload it here. If your instructor grades your work in class, upload a text file with the assigned grade instead. Document Upload (Direct)

You have now completed this Lab. Click "Submit" to send out your work for grading.

Online Homework System

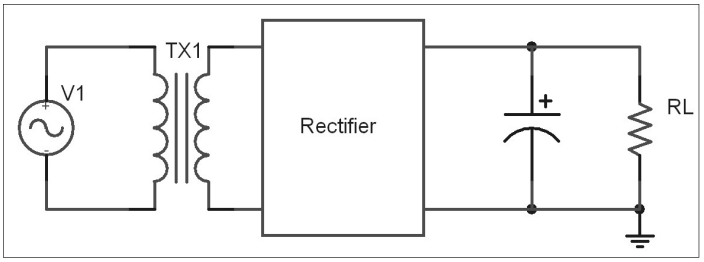
Assignment Worksheet
1/16/23 - 12:34:47 PM MST

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Filtering and Regulation

Question 1: (1 point)

Power Supply Filtering

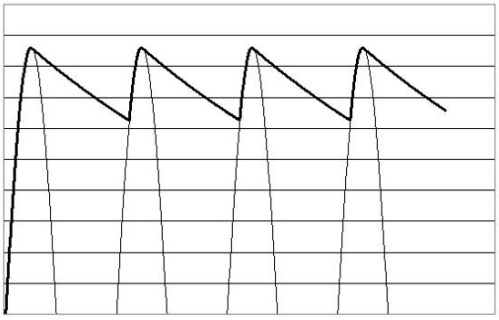
In a previous course, you were introduced to the concept of filtering -- removing unwanted frequency components from a compound signal. With DC power supplies, we want the DC component, which has a frequency of zero. Therefore, we want to create a Low Pass Filter to remove all components from our rectified signal other than zero, or DC. We could use a series resistor and a capacitor to ground, but it turns out that the following configuration of a Low Pass Filter is much more effective for our circuit, because of the characteristics of the diode.



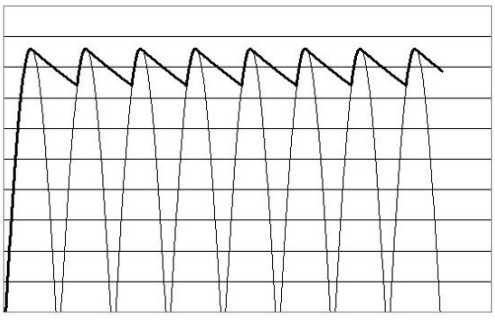
This arrangement uses the circuit load, R_L, as the resistor in the filter, so no power is dissipated to anything but the load.

However, the even greater improvement over a standard series LPF is the way the capacitor is charged by the diode or diodes in the rectifier.

The capacitor can be quickly charged through the very low internal resistance of the forward biased diode or diodes, raising the capacitor voltage to very nearly the peak voltage of the rectifier. However, when the rectifier voltage would normally drop, the diodes become reverse biased, and no current drains back. This means that the only current drain from the capacitor is through the load, which has a much higher resistance than the forward biased diode or diodes had, so the voltage does not drop very quickly. We achieve the following result for a half-wave rectifier:



For a full-wave rectifier, the result is even better (no surprise, given that the frequency is double, and therefore further from zero):



In each of these, the rising side practically follows the rectified input up; then, the capacitor begins its slow discharge through the load, only to be overtaken by the next rising side.

Mathematically, this is a difficult signal to analyze, as the point at which it switches from a falling exponential curve to a rising sinusoid changes with the rate of decay of the exponential. An attempt to solve for this produces a situation in which the time cannot be isolated -- it's always either in a sine expression or in an exponent. Consequently, the best we can do to predict the characteristics of these signals is to form an approximation.

Ripple

The tops of these waveforms look like waves on water, so their amplitude is referred to as "Ripple Voltage". This is typically measured in peak-to-peak volts.

The ripple amplitude is affected by the following three variables:

1. Discharge time, which is the period of the rectifier frequency. The shorter the period, the less ripple appears.
2. Size of the capacitor. A large capacitor stores more charge, so the bigger the capacitor, the less ripple appears.
3. The load current. The bigger the current, the more charge is drained, so the smaller the load resistance (i.e.) the more current, the more ripple appears.

Putting these together, we arrive at the following relationship:

$V_r = \frac{I_L T}{C}$, in $V_{p\text{-}p}$

The problem that arises is that the current is dependent on the voltage, which is changing in a way that can't be mathematically isolated.

$I_L = \frac{V_L}{R_L}$, but V_L can't be definitely determined.

For our approximation, we assume the worst case -- that V_L = the peak voltage.

Therefore,

$V_r \sim \frac{V_p T}{R_L C}$

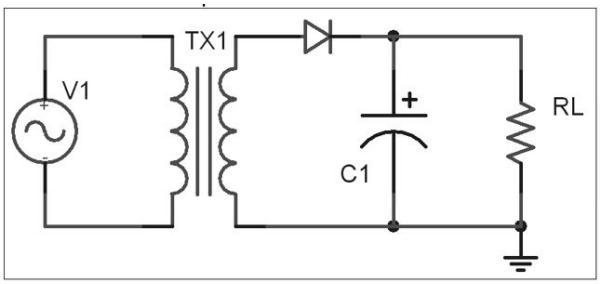
Now comes the true significance of what happens as a result of the quick charging through the diode: The DC voltage is much higher than it was for the unfiltered signal! We approximate the DC component of a filtered rectifier as follows:

$V_{ave} = V_p - \frac{V_r}{2}$

Of course, this becomes a worst case approximation, because the ripple is a worst case approximation. In reality, the ripple will be less, and the average voltage will be higher than these calculations predict.

By the way, we will encounter circuits where the Load Current, I_L, is known, in which case we don't need to do the approximation and can just use the first formula to determine the ripple voltage.

Question: Use the schematic below to answer the questions that follow. V_1 is 120 VAC at 60 Hz, the transformer turns ratio is 10:1, the diode has a forward drop of 0.7 V, the capacitor is 220 μF, and the load resistance is 330 Ω.



1. What is the peak voltage across the load, referenced to ground? _____ V_p
2. What is the worst case analysis of the ripple voltage? _____ $V_{p\text{-}p}$
3. What is the worst case estimate of the average voltage? _____ V_{DC}

If you aren't satisfied with the "approximation" aspect of this, you could now use the average voltage instead of the peak voltage to do a new calculation, but you should discover that there is no appreciable difference in your new answer, because the ripple voltage is fairly small.

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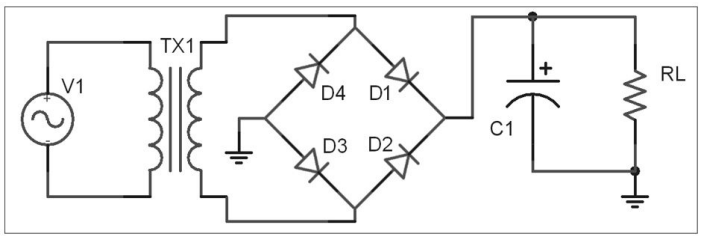
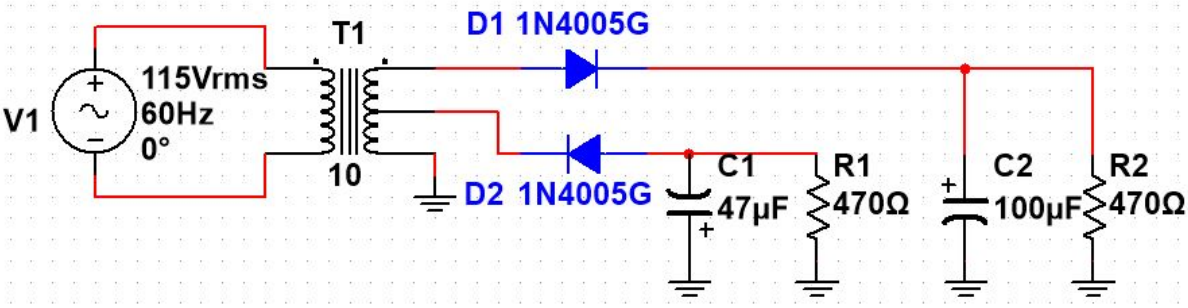


1. What is the peak voltage across the load, referenced to ground? _____ V_p
2. What is the worst case analysis of the ripple voltage? _____ $V_{p\text{-}p}$
3. What is the worst case estimate of the average voltage? _____ V_{DC}

From these two examples, it should be apparent that the full-wave rectifier circuit produces a much better filtered output than the half-wave, part of the reason this circuit is the most common one used in inexpensive linear power adapters.

Here's a worked example that will reinforce what you've already learned, while exposing you to some useful variations to the types of circuits you've been investigating.



At first glance, you may be tempted to say this is some kind of full-wave rectfier, since it has two diodes. However, upon closer inspection, it turns out it's two independent half-wave rectifiers: the diodes are connected to two separate load resistors (and their associated filter capacitors). In addition, the diodes are driven from different points on the secondary of the transformer, so the output voltages will be different in magnitude as well as polarity.

We'll analyze the two parts separately.

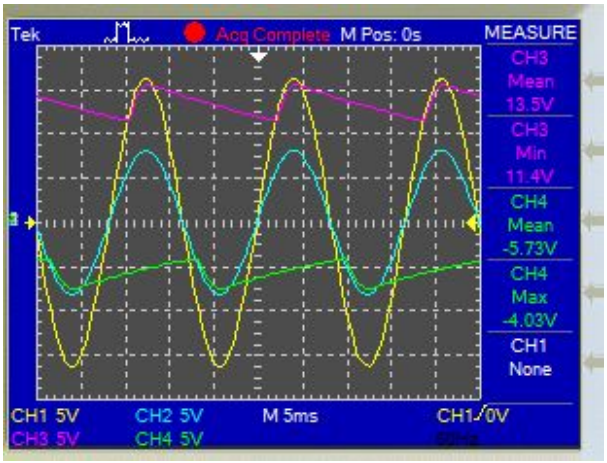
D1 Circuit

- Current flows through D1 during the positive half-cycle of the transformer signal, therefore this is a positive supply.
- The entire secondary signal appears across this circuit, so the peak voltage across the load would be $\frac{115 \cdot \sqrt{2}}{10} - 0.7 = +15.6\ V_p$
- Since only the positive half-cycle forward-biases D1, this is a half-wave rectifier with a frequency of 60 Hz and a period of 16.7 ms.
- The worst-case prediction for the ripple voltage would be $V_r = \frac{V_p \cdot T}{R_L \cdot C} = \frac{15.6 \cdot 0.01667}{470 \cdot 100\ x10^{-6}} = 5.52\ V_{p-p}$
- The worst-case prediction for the average voltage would be $V_{ave} = V_p - \frac{V_r}{2} = +15.6 - \frac{5.52}{2} = +12.8\ V_{DC}$
- The minimum voltage expected would be $V_{\min} = V_p - V_r = +15.6 - 5.52 = +10.1\ V$

D2 Circuit

- Current flows through D2 during the negative half-cycle of the transformer signal, therefore this is a negative supply.
- The proper orientation for the electrolytic capacitor, C1, is positive to ground, negative to the more negative voltage as shown.
- Only half of the secondary signal appears across this circuit, so the peak voltage across the load would be $-\left(\frac{(115 \cdot \sqrt{2})}{10 \cdot 2} - 0.7\right) = -7.43\ V_p$
- Since only the negative half-cycle forward-biases D2, this is a half-wave rectifier with a requency of 60 Hz and a period of 16.7 ms.
- The worst-case prediction for the ripple voltage would be $V_r = \frac{7.43 \cdot 0.0167}{470 \cdot 47\ x10^{-6}} = 5.61\ V_{p-p}$
- The worst-case prediction for the average voltage would be $-\left(7.43 - \frac{5.61}{2}\right) = -4.63\ V_{DC}$
- The smallest negative voltage expected would be $-(7.43 - 5.61) = -1.82\ V$

The actual results for this circuit as simulated by Multisim are shown below, and, as expected, are better than the "worst case" predictions:



The ripple for the positive supply is only 4.2 $V_{p\text{-}p}$ instead of 5.52 $V_{p\text{-}p}$, the average is +13.5 V_{DC}, and the minimum voltage is +11.4 V.

The ripple for the negative supply is only 3.4 $V_{p\text{-}p}$ instead of 5.61 $V_{p\text{-}p}$, the average is -5.73 V_{DC}, and the minimum voltage is -4.03 V -- quite an improvement over the worst-case predictions. In fact, this part of the circuit would be suitable for a -3.3 VDC regulated supply, something our worst-case predictions would have ruled out due to the voltage dropping below -3.3 V.

In reality, it would be a good idea to increase the size of the filter capacitor for the second circuit. If we used a 100 μF capacitor instead of the 47 μF capacitor shown, the worst-case prediction for the minimum voltage would be -4.80 V, which is a huge improvement over the circuit as shown. We've already got a 100 μF capacitor in the parts list, so it makes good sense to use one here, too. (For practice, you might want to verify the minimum voltage value presented here.)

Question 2: (1 point)

Voltage Regulation

We've come a long way from an AC circuit with no DC to a DC signal with some ripple on it, which we can control to some extent through our choice of rectifying circuit and filtering capacitor.

However, our circuit's DC output is still dependent on the peak voltage of the input signal, for which we will need what's called "Line Regulation" -- making the output DC less dependent on changes in the Line voltage. It's also dependent on the current drawn through the attached load, for which we will need what's called "Load Regulation" -- making the output DC less dependent on changes in the load resistance.

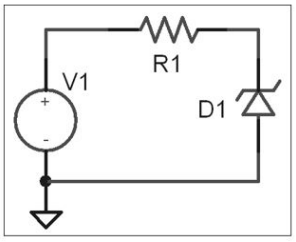
Regulation refers simply to the attempt to maintain a constant output regardless of changes in the source or the load.

Most regulator circuits employ Zener Diodes in one way or another to help them maintain a constant output voltage.

Zener Diode

The Zener Diode is designed to have a predictable reverse breakdown voltage, and is therefore typically installed in reverse bias in a circuit.

Using Multisim, build the following circuit, and answer the questions that follow. use a 3.3 kΩ resistor and a 1N4738A Zener diode. Use a "DC_INTERACTIVE_VOLTAGE" for V_1, as you will be changing its value. Place an "A/V" probe on the node between the resistor and the diode.



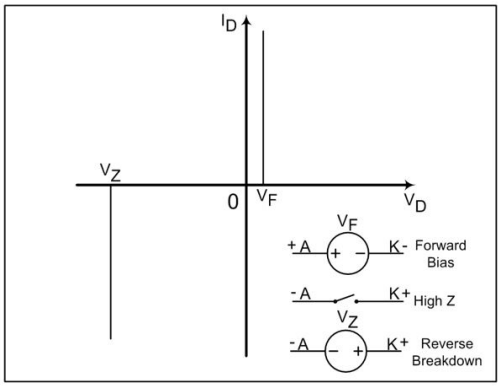
Set the input voltage to the values shown in the table, and record the voltages and currents observed at the cathode of the diode.

V_1, V	V_D, V	I, mA
-0.35	_____	_____
-3.0	_____	_____
5.0	_____	_____
15.0	_____	_____

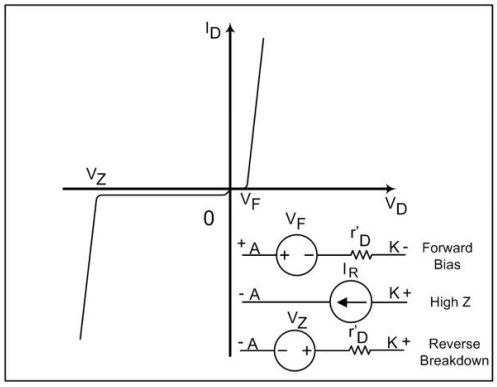
Notice that the diode establishes constant voltages in both the forward and reverse biasing configurations.

Zener Diode Models

The Practical Zener Diode Model says that once either the forward or reverse breakdown voltages have been exceeded, the Zener Diode becomes a constant voltage source regardless of other conditions in the circuit. In between those two voltages, it behaves as an open switch.



The Complete Zener Diode Model includes a fairly significant difference -- that when the diode conducts in either direction, its internal resistance will produce a slight change in voltage, dependent upon the current.



Unfortunately, since power supplies tend to be high current devices, this change in voltage is often significant when Zeners are employed.

Question: Go to the datasheet link below and locate the 1N4733A Zener diode to answer the questions that follow.

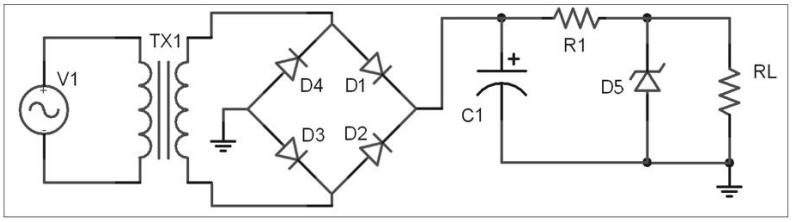
Zener Diode Datasheet (https://datasheetspdf.com/pdf-file/134169/DcComponents/1N4735A/1)

1. What is the reverse breakdown voltage for the 1N4733A (Vz) _____ V
2. What current is this reverse breakdown voltage measured at? _____ mA
3. What is the internal resistance of this Zener diode (Z_{ZT})? _____ Ω
4. If the current through the Zener is 250 mA, what is the Zener diode reverse voltage, using the Complete Model? _____ V

Clearly, this Zener diode isn't capable of holding the "regulated" voltage at its reverse breakdown value when a lot of current is drawn through it.

Here's a typical Zener diode-regulated circuit. Since you're not likely to use a circuit like this, we won't spend too much time on the design of it. Instead, we'll work through it as an instructional exercise, from which you should learn how a Zener regulator works and what its limitations are, while reinforcing some of the electrical and electronic concepts you've learned so far.

For this circuit, V1 is 115 VAC, the transformer turns ratio is 16:1, the rectifier diode drops are 0.7 V, C1 is 470 μF, R1 is 39 Ω, D5 is a 1N4733A, and RL is never smaller than 100 Ω.



As usual, we need to work our way through the transformer and rectifier:

- First, determine the peak voltage at the output of the rectifier:
  - start with converting the AC supply from RMS to peak: $V_1 = 115\ V_{RMS} \cdot \sqrt{2}$=162.6 V_p
  - next, determine the voltage at the secondary using the turns ratio: 162.6 V_p/16 = 10.2 V_p
  - finally, subtract two diode voltage drops from the positive peak, since there are always two diodes conducting at at time: V_{rect} = 10.2 V_p - 2(0.7 V) = +8.76 V_p
- Since the load resistor, R_L is in parallel with the Zener diode, they have the same voltage across them; so when the Zener is conducting, the voltage across $R_L = V_Z$. Using the Practical model of the Zener, we conclude that V_{RL} = 5.1 V_{DC}.
- The current through the load, using this voltage, can be predicted using Ohm's Law. The worst case current will be determined using the minimum value of the load resistance. $I_L = V_{RL}/R_L$ = 5.1 V_{DC}/100 Ω = 51 mA_{DC}.
- Let's work back through the circuit. The voltage drop across R_1 (a current-limiting resistor that protects the Zener diode) will be, at the peak of the rectifier cycle, 8.76 V_p - 5.1 V_{DC} = 3.66 V_p
- Using the peak voltage across the current-limiting resistor, we can determine the peak current drawn from the rectifier: $I_T = \Delta V_{R1}/R_1$ = 3.66 V_p/39 Ω = 94.0 mA_p. (You may get a slightly different answer if you use the rounded values above rather than keeping the values on your calculator.)
- Any current in excess of the load current must go through the Zener diode, since there are two parallel current paths. So, the current through the Zener diode is $I_Z = I_T - I_L$ = 94.0 mA_p - 51 mA_{DC} = 43.0 mA_p.
- Now, let's use the Complete model of the diode to determine the actual voltage across the Zener (and the load resistor) at the peak of the regulator's cycle: $V_D = V_Z + I_Z * Z_{ZT}$ = 5.1 V + 43.0 mA_p*7.0 Ω = 5.40 V_{DC}. That's a bit disturbing, as we're using the Zener to "regulate" the voltage at 5.1 V_{DC}. More on that later.
- Let's also determine what voltage would be expected across the Zener if the load resistor was completely removed (i.e. no load attached). $V_D = V_Z + I_Z * Z_{ZT}$ = 5.1 V + 94.0 mA_p*7.0 Ω = 5.76 V_{DC}.

If you think about it, the last two results could get us going on an endless loop of refinements, because the load voltage is no longer what we predicted with the Practical model, so the current is wrong so the load voltage is wrong so the current is wrong .... However, we won't do any iterations on the calculation, because we've based our calculations on some fairly variable values already, such at the diode voltage drops and the supply line voltage.

The formal term for the effect on the output voltage of changing the resistance of the load is ***Load Regulation***. A good voltage regulator will not be affected seriously by the load applied. This means that the Zener regulator we're analyzing does not have good Load Regulation, since it changes from 5.76 V_{DC} when not loaded to 5.40 V_{DC} when typically loaded; theoretically, it could be loaded sufficiently to drop the regulated voltage to 5.1 V_{DC} before it quits regulating at all, so its output could vary by about 0.66 V in response to load changes.

While we're at it, the output voltage would also be affected if the line voltage changed: an increase in line voltage would mean an increase in the peak voltage presented to the current-limiting resistor, which in turn would mean a higher total current, more of which would go through the Zener, resulting in a higher output voltage. The formal term for the effect on the output voltage of changing the supply voltage is ***Line Regulation***. We won't do an analysis of this for our circuit, but suffice it to say that the Zener regulator does not have very good Line regulation performance, either.

Also, it should be apparent that, as the input voltage swings up and down due to its ripple, the output voltage will also swing up and down a little bit, but much less than the input. The measure of the reduction of ripple in a regulator circuit is referred to as ***Ripple Rejection***. Since most regulators significantly reduce the amount of ripple in a signal, the ripple rejection is usually stated in decibels.

$$RR = 20\ \log\left(\frac{V_{r(in)}}{V_{r(out)}}\right)$$

- To do a worst-case analysis of the ripple rejection of the unregulated input to the regulator, we'll use the peak values from our previous calculation.
    - Using the peak total current, we can determine the worst case ripple voltage at the output of the rectifier using $V_r = \frac{I_L T}{C}$ =94.0 mA_p*(1/120 Hz)/470 μF = 1.67 $V_{p\text{-}p}$.
- To determine the output ripple, we've already calculated the voltage expected when the input signal is at its maximum point: 5.40 V. Now we need to calculate the minimum so we can subtract it from the maximum to get the peak-to-peak output ripple.
    - The minimum value for the signal out of the regulator is $V_{min} = V_{max} - V_r = 8.76\ V_p - 1.67\ V_{p\text{-}p} = 7.10$ V
    - From this, we can determine the current through the current-limiting resistor: I_{min} = (7.10 V - 5.1 V)/39 Ω = 51.3 mA
    - The current through the Zener diode would be this minimum total current minus the load current, or 51.3 mA - 51.0 mA = 0.3 mA.
    - Using the Complete model of the Zener diode, we can determine that the output voltage at this minimum point would be 5.1 V + 0.3 mA * 7 Ω = 5.10 V (essentially the Zener voltage, since the current is so small).
    - So, the output ripple would be 5.40 V - 5.10 V = 0.3 $V_{p\text{-}p}$
- Finally, we can do a Ripple Rejection calculation: RR=20log(1.67 $V_{p\text{-}p}$/0.3 $V_{p\text{-}p}$) = 14.9 dB

Since most regulators have Ripple Rejection values of over 50 dB, this is not a great regulator from a Ripple Rejection point of view, either.

Much more important than the variation in output voltage is the power wasted by this circuit.

16. How much "useful" power is dissipated by the 100 Ω load? _____ mW
17. At the peak of the rectifier signal, how much power does this entire circuit dissipate? _____ mW
18. At the peak, what is the efficiency of this circuit? _____ %

Clearly, a circuit that wastes two-thirds of the power it consumes is not a very good circuit. This circuit is wasteful because it "shunts" whatever current is not needed through the Zener diode in order to maintain the desired voltage across the load, and is therefore referred to as a **Shunt Regulator**, or parallel regulator.

The points of this exercise were to introduce the concept of regulation, provide you some familiarity with the Zener diode, and to give you an example of a "quick and dirty" regulator circuit you could use if your circuit requirements in a particular project aren't too rigid. You won't be asked to build or analyze a Zener Regulator again in this course. That's because there are much better (and easier) ways to regulate voltages in an electronic circuit.

Integrated Circuit Regulators

Voltage regulation is required for practically all electronic circuits. Many devices have a single DC power supply, then regulate that down to the various voltages required by different parts of the circuit. Our microcontroller development kit, for example, uses an unregulated +12 V supply, and we create +10 VDC, -10 VDC, +5.120 VDC, +5 VDC, +3.3 VDC, and +2.5 VDC from it to drive the various chips installed on the board. Fortunately, there are commercially-available Integrated Circuit Regulators to handle all of these required voltages.

Linear Regulators and Switching Regulators

Linear Regulators are simple devices to use, typically available as three-pin devices and requiring no external components other than filtering capacitors. However, as with most simple things, these are limited in their application. Linear Regulators can only reduce the available voltage -- they can't step it up to a higher voltage; and Linear Regulators cannot invert the voltage -- a positive Linear Regulator can only produce a positive output from a positive input, and a negative Linear Regulator can only produce a negative output from a negative input.

Switching Regulators are more complex, requiring external components -- typically a Schottky Diode, an inductor, two feedback resistors, and a frequency setting capacitor, in addition to filtering capacitors at the input and the output. However, by switching a current on and off through an inductor, Switching Regulators can be designed to it all: drop the voltage, increase the voltage, and invert the voltage. In addition, Switching Regulators are more efficient than Linear Regulators, and rarely need heatsinks for typical small applications.

Linear Regulators

Linear Regulators, unlike the Zener Diode Shunt Regulator, are Series Regulators -- they operate by limiting the current through the load to maintain a constant output voltage. If no load is attached, no current is required, so the regulator draws essentially no appreciable current. When a load is attached, current is supplied as needed. Power lost when using a Linear Regulator is due to the voltage drop across the regulator, which behaves like a variable resistor to control the current. Therefore, the bigger the difference between the input unregulated voltage and the output regulated voltage, the greater the power dissipated by the regulator as heat. Also, the greater the current through the regulator, the greater the power dissipated as heat.

19. A Linear Regulator is being used to produce +5 VDC from +12 VDC. How much power is dissipated by the regulator if the current drawn is 500 mA? _____ W ... if the current drawn is 20 mA? _____ mW.
20. How much power would be dissipated by the same Linear Regulator, producing 500 mA of current, if it was using +8 VDC at its input instead of +12 V? _____ W

Very often, Linear Regulators require heatsinks to prevent them from burning out or from causing heat damage to other parts of a piece of equipment. The manufacturer's specification sheet provides information that can be used in determining the heat sink requirements.

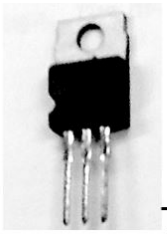
Question 3: (1 point)

Fixed Linear Regulators

The simplest linear regulators are designed to produce a fixed output voltage. The most commonly-used family of these are the 78xx positive regulators and 79xx negative regulators, where the 'xx' represents the output voltage of the device. Typical values for 'xx' are 05, 06, 08, 09, 10, 12, 15, 18, and 24. These regulators require an input voltage of at least 2 V more than the output voltage. This "overhead" voltage is also called the **Dropout Voltage**, because if the input supply drops below the required value, the output voltage will "drop out", or go below the expected regulated output voltage.

More expensive Linear Regulators do not require as much overhead, and are called **Low Dropout Regulators**, or **LDO Regulators**.

Many of the Fixed Linear Regulators are available in a higher-power package called the TO220 Package, shown below.


TO220 Package

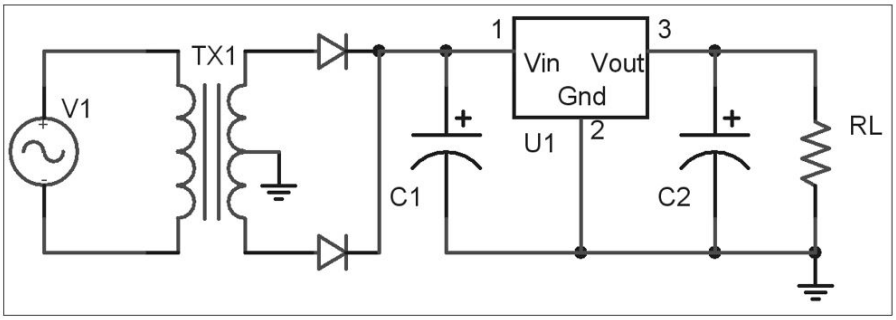
Unfortunately, the pinout for the 78xx devices is different from that of the 79xx devices, as shown below. Also notice that the metal tab is not passive -- it is connected to one of the internal voltages!

Pin	78xx	79xx
1 (left)	Input	Ground
2 (mid)	Ground	Input
3 (right)	Output	Output
Metal Back	Ground	Input

Questions:

1. What is the expected output voltage for an LM7812? _____ V_{DC}
2. What relatively inexpensive device would produce -8 V_{DC} from -12 V_{DC}? _____
3. What general group of Linear Regulators can generate an output voltage using an input voltage that is less than 2 V greater than the expected output? _____
4. What general group of regulators can produce a voltage higher than the input voltage? _____
5. What general group of regulators can produce a negative voltage from a positive voltage? _____

Question: Use the schematic below to answer the questions that follow. V1 is 115 VAC, the transformer turns ratio is 6:1, the rectifier diodes have a forward voltage drop of 0.6 V, C1 is 470 µF, and RL is never lower than 75 Ω.

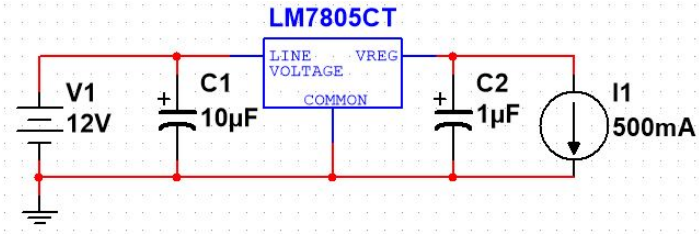


1. Given that U1 is an inexpensive fixed linear regulator, what device number would be required if the output voltage is expected to be +8 VDC? _____
2. What is the peak voltage at the output from the rectifier? _____ V_p
3. What is the load current for the heaviest load allowed? _____ mA
4. Based on the maximum load current, what is the expected ripple voltage? _____ V_{p-p}
5. How low does the ripple voltage drop to? _____ V
6. Given the specified dropout voltage for the device chosen, will the ripple voltage result in droputs in the output signal? _____
7. What is the average voltage of the unregulated input signal? _____ V_{DC}

8. Assuming that the RMS voltage of the unregulated input signal is fairly similar to the average voltage, what power is dissipated by U1 when connected to the heaviest allowable load? _____ mW
9. From the manufacturer's specification sheet (https://www.st.com/resource/en/datasheet/l78.pdf), locate this device's ripple rejection. It's called "Supply Voltage Rejection" in this data sheet. _____ dB
10. Use this ripple rejection value to determine the expected ripple for the output signal. _____ mV_{p-p}

As can be seen from this last example, the 7808 Linear Regulator is much better at rejecting the input voltage ripple than the Zener Diode regulator on the previous page.

Here's a quick worked example of a fixed regulator circuit that also introduces some of the basic concepts involved in choosing an appropriate heatsink. In this application, a 12 VDC supply is available, but the desired voltage is 5.0 VDC; so an LM7805 has been chosen. The load is expected to draw up to 500 mA from the regulator.



The output voltage, as indicated above and as can be determined from the part number, is +5 VDC.

The device can operate with any unregulated input that provides 2.0 V overhead. In this case, there is an overhead of 7.0 V, so there will be no problems with the device maintaining regulation.

However, power will be an issue. $P = I\Delta V$ = 500 mA*(12.0 V -5.0 V) = 3.5 W.

Here's a snippet of the datasheet to help us determine if the circuit needs a heatsink.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Value	Unit
V_I	Input Voltage	V_O = 5 V to 18 V	35	V
		V_O = 24 V	40	
$R_{\theta JC}$	Thermal Resistance, Junction-Case (TO-220)		5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-Air (TO-220)		65	°C/W
T_{OPR}	Operating Temperature Range	LM78xx	-40 to +125	°C
		LM78xxA	0 to +125	
T_{STG}	Storage Temperature Range		- 65 to +150	°C

Notice that two values are provided related to the dissipation of heat -- one from the "junction" i.e. the silicon to the outside of the component and one from the junction to the surrounding air. At this point, let's work with just the second one to see if we can get away with not using a heatsink.

The change in temperature between the air and the junction can be calculated by multiplying the thermal resistance by the power dissipation; so ΔT = 3.5 W * 65°C/W = 227.5°C. If the ambient temperature is 25°C, the junction temperature will be 252.5°C. However, the operating temperature cannot exceed 125°C, so we will need a heatsink on this circuit.

If we want to keep the temperature at a safe value, say 55°C (the temperature of very hot tap water), assuming a room temperature of approximately 25°C we would need to have an overall thermal resistance of (55°C - 25°C)/3.5 W = 8.7°C/W. Since the thermal resistance from junction to case is 5°C/W, we would need a heatsink with a thermal resistance to air of 3.7°C/W or less. A quick search at digikey.ca turned up the following heatsink, which takes up a fair bit of space and costs about $2.50:

In an actual design, we'd also need to consider the thermal resistance between the IC case and the heatsink, although that can be reduced to the point of being negligible using a thermal paste between the regulator and the heatsink.

Question 4: (1 point)

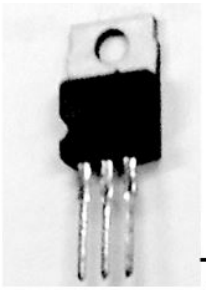
Adjustable Linear Regulators

As nice as it is to be able to buy a simple device that produces a constant output voltage, the Fixed Linear Regulators are limited to the output voltages selected by the manufacturer. The Adjustable Linear Regulators provide the possibility to produce other voltages, and, using potentiometers in the feedback, to provide a range of output voltages from the same device. Benchtop power supplies use adjustable regulators to allow the user to set the output voltage to anything they want, within the limits of the equipment.

The most common Adjustable Linear Regulators are the positive in - positive out LM317 and the negative in - negative out LM337.

These two devices have the same pinout, which is nice, but the pinout is not intuitive, so many students wire these up incorrectly and burn them out. Be careful!

Again, these typically come in a TO220 Package.



TO220 Package

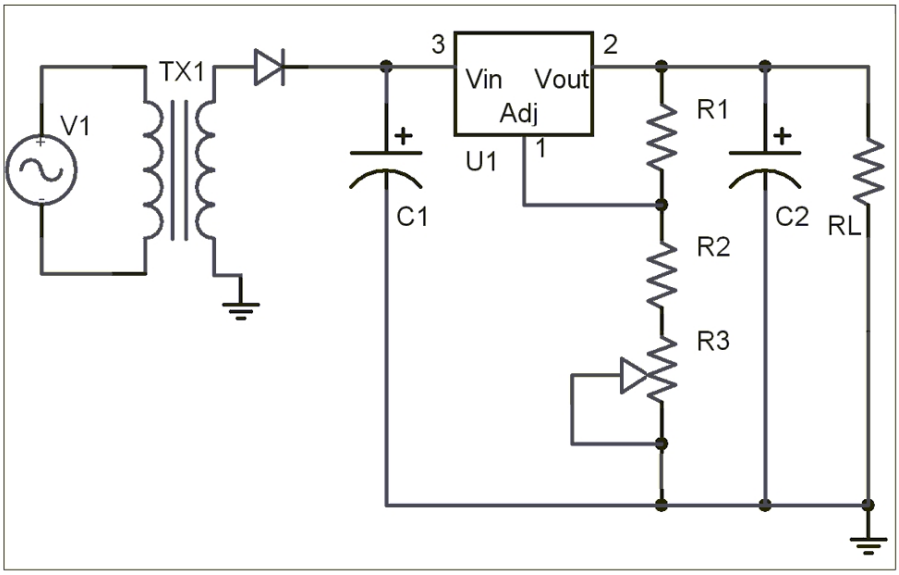
Pin	Function
1	Adj
2	Vout
3	Vin
Metal Back	Vout

Three things are important when using these devices in a design:

1. The dropout voltage is 2.5 V
2. The voltage between Vout and Adj is designed to be 1.25 V
3. There is a small, constant leakage current of about 50 μA, from the Adj pin

Point #2 is the most important one -- it's the one we use to come up with a workable design. However, the other two points need to be taken into account in order to avoid nasty surprises.

Here's a typical design using an adjustable linear regulator.



Notice that, since the regulator is not directly referenced to ground, the leakage current from pin 1, Adj, passes through R2 and R3, and will therefore produce an error voltage in the design. Let's investigate:

1. If the combined value of R2 and R3 is 2.0 kΩ, what error in the output voltage would be introduced by the 50 μA leakage current? _____ V
2. If, however, the combined value of R2 and R3 is 10 kΩ, what error in the output voltage would be introduced? _____ V

Clearly, to minimize the error introduced by the leakage current, the resistance between the Adj pin and ground must be kept small. However, the 1.25 V between the Vout and the Adj is usually smaller than the voltage across R2 and R3, so that means R1 is typically smaller, and sometimes significantly smaller, than the R2, R3 combination. As a rule of thumb, we aim for a combined resistance of R2 and R3 of 2 kΩ or slightly less to give us some room to pick suitable resistors.

Question: For the circuit above, assume V1 is 120 VAC at 60 Hz, the transformer turns ratio is 10:1, the rectifier diode has a forward voltage drop of 0.7 V, C1 is 680 μF, C2 is 10 μF, and the minimum resistance of RL is 100 Ω.

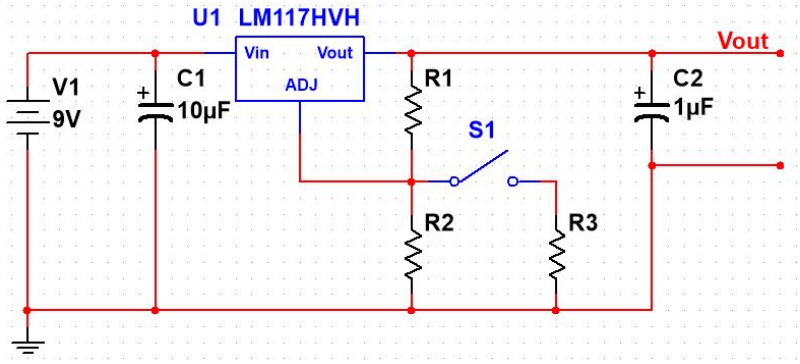
1. Which adjustable regulator should we use for U1? _____
2. What is the peak voltage at the output from the rectifier? _____ V_p
3. Starting with a combined value for R2 and R3 of 2 kΩ, calculate a value for R1 that will produce an output voltage of 8,192 mV. _____ Ω
4. Locate a list of 10% resistor values (there's one on the formula sheet for this course). Since there isn't a 10% resistor value that exactly matches the calculated value, pick the next smallest one (picking a bigger one would mean we would have to increase the R2, R3 combination, which we don't want to do) _____ Ω
5. Now for the R2, R3 combination. Typically, to allow for fine tuning, we make the fixed resistor 2x to 5x bigger than the potentiometer. Potentiometers, being adjustable, don't come in a lot of values -- typically multiples of 1, 2, or 5. Usually, we would play with the numbers until a suitable set is arrived at, but to help with Mobius grading, let's start with the assumption that the fixed resistor will be 3x the size of the potentiometer. Fixed resistor = _____ kΩ, Potentiometer = _____ Ω
6. In reality, we would simply adjust the potentiometer until the output is what we want it to be. What would the combined resistance of R2 and R3 be, approximately, when the output is adjusted to 8192 mV? _____ kΩ
7. What is the maximum load current, once the voltage is set to 8192 mV? _____ mA
8. What ripple voltage would be seen at the output from the rectifier diode? _____ V_{p-p}
9. Using this ripple voltage, what voltage would the unregulated input signal drop to each cycle? _____ V
10. Is this likely to cause dropouts in the output signal? _____

Worked Example: Selectable 3.3 V / 5 V Regulator

For this circuit, a client has asked for a regulator operating from a 9 V battery that has a switch to select between 3.3 VDC and 5 VDC. Since the LM317 requires an overhead of 2.5 V, we'll have no trouble using a 9 V battery, because it will give us an overhead of 4.0 V when generating 5 VDC, which is ample.

Assuming that the choice of voltages means that this will be a power supply for TTL-level devices (5 V) or LVTTL-level devices (3.3 V), there will be a range of allowable voltages: "5 V" for TTL can range from 4.5 V to 5.5 V, and "3.3 V" for LVTTL can range from 2.7 V to 3.6 V. We'll aim for values equal to or slightly higher than the nominal voltages.

For this design, we'll pick a fixed value for the resistor between the Vout and ADJ pins of an LM317-style regulator, and we'll provide two different values for the other resistance by switching in a second resistor in parallel, as shown in the following schematic. The LM117HVH is a military-specification version of the LM317, and is used in this schematic because it's the only version of the IC that's available in Multisim.



The larger the resistance between ADJ and ground, the higher the output voltage. So, we'll start our design for 5 VDC, as that will only involve R1 and R2 in the calculations. That way, we can make R2 a reasonable size but still less than the 2 kΩ maximum needed to minimize the efffect of leakage current.

The voltage divider formula used for the feedback network can be rearranged to provide us with the ratio of the resistor values:

$$V_{reg} = 1.25\left(\frac{R_1}{R_1+R_2}\right)$$

rearranges to

$$\frac{R_2}{R_1} = \frac{V_{reg} - 1.25}{1.25}$$

For 5 V, then, R_2/R_1= 3.00

Playing around with the various 10% resistor values in the kit, the closest we can get to this ratio is R_2 = 1.2 kΩ and R_1 = 390 Ω. To see how close our theoretical results (based on the chosen values) are to the ideal value, we'll enter the resistors into the original formula. When we do this, we get V_{reg} = 5.1 VDC, which meets our specifications.

For 3.3 V, we'll need to use the same R_1 -- 390 Ω -- and determine what resistor we'll need to have in parallel with R_2 to get close to 3.3 V.

The ratio of resistances gives us, for 3.3 V, R_2/R_1 = 1.64

So that means the parallel combination of R_2 and R_3 needs to be 1.64*390 Ω, or 640 Ω

Rearranging the parallel resistor calculation is a bit of a challenge -- give it a try!

$$R_T = \frac{1}{\frac{1}{R_2} + \frac{1}{R_3}}$$

rearranges to

$$R_3 = \frac{R_2 \cdot R_T}{R_2 - R_T}$$

... which produces a value of 1.37 kΩ for R_3 using our chosen value of 1.2 kΩ for R_2. 1.37 kΩ is halfway between two 10% resistor values, so we'll choose the larger value to bump the voltage up slightly. We'll pick R_3 = 1.5 kΩ.

Again, we'll check to see that the theoretical output for this resistor is to see if it matches the specification. We get 3.4 VDC, which is suitable.

Question 5: (1 point)

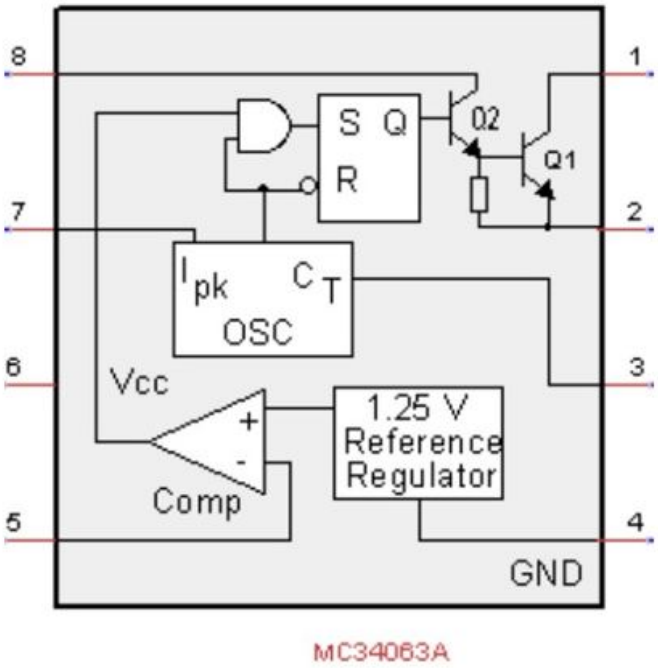
Switching Regulators

Switching regulators are considerably more complex than linear regulators, both in terms of the components required and the design process. Consequently, this course is not intended to provide an in-depth coverage of these designs – only a quick overview.

All switching regulators require a high-speed switching controller with an electronic switch, an inductor, a diode (typically a Schottky diode), a storage capacitor, and a feedback network. Different arrangements of these circuit elements allow for basically three configurations:

- Buck Mode: very efficient step-down only
- Boost Mode: best used as a step-up regulator, but will do step down (not as efficient as Buck)
- Buck-Boost Mode: voltage-inverting regulator, step up or step down

One example of the high-speed switching controller is the MC34063A, pictured below with its internal block diagram displayed.



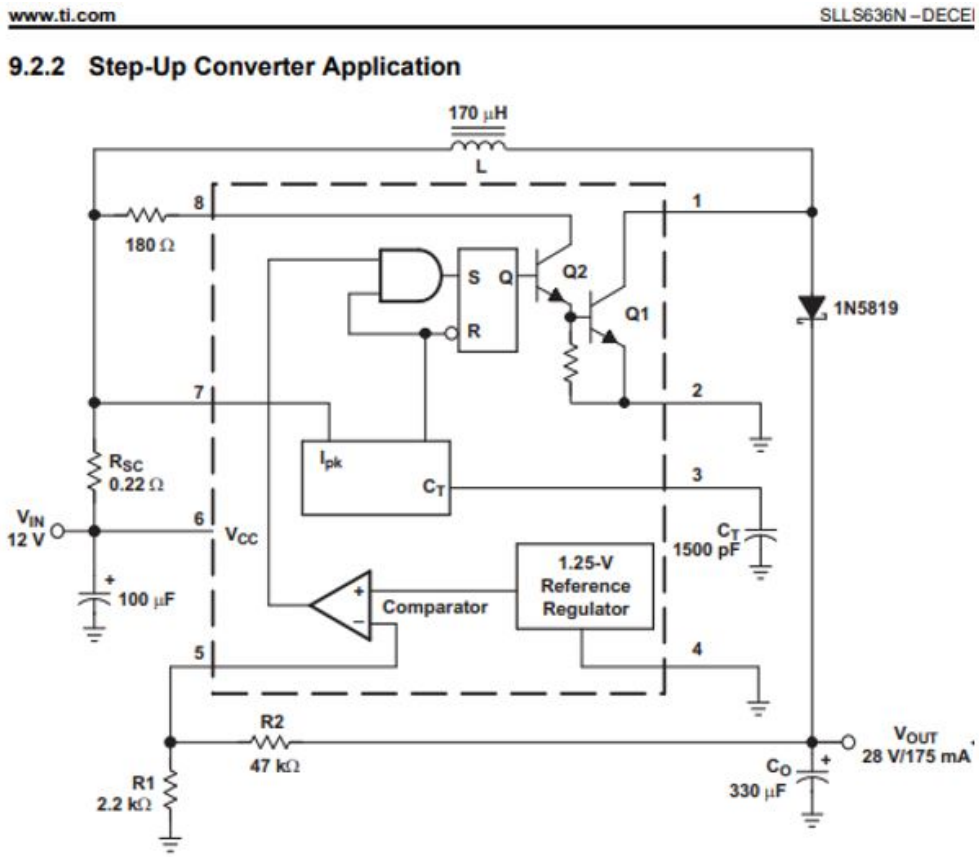
MC34063A

Here's a brief description of the various components. As you proceed with this course, along with your digital logic course and embedded processors course, you will learn more about the concepts behind each of these blocks. However, a quick overview at this point will help you understand how this IC works.

- OSC is an oscillator -- a device that runs as a clocking device at a speed established by a capacitor connected to CT at pin 3. This is usually set to run at 100 kHz or higher so that this "switching frequency" can be easily filtered out of the final DC supply voltage. The oscillator can also be shut down by an external current-sensing network through Ipk at pin 7. Typically, a very small resistance value is placed between the unregulated supply and pin 7 as a current-sensing device.
- The 1.25 V Reference Regulator provides a constant voltage with respect to pin 4, which is typically connected to ground.
- Pin 5 provides feedback from the output signal. Typically, a voltage divider from the output is designed to provide 1.25 V to this pin when the output is at the desired value.
- Comp is a voltage comparator that indicates whether the feedback from the circuit is higher or lower than the 1.25 V reference. If the feedback is too low, the comparator indicates to the remaining circuitry that more current must be provided to increase the output voltage; if the feedback is too high, the comparator indicates that less current should be provided to decrease the output voltage.
- The S-R Flip-Flop is a digital logic circuit used, in this case, to control a transistor switch. One of its inputs is the clock signal from the oscillator; the other is the output from the comparator. For reasons likely beyond your current level of understanding, this combination results in a Pulse-Width Modulated (PWM) signal that drives the transistor switch. When more current is required, the transistor is turned on for a greater part of the period of the clock (higher duty cycle), and when less current is required, the transistor is turned on for a lesser part of the period of the clock (lower duty cycle).
- The Transistor Switch allows current to flow from the unregulated power supply to the remaining circuitry only when the S-R Flip-Flop's output is active.

Boost Mode Switching Regulator

The easiest of the three configurations to understand is the Boost Mode Regulator, pictured below from Texas Instruments datasheet https://www.ti.com/lit/ds/symlink/mc34063a.pdf (https://www.ti.com/lit/ds/symlink/mc34063a.pdf).



Here's a simplified explanation of its operation.

- When the switch is closed, current from the unregulated supply connected to Pin 6 begins to move through the inductor, L, through the current-sensing resistor RSC and the transistor switch to ground.
- Once this current has been established, the switch opens. The current cannot stop instantly, so it generates a voltage high enough to drive through the Schottky Diode to the storage capacitor on Vout.
- R1 and R2 provide feedback to the comparator, which then determines if the output voltage is too high or not high enough, thereby controlling the pulse-width of the switch-controlling signal.

Since the current-charged inductor is very nearly an ideal current source, it will increase the voltage to whatever is required to make its current flow, so the output voltage can be significantly higher than the unregulated input voltage. The only limitation is the breakdown voltage of the transistor switch. This limitation can be overcome by using an additional high-voltage transistor external to the IC.

This circuit is more efficient than typical linear regulators because the switch is either on or off: ON means practically no resistance so no power loss, OFF means no current so no power loss. However, it isn't the most efficient switching circuit because it "wastes" the electrical power required to establish the inductor current while the switch is connected to ground.

Another issue with this circuit is that it is not short-circuit protected. If the output is shorted to ground, current will flow from the unregulated voltage through RSC, the inductor, and the Schottky Diode directly to ground, unaffected by the switch condition. This will probably result in the thermal destruction of one of the series components, likely the diode.

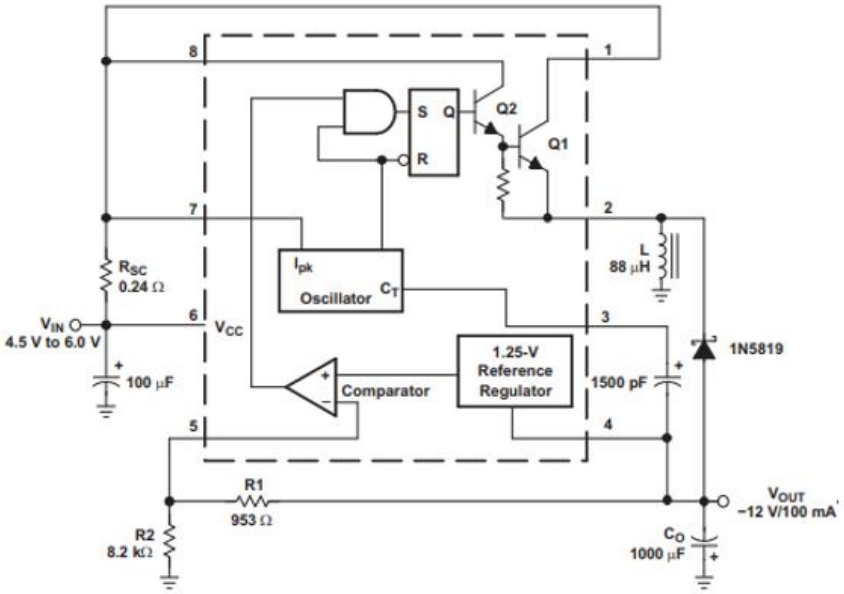
Question:

1. Use the voltage divider to determine the output voltage for this circuit: _____ VDC

Buck-Boost Mode Switching Regulator

The Buck-Boost Mode is very similar to the Boost Mode, except that the reference voltage is the output instead of ground, the inductor goes to ground instead of coming from the unregulated input, and the Schottky diode and capacitor are reversed. The result is a negative output from a positive input. Here is the circuit, pictured below from the Texas Instruments datasheet.

9.2.1 Voltage-Inverting Converter Application



- When the switch is closed, current builds up through the inductor to ground.
- When the switch is open, the inductor current continues to flow, this time “pulling”, or “bucking” current from the storage capacitor at Vout through the Schottky diode, resulting in a negative output voltage.
- The voltage divider provides feedback from ground to the negative output, which is compared to the 1.25 V reference to control the PWM circuitry. The reference is now 1.25 V more positive than the output voltage, because its point of reference is the negative output instead of ground.

Again, since this circuit “wastes” current to ground when the switch is closed, its efficiency is not optimal. However, it is still more efficient than the linear regulators.

Clearly, the biggest reason for using this configuration is to produce a negative voltage from a positive unregulated input, which eliminates the need for an unregulated negative supply. The fact that it can produce a negative voltage with a greater magnitude than the input voltage is another valuable feature.

Also, notice that, if the output is shorted, opening the switch prevents the flow of current from the unregulated supply to either ground or the output, so this circuit is short-circuit protected if RSC is installed.

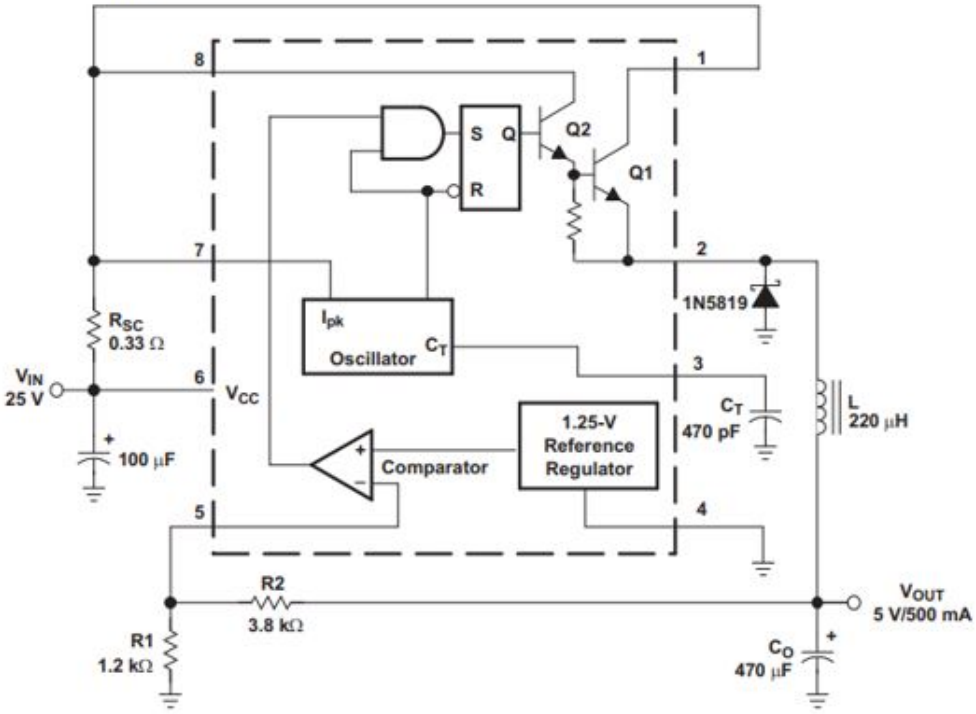
Question:

2. Use the voltage divider to determine the output voltage: _____ VDC

Buck Mode Switching Regulator

The Buck Mode regulator is the most efficient circuit of the three, but it has its limitations. Here is the circuit, pictured below from the Texas Instruments datasheet.

9.2.3 Step-Down Converter Application



- When the switch closes, current flows from the unregulated supply through the inductor to the storage capacitor at the output.
- When the switch opens, the inductor's current continues to flow, "pulling" or "bucking" current from ground through the Schottky Diode, which also ends up on the storage capacitor.
- The feedback network established by R1 and R2 tells the comparator whether the output voltage is too high or too low, in order to adjust the PWM duty cycle to compensate.

Buck Mode is very efficient, because both the current used to establish the inductor current and the current pulled through the inductor when the switch opens charge the output capacitor. Typical applications are claimed to approach 98% efficiency. However, the output voltage must be lower than the unregulated supply, so it is more limited than the Boost Mode or Buck-Boost Mode regulators.

Notice, also, that shutting off the switch shuts off the current, so, as long as RSC is installed, this design is short-circuit protected.

Question:

3. The current limiter kicks in when the peak voltage at Ipk is 0.3 V below Vin. What is the peak current allowed for the circuit as shown above? _____ mA You may be surprised that this isn't the number indicated above. The designers of this circuit have been careful to indicate a value considerably lower than the calculated value, as the circuit will become noisier and may not maintain good regulation close the the limit imposed by the current-limiting resistor.

Question 6: (1 point)

Uninterruptable Power Supplies

Networking and industrial computing systems are supposed to be reliable, with almost no down-time. The catch-phrase is “five nines”, meaning that the system should be up and running 99.999% of the time. In order to help ensure this, equipment needs to be supplied with power that will not be affected by temporary outages or brown-outs in the transmission and distribution system.

An Uninterruptable Power Supply (UPS) is a device that uses battery storage to provide power when the power distribution system fails. Of course, the UPS can only supply power until its batteries lose their charge, so the storage capacity of the UPS batteries must be considered when acquiring a UPS.

There are a few different technologies used for uninterruptable power supplies. Simple units for home or small office use are typically Standby systems, whereas larger, more sophisticated applications require Double Conversion systems.

Standby UPS

During normal operation, the output receptacles in a Standby system are switched directly to the building supply, and the battery is trickle-charged using a DC battery-charging system, similar to the filtered DC power supplies you’ve recently studied.

When the building electrical supply fails, a sensor in the UPS quickly detects the failure, activates an ***inverter*** which converts the DC power supplied by the battery to 120 VAC, and delivers this to the duplex receptacles on the device. Usually, an alarm is activated to let operators know that the building electrical supply has failed. When the power returns, the unit goes back to its original configuration.

The inverter is a device that uses switches (usually powerful transistors controlled by logic circuits), inductors, and capacitors to convert low voltage DC to 120 VAC at 60 Hz (for North America).

A simplified description of one type of inverter goes like this:

- One pair of switches closes temporarily (every 1/60th of a second, in the first half of the output signal), allowing the 12 V battery to build up a current flowing in one direction through an inductor.
- Once the current has been established, it cannot be stopped instantly. So, when the switches are opened, the current will continue to flow, and will develop whatever voltage is necessary to maintain the current. In this way, the 12 VDC input can be used to produce a 170 Vp (i.e. 120 VRMS) output.
- Another pair of switches closes temporarily (every 1/60th of a second, in the second half of the output signal), allowing the 12 V battery to build up a current flowing in the opposite direction through the inductor.
- When the switches are opened, the current will continue to flow, and will develop whatever voltage is necessary to maintain that current. In this way, the 12 VDC input can be used to produce the negative peak of the output waveform.
- Additional circuitry helps to smooth out the voltage transitions to make the output more sinusoidal. Some inverters break up the rising and falling parts of the cycle into steps, whereas other, more expensive units, may produce “true sine waves”.
- Sensors monitor the output voltage and adjust the amount of time the switches are closed each cycle (thereby controlling the inductor current) to keep the output voltage within acceptable levels.

Double-Conversion UPS

One of the issues with the Standby system is the small glitch in power that occurs as the system switches between line and backup power. In a double-conversion system, the building power is always converted immediately to DC, then, using a true sine wave inverter, is always converted back to the AC that is used by the attached equipment. The battery is always in parallel with the DC part of the system. When the building supply fails, the system continues to produce the required AC, but from the battery only.

These systems are more expensive, due to the extra complexity of pure sine wave inverters, and will likely only be employed for larger applications.

Selecting a UPS

When it comes to choosing a UPS for a particular application, the following items should be considered.

- Storage capacity – How much energy is needed to keep the attached equipment powered for 15 minutes, as most power failures are fairly short in duration? The storage capacity must be chosen on the basis of the power requirements of the attached equipment. Storage capacity may be indicated in joules (typically megajoules), kilowatt-hours, or, more typically, in amp-hours. The first two are a true measure of stored energy; the voltage of the batteries must be considered when determining the actual energy stored when the battery is rated in amp-hours.
- Power signal purity – Some inverters, typically those in standby systems, produce signals that are more like square waves, rising and falling staircases, or triangle waves – not pure sine waves. This may adversely affect equipment relying on the AC signals, such as CRT monitors or audio equipment. Also, the frequency will not be as precisely controlled as it is in the distribution grid, so anything that relies on the power line frequency for timing will lose its accuracy. In a standby system, the power glitch when switching from line power to inverter power may be unacceptable, depending on what is being powered.

- System monitoring – This may be provided in different ways:
  - Some simple UPS devices produce an audible tone to indicate a power failure.
  - If the UPS is to be placed in a service closet or server room, it probably makes sense to buy one that automatically calls a monitoring service whenever the power goes down.
  - In an application where a computer is to be left running but unsupervised, it's possible to implement a UPS that sends a "standby" or "shut-down" signal to the computer via USB when the UPS battery is on the verge of failing.
- Multiple redundancy – If an essential or critical service is being provided, it may be necessary to have several uninterruptable power supplies connected in such a way that, if one fails or loses its charge, others are available to take over operation.

Question:

One 120 V application requiring a UPS needs to provide a maximum current of 10.0 A to connected equipment.

How much electrical energy does the UPS unit need to store, in order to supply the maximum current for fifteen minutes?

1. …in megajoules: _____ MJ
2. …in kilowatt-hours: _____ kW.h
3. …in amp-hours for a 12 V battery [find the current required from 12 V first in order to provide the required power: _____ A] now use the current to find the storage requirement: _____ A.h
4. The equipment attached to this UPS is a mix of laptop computers, routers, and network switches, all of which are connected to the UPS by means of external DC adapters. Which type of UPS is best suited to this application? _____

Online Homework System

Assignment Worksheet
9/15/22 - 12:03:46 PM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA03 Zeners and Regulation Activity

Question 1: (10 points)

When working with circuits, you will often see the following three terms, so it's important to know what they mean:

Ideal -- this is what you want the circuit to do, the specification you are designing the circuit for

Theoretical -- the predicted operation of the circuit, based upon models

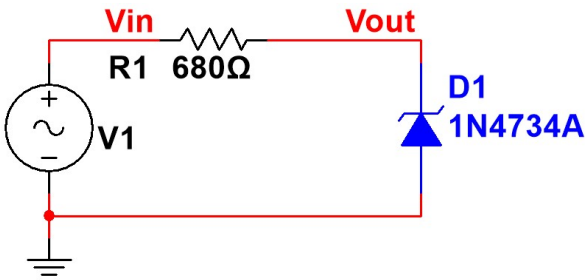
Empirical -- the actual performance of the circuit, based upon measured values

Using Multisim, build the following circuit. Use the positive side of the generic Function Generator as V_1 in the following circuit, and use the Tektronix oscilloscope to observe V_{in} on CH1 and V_{out} on CH2.

Note: On the generic Function Generator, there are two outputs -- one positive and one negative. Use the positive one, and reference the COM jack to ground.

Also Note: The generic Function Generator only allows you to enter values in peak volts -- since you are entering AC signals, divide the specified peak-to-peak values by two to get peak values.

Initially set up V_{in} to be a 60 Hz 15.0 $V_{p\text{-}p}$ sine wave with no DC offset.



You will need to reference the manufacturer's data sheet for the Zener diode, available through the Internet (or use this link (https://www.vishay.com/docs/85816/1n4728a.pdf)).

1. What is the theoretical upper limit of the output signal? _____ V.
2. The upper limit is determined by _____ .
3. Using the practical Zener model and voltages typically used in class, what is the theoretical lower limit of the output signal? _____ V.
4. The lower limit is determined by _____ .

Now, change the settings of the function generator so that V_{in} is a 60 Hz 3.0 $V_{p\text{-}p}$ **triangle** wave with a DC offset of +9.00 V_{DC} and a symmetry ("duty cycle" on this generator) of 20%. Adjust your oscilloscope so that this signal is properly displayed. To improve resolution, you could move the ground markers for both channels to one of the lines close to the bottom of the screen. Now, set up the second channel with the same settings, and use it to monitor V_{out}. You will probably have to play with the oscilloscope triggering to stabilize the display – make sure you've chosen the appropriate trigger source, given the shapes of the two signals displayed. (Hint: there must be visible variations in the signal chosen for the trigger to detect a starting edge, and the trigger level must be within the signal, as well.)

6. Record the voltage of the output signal, using the most appropriate unit of measure. _____ _____
7. Slowly decrease the DC offset (you can type in values with one or two decimal places, then use the keyboard or mouse to adjust them) until you see a change in the output signal. What is the voltage at the low point (Min) of the input signal when this undesirable change appears? _____ V.

What you have just observed is loss of regulation due to changes in the ***Line***. The ability of a regulator to compensate for changes in the unregulated input is called "Line Regulation".

If you had difficulty with any part of this exercise, ask your instructor to clarify or help you achieve the expected results.

7. Take a screenshot of your circuit and oscilloscope side by side, demonstrating the effect seen in this last part of the exercise, for your instructor to grade out of three marks. You will be marked for appropriate Horizontal and Vertical scales, as well as triggering. Document Upload (Direct)

Note: Don't use spaces or other special characters in you filename, but include something related to your name to help with identification while grading.

Online Homework System

Assignment Worksheet
5/20/22 - 9:26:27 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Photovoltaic Cells

Question 1: (1 point)

Photovoltaic Cells

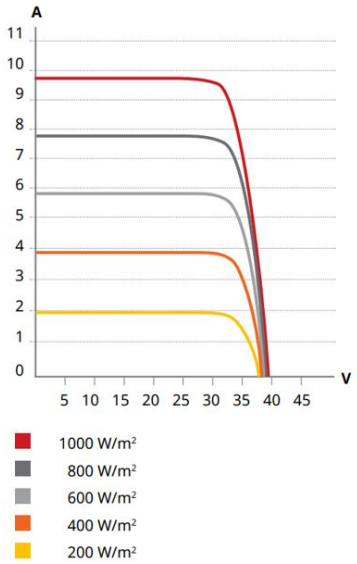
Photovoltaic Cells are also P-N junction devices, but set up to maximize the Photovoltaic Effect.

When a photon of light encounters an electron within the P-N junction's barrier region, the electron is ejected from its covalent bond and is driven by the potential difference of the barrier region into the N-Type material. The hole left behind migrates into the P-Type material, resulting in a separation of charges – negative on the N-Type material and positive on the P-Type material.

If a current path is provided externally, the accumulated charge will flow through it to restore the original neutral condition.

The potential difference is essentially the barrier potential, so for an individual "cell", the potential difference is only about 0.6 V to 0.7 V. However, by increasing the surface area of an individual cell, significant current can be generated. Cells are then connected together in series to increase the potential difference (voltage) generated by a "solar panel". Further series and/or parallel connections result in the desired current and voltage characteristics of a solar array.

A solar panel behaves much like an ideal current source, where the available current is directly related to the "insolation", which is a measure of the light power per unit area striking the panel. As with any ideal current source, it will make the voltage whatever is required to drive the current, within reasonable limits. The following shows the characteristic curves for a KuPower CS3K solar panel from Canadian Solar Inc. (http://www.canadiansolar.com (http://www.canadiansolar.com)), along with other specifications for this panel, to be discussed below.



ELECTRICAL DATA | STC*

CS3K	285P	290P	295P	300P
Nominal Max. Power (Pmax)	285 W	290 W	295 W	300 W
Opt. Operating Voltage (Vmp)	32.1 V	32.3 V	32.5 V	32.7 V
Opt. Operating Current (Imp)	8.92 A	8.98 A	9.08 A	9.18 A
Open Circuit Voltage (Voc)	38.7 V	38.9 V	39.1 V	39.3 V
Short Circuit Current (Isc)	9.42 A	9.49 A	9.57 A	9.65 A
Module Efficiency	17.15%	17.45%	17.75%	18.05%
Operating Temperature	-40°C ~ +85°C			
Max. System Voltage	1000 V (IEC / UL) or 1500 V (IEC / UL)			
Module Fire Performance	TYPE 1 (UL 1703) or CLASS C (IEC 61730)			
Max. Series Fuse Rating	30 A			
Application Classification	Class A			
Power Tolerance	0 ~ + 5 W			

* Under Standard Test Conditions (STC) of irradiance of 1000 W/m², spectrum AM 1.5 and cell temperature of 25°C.

The graph provided is for the 290 W version. On the graph, the top line represents bright sunlight, at 1000 W/m^2, and the bottom line represents diffuse light at only 200 W/m^2. Both produce constant current (over 9.5 A for bright sunlight and only 2 A for diffuse light), up to a potential difference of about 35 V. After this, the current drops off. When the current drops to zero ("open circuit" conditions), the voltage is just under 40 V.

1. What value is given for the Short Circuit Current? _____ A. Notice that the graph indicates this is a conservative specification.
2. What value is given for the Open Circuit Voltage? _____ V. On the graph, this is where the current drops to zero.

Notice that the optimal operating voltage and current are slightly less than the two extreme values.

3. Find the point on the top line of the graph that corresponds to the coordinates given for optimal voltage and current. This point should be within the "knee" of the graph. What power is generated at this point, using the values from the

table? _____ W

4. Find the coordinates for a point about half-way along the voltage scale for the top line (pick 20 V). What power is generated at this point? _____ W
5. Find the coordinates for a point about half-way up the current scale for the top line (pick 5 A). What power is generated at this point? _____ W

The optimal operating values represent the point of Maximal Power. Since power is the product of current and voltage, operating at a lower voltage with the same current or operating at a lower current with the same voltage both result in a loss of power. A piece of equipment that locates and tracks the point of maximal power even as insolation (brightness) changes is called a Maximum Power Point Tracker (MPPT).

Often solar panels are used to charge batteries. If the solar panel open voltage is considerably higher than the battery voltage, directly connecting the panel to the battery results in a significant loss of power:

6. The solar panel above is connected directly to a 12 V battery. How much power can be harnessed by this system with bright sunlight? _____ W

A true MPPT battery charge controller would use a buck-mode switching system to adjust the voltage and current at its output in order to maximize the power.

7. If a true MPPT battery charge controller is used between the solar panel above and a 12 V battery, how much current would have to be available to the battery in order to utilize the panel's maximum power of 290 W? _____ A. How many times greater is this than the current available from the panel directly? _____ times greater.

Since the MPPT battery charge controller uses buck mode switching regulation, most are specified as having an efficiency in the range of 98%.

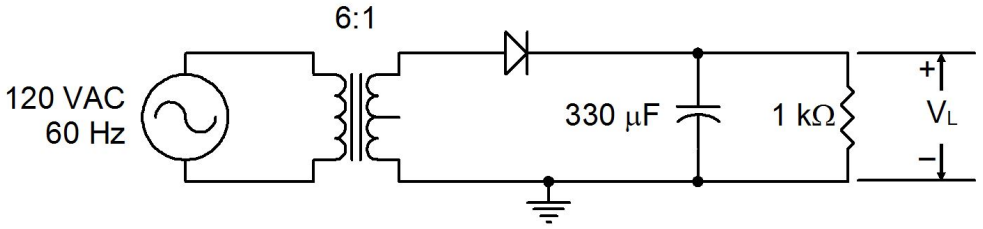
Online Homework System

Assignment Worksheet
5/31/21 - 9:17:46 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA04 Filtering, Regulation and PV Cells Quiz

Question 1: (8 points)

Use the circuit below to answer the following questions. Assume a forward-biased diode drop of 0.7 V.



Find the peak voltage across the load resistor.

_____ _____

Determine the worst case ripple voltage expected across the load resistor.

_____ _____

Determine the average voltage expected across the load resistor.

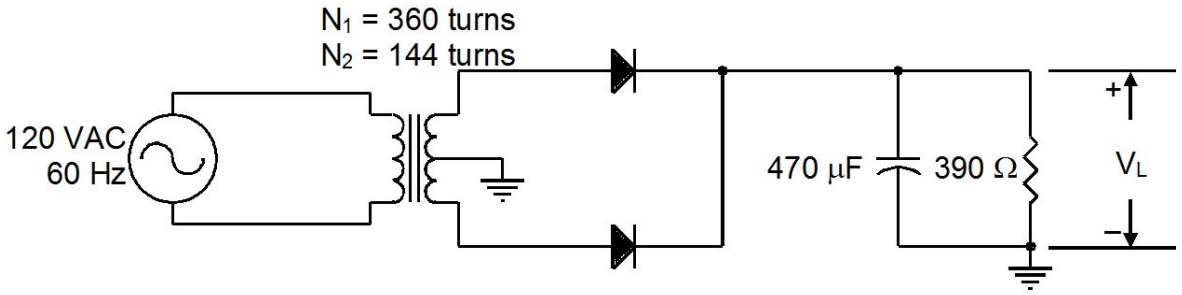
_____ _____

Find the minimum voltage expected across the load resistor.

_____ _____

Question 2: (8 points)

Use the circuit below for the following questions.



What is the peak voltage across the load resistor, assuming a forward-biased diode drop of 0.7 V?

_____ _____

Find the worst case ripple voltage seen across the capacitor.

_____ _____

Find the average voltage across the load resistor.

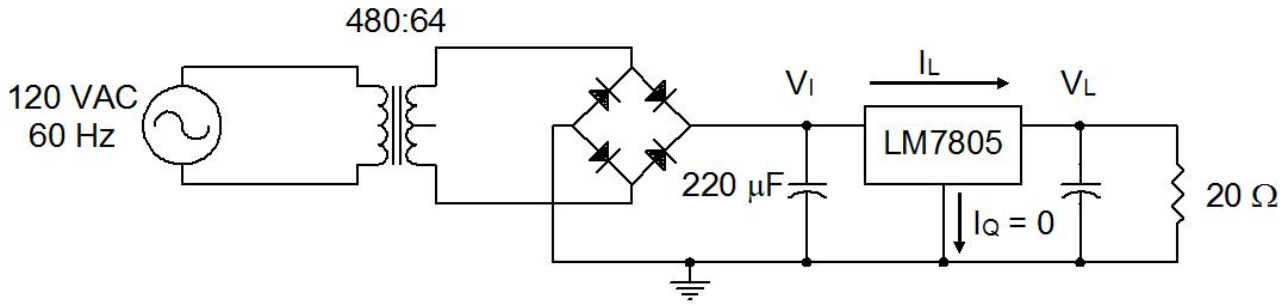
_____ _____

Find the minimum voltage across the load resistor.

_____ _____

Question 3: (9 points)

Use the circuit below to answer the following questions. Assume a forward diode drop of 0.7 V throughout.



What is the voltage expected across the load, VL?

_____ _____

What is the expected load current, IL, using proper engineering notation?

_____ _____

What is the expected peak voltage at the output of the rectifier, VI?

_____ _____

Determine the ripple voltage expected across the filter capacitor, assuming that the current directly to ground from the LM7805, IQ, is zero.

_____ _____

True/False: The output voltage is likely to exhibit dropouts when the unregulated input, VI, drops to its typical minimum voltage.

(a) True
(b) False

Question 4: (3 points)

Match the following regulators to the appropriate description.

_____

Question 5: (2 points)

In a circuit employing an MC34063A switching regulator controller, the resistive feedback network has a 10 kΩ and a 6.8 kΩ resistor between the output and ground, with the mid point of the voltage divider connected to the "Comp" pin. What will the output voltage of this regulator be? _____ _____ V

Question 6: (1 point)

Which type of Uninterruptable Power Supply converts DC battery voltage to clean AC power even when building power is available? _____

Question 7: (1 point)

Which Uninterruptible Power Supply configuration may not be suitable for equipment requiring true sine wave power? _____

Question 8: (1 point)

Photovoltaic cells demonstrate the behaviour of a nearly-ideal _____

Question 9: (5 points)

A particular solar panel has an optimal operating voltage of 32.5 V and an optimal operating current of 9.08 A. Treat these as the maximum operating voltage and current values for the following questions.

1. What is its power rating? _____ W
2. What power would it be capable of generating if it was connected directly to a 12 V battery as a charger? _____ W
3. What power would it be capable of generating if it was connected to a device that required 3.8 A at the operating voltage? _____ W
4. If the solar intensity dropped from the 1000 W/m^2 value expected for a cloudless day to 500 W/m^2,

   (a) The panel voltage would drop to approximately half

   (b) The panel current would drop to approximately half

   (c) Both the panel voltage and the panel current would drop by half
5. Shorting a solar panel will cause major damage, because the current will rise significantly -- true or false?
   (a) True
   (b) False

Question 10: (2 points)

A particular UPS uses a 12 V, 27 A.h battery for storage.

1. If this battery is designed to maintain an AC voltage of 120 VAC for 13 minutes, how much current would it supply at 12 V? _____ A
2. What would be the available current, at 120 VAC? _____ A

Online Homework System

Assignment Worksheet
9/23/22 - 9:10:41 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Lab03 Filtering and Regulation

Question 1: (10 points)

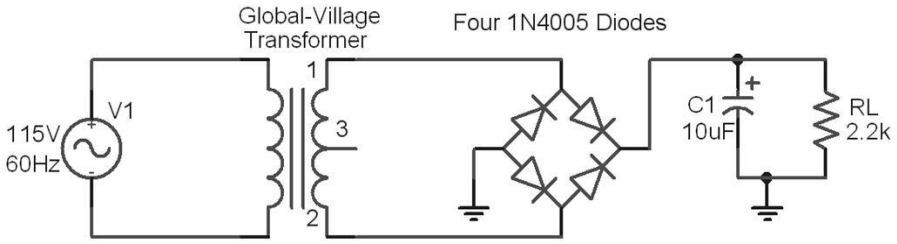
Lab 03 Pre-Lab

Note: Safety Glasses are required!

Note: Do not move on to the "Next" page until you have completed your Pre-Lab. The next page is the Lab Activity, and once you move to that page, you will not be able to return to the Pre-Lab page!

Filtered Bridge Rectifier Power Supply

Use the schematic diagram below to predict the circuit characteristics that follow. Assume that the transformer turns ratio is 6:1 and that the diodes have a forward barrier potential of 0.7 V.

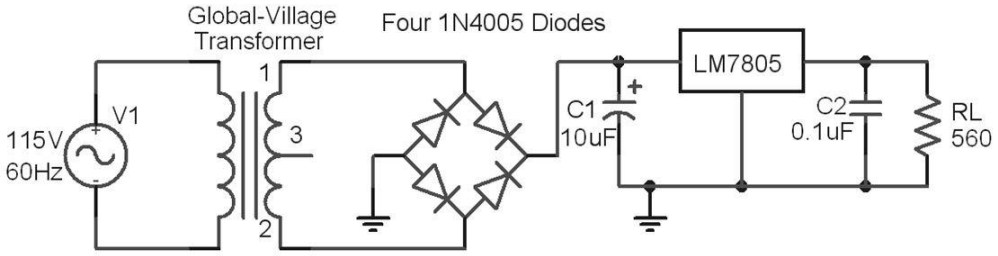


1. What is the peak voltage at the secondary of the transformer? _____ _____
2. What is the peak voltage at the output of the rectifier circuit? _____ _____ _____
3. What is the worst-case estimate for the ripple voltage across the load? _____ _____
4. What is the minimum voltage expected in the waveform seen across the load? _____ _____
5. What is the average voltage expected across the load? _____ _____ _____

Note: Normally, the filter capacitor would be larger and the load heavier (i.e. smaller resistor). However, for demonstration purposes and safety, the values above have been chosen. With these values, substantial ripple can be observed without overheating the load resistor in an actual circuit.

Regulated Power Supply

Use the schematic diagram below to predict the circuit characteristics that follow. Again, assume that the transformer turns ratio is 6:1 and that the diodes have a forward barrier potential of 0.7 V.



What is the expected average voltage seen at the load resistor? _____ _____

What is the expected average current passing through the load resistor? _____ mA

What is the expected ripple voltage seen across the rectifier filter capacitor, C1? _____ _____

What is the expected minimum voltage seen for the signal at the input to the LM7805? _____ _____

You have now completed the Pre-Lab. You may Save and Close or move on to the Lab Activity page, but do not "Submit" until you have completed the Lab Activity!

Question 2: (10 points)

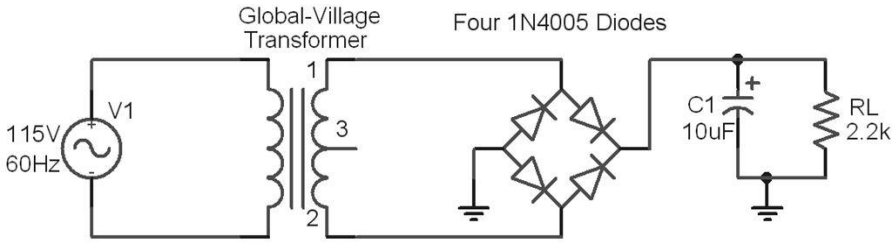
Lab 03 Activity

Note: Safety Glasses are required!

Filtered Bridge Rectifier Power Supply

Using the Global Village Transformer provided in class, build the circuit as shown.

- *Be careful to orient the 10 μF capacitor correctly!*
- *Do not connect the centre pin of the transformer to anything -- it must float in this configuration!*
- *Do not connect any of the pins on the secondary of the transformer to ground -- the secondary must float with respect to ground.*



Since the secondary of the transformer is floating with respect to ground, we can't display its signals directly with a single channel of an oscilloscope. Rather than showing you how to display the signal using both channels and the Math functions, we will concentrate on the output signal alone. (If you have time, you could ask your instructor for assistance in setting up and displaying a differential Math signal to display the secondary voltage.)

Use Channel 1 of the the Tektronix Oscilloscope to monitor the voltage across the load resistor. Move the Zero Marker (vertical Position) to the first graticule line above the bottom of the screen so you can maximize the Vertical Attenuation (Volts/Div).

Display two to five cycles of the output signal on the screen.

Locate the Trigger controls on your oscilloscope. Set the Source to Channel 1, the Type to Edge, the Slope to Rising; then move the Trigger Level so that its marker is within the upper and lower limits of the signal.

Now, using the Measure options, display the peak voltage, the minimum voltage, the period, and the ripple voltage.

Here are some tips on using an oscilloscope for measurements like these:

- Use HIGH and LOW instead of MAX and MIN, as the latter two include any noise spikes in the signal, generating unexpectedly high values occasionally
- Use AMPLITUDE instead of PEAK-TO-PEAK for the same reason; just remember that the correct unit for AMPLITUDE is $V_{p\text{-}p}$, unless you are measuring a unipolar (one polarity and zero volts as the two extremes).

Ask your instructor to grade your circuit and oscilloscope setup out of five marks. _____

Record the following, from your oscilloscope:

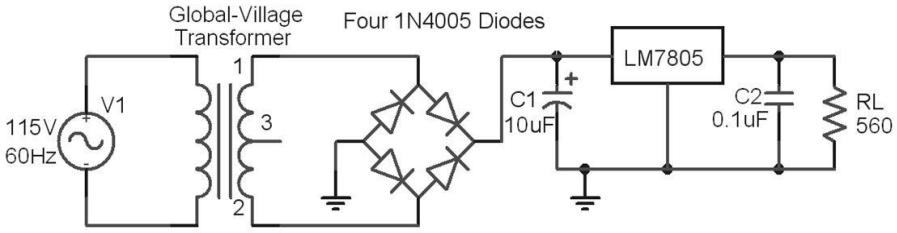
1. Peak voltage: _____ _____
2. Minimum voltage: _____ _____
3. Ripple voltage: _____ _____
4. Period: _____ ms
5. Average voltage: _____ _____
6. RMS voltage: _____ _____
7. We can tell that this signal is very close to being a true DC signal because _____ is very nearly the same as _____ .

9. Change the resistor value to 560 Ω. What is the Average Voltage now? _____ VDC
10. This change in the output voltage demonstrates poor _____

(Note: If you try this circuit in Multisim, your resistor may "burn out". Just restart the simulator.)

Regulated Power Supply

Modify your circuit, or start from scratch, to create the following.



Use Channel 1 of the oscilloscope to monitor the signal at the output of the rectifier (i.e. across C1) and Channel 2 to monitor the signal across RL. Set up your oscilloscope to display the Channel 1 signal optimally. Now, set up Channel 2 to have the same settings for quick signal comparison. From the Measure menu, display the following (remember to use the best measurement tools on the oscilloscope, not just the ones that match the terms below):

Channel 1 Peak voltage

Channel 1 Minimum voltage

Channel 1 Ripple voltage

Channel 1 Period

Channel 2 Average voltage

13. Ask your instructor to grade your circuit and oscilloscope setup out of five marks. _____

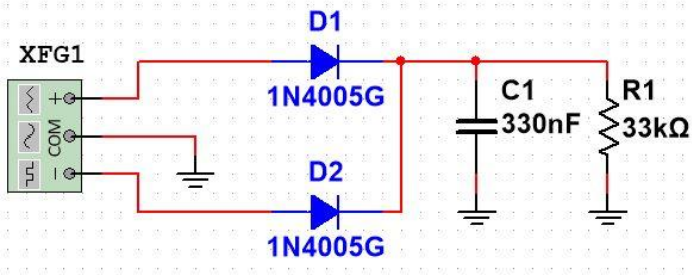
For the unregulated signal, record the following:

Peak voltage: _____ _____

14. Minimum voltage: _____ _____
15. Ripple voltage: _____ _____
16. Period: _____ ms
17. Place a Voltage Probe to monitor the regulated voltage across the load resistor. From this, record the following:
18. Average voltage: _____ _____
19. RMS voltage: _____ _____
20. From the Minimum voltage of the unregulated signal and the Average voltage of the regulated signal, determine the Overhead, or Dropout, voltage: _____ V

Simulation

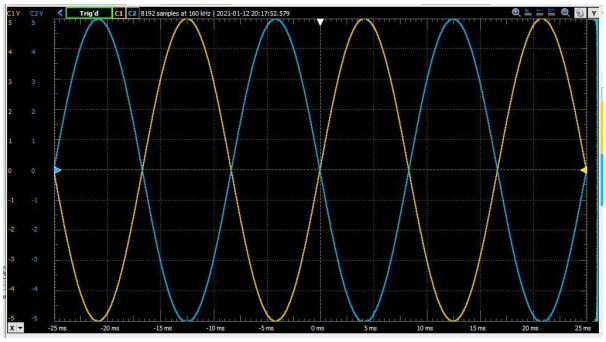
Using Multisim, build the following circuit, using the two outputs of a generic function generator as the '+' and '-' outputs of XFG1. Set the signal amplitude to 5.0 V_p and the frequency to 60 Hz.



(Note: In a typical circuit, the load resistor would be much smaller and the capacitor much larger. The values above were chosen in case you wanted to verify the circuit using two channels of the Analog Discovery 2 device as the two input signals, to reduce the loading on the Waveform generator.)

- Make sure you connect all grounds together
- Verify the orientation and connections of the two diodes

Start by checking your two input signals. Use the two oscilloscope probes to observe the two waveform channels. You should see the following, showing that the two signals are equal but opposite:



Now, move oscilloscope CH2 to the output of the rectifier, across R1. Verify, from what you know about the centre-tapped rectifier and filter, that the circuit output shape is what your expect. Measure and record the following, using the measurement menu items available. (As previously indicated, use "High" and "Low" rather than "Max" and "Min" in case there is noise on the signals.)

21. Peak voltage of the input signal: _____ V_p
22. Peak voltage of the output signal: _____ V_p
23. Minimum voltage of the output signal: _____ V
24. Ripple voltage of the output signal: _____ $V_{p\text{-}p}$
25. Average voltage of the output signal: _____ _____
26. Use a voltage probe to measure the RMS voltage of the output signal (Multisim's oscilloscopes don't calculate RMS properly): _____ V_{RMS}
27. Frequency of the input signal: _____ Hz
28. Frequency of the output signal: _____ Hz

Take a screenshot of the oscilloscope display, with all of the output signal values visible, and upload it here for a grade out of four marks. Do not use any spaces or special characters in your filename, but personalize it for easy identification as belonging to you. Document Upload (Direct)

You have now completed this Lab Activity. Once you submit your results, you will not be able to access this activity again.

Online Homework System

Assignment Worksheet
6/7/22 - 1:07:50 PM MDT

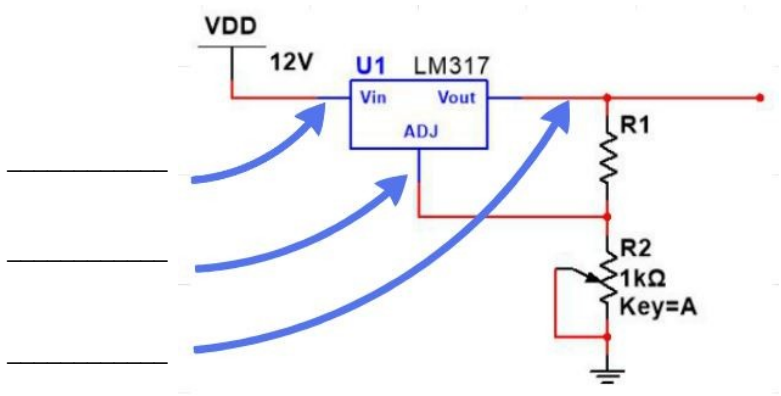
Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA05 Adjustable Regulator Activity

Question 1: (15 points)

DESIGN:

In this activity, we want to build a variable positive voltage regulator that provides a range of voltages from 1.25 V_{DC} to approximately 9.5 V_{DC}. The basic circuit is shown in the following schematic.

Start by checking the specifications for the LM317 and label the pins using the listbox beside the schematic.



_____
_____
_____

2. Make R_2 a 1 kΩ Potentiometer. Calculate a suitable resistance value for R_1 that will provide you with approximately 9 V_{DC} when the sweeper of the potentiometer is turned all the way to the bottom. Pick the closest value from your kit to use as R_1:

_____ Ω.

3. Using the value of R_1 that you picked, predict the voltage you would actually expect to see when the sweeper of the potentiometer is turned all the way to the bottom.

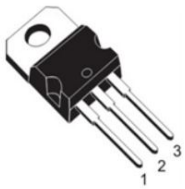
_____ V_{DC}

4. What voltage do you expect to see at the output when the potentiometer sweeper is turned all the way to the top?

_____ V_{DC}

BUILD:

Using a +12 VDC power supply (at home, you can use the +/-12 V PowerBRICK), the resistor value you chose for R_1, and the other components shown, build the circuit on your breadboard. Your adjustable regulator may be made by a different manufacturer, in which case it may be "LT" instead of "LM", or even some other designation; the "317" is what you're looking for. Be very careful with the pinout! On any TO220 package device, the pins appear as shown below:



TO-220

Use a single-turn 1 kΩ potentiometer to allow for quick changes in the output voltage.

Connect the output of your circuit up to your Digital Multimeter (DMM), and set it to display the output correctly.

Check to see if turning the potentiometer clockwise makes the voltage increase. If not, turn the potentiometer around (i.e. reverse the positions of pins 1 and 3, the two ends of the resistive element).

TEST:

5. Measure and record the minimum output voltage.

_____ V_{DC}

6. Measure and record the maximum output voltage.

_____ V_{DC}

7. Your work will be gradedout of seven marks. If you are completing the exercise at home, set the output voltage as near to 8.00 V as possible; arrange your circuit and your multimeter so you can take a picture of the circuit, your settings and the results; and upload the file here for your instructor to grade. Don't use any spaces or special characters in your filename, but personalize it for easy identification as belonging to you. In the lab, ask your instructor to grade your work.

Document Upload (Direct)

Online Homework System

Assignment Worksheet
9/26/22 - 12:33:54 PM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Project #1 1221

Question 1: (0 points)

This Project must be submitted for grading at the time specified by your instructor. You will be given some class time to work on it, and will be expected to do other work on your own time.

As this is a more formal assessment than the Lab activities, your intructor's involvement will be limited to clarification of the requirements and simple feedback on your work. This assessment is intended to show that you have a good grasp on the associated course outcomes, so please limit your interactions with others to points of clarification or improvement of your understanding of the material rather than working together to arrive at solutions.

The first part of this assessment will involve prep work and predictions regarding a circuit similar to what you will build in class, culminating in a simulation to demonstrate its operation. The second part will involve building and testing a real circuit, somewhat simplified, and will be graded primarily upon your technical skills of circuit building and use of test equipment.

Grading breakdown:

20% -- prep work and predictions

30% -- simulation schematic and results

50% -- circuit building and testing

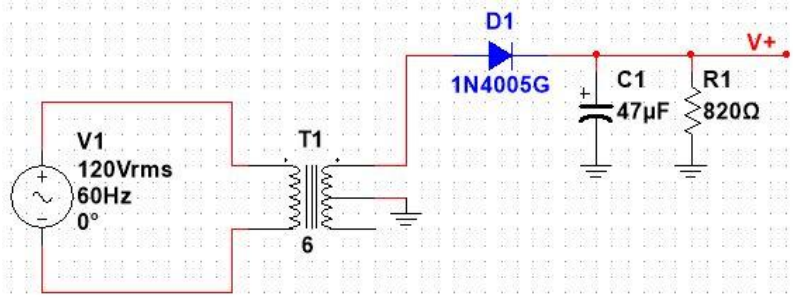
Question 2: (50 points)

NOTE: Once you submit this part of the project, you will not be able to return to it! Instead of moving on to the next question, you can save this if you intend to return to it later.

The "Printable Version" is also available for you to work through before submitting your answers, but the voltage indicated in the Printable Version for the Adjustable Regulator may not match what you have been assigned. Use the one assigned to you in your calculations.

Positive Supply, Unregulated

Consider the schematic diagram below when answering the questions that follow.



The transformer is the 6:1 centre-tapped Global Village transformer used in the lab.

Assume a diode voltage drop of 0.7 V throughout.

NOTE: The ground return is connected to the centre-tap, not to the bottom end of the transformer secondary!

1. Determine the peak voltage expected at V+ (i.e. across the load). _____ V_p
2. Determine the expected period of the ripple at V+, in milliseconds. _____ ms
3. Determine the worst-case expected ripple voltage expected at V+. _____ _____
4. Determine the worst-case expected average voltage expected at V+. _____ _____
5. Determine the worst-case minimum voltage expected at V+. _____ V

6. An actual circuit would demonstrate:

(a) Higher ripple, lower average, and lower minimum voltages than predicted.

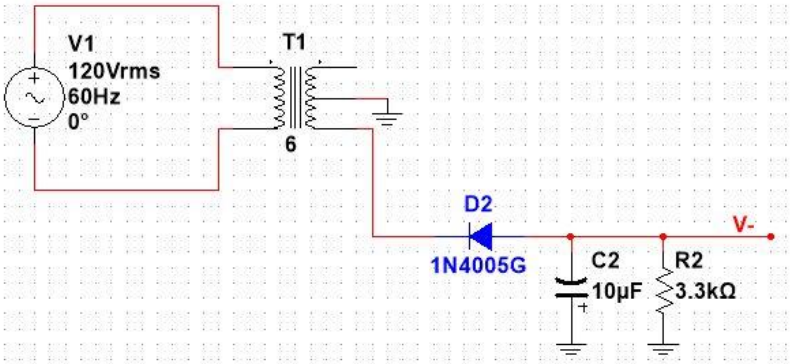
(b) Higher ripple, higher average, and higher minimum voltages than predicted.

(c) Lower ripple, higher average, and higher minimum voltages than predicted.

(d) Lower ripple lower average, and lower minimum voltages than predicted.

Negative Supply, Unregulated

Consider the schematic diagram below to answer the questions that follow.



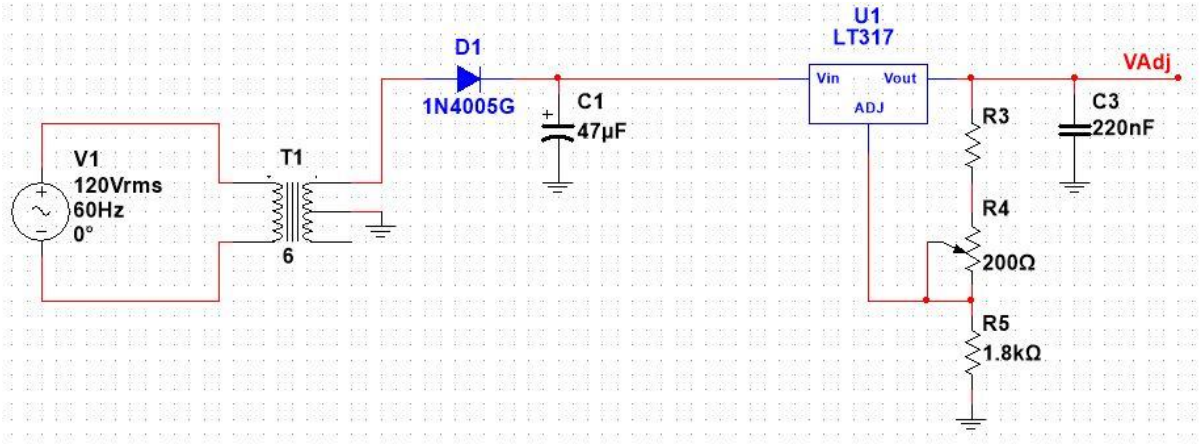
The transformer is the 6:1 Global Village centre-tapped transformer used in the lab.

NOTE: The ground return is again connected to the centre-tap!

7. Determine the peak voltage expected at V- (i.e. across the load). _____ V_p
8. Determine the worst-case expected ripple voltage expected at V-. _____ _____
9. Determine the worst-case expected average voltage expected at V-. _____ _____
10. Determine the worst-case "minimum" (i.e. the smallest negative) voltage expected at V-. _____ V
11. For this signal, the expected RMS voltage would be _____

Positive Supply, Adjustable

Consider the schematic diagram below when answering the questions that follow.



The transformer is the 6:1 Global Village centre-tapped transformer used in the lab.

The first part of this circuit is the same as the first circuit, but with the load resistor replaced by the LT317 circuit.

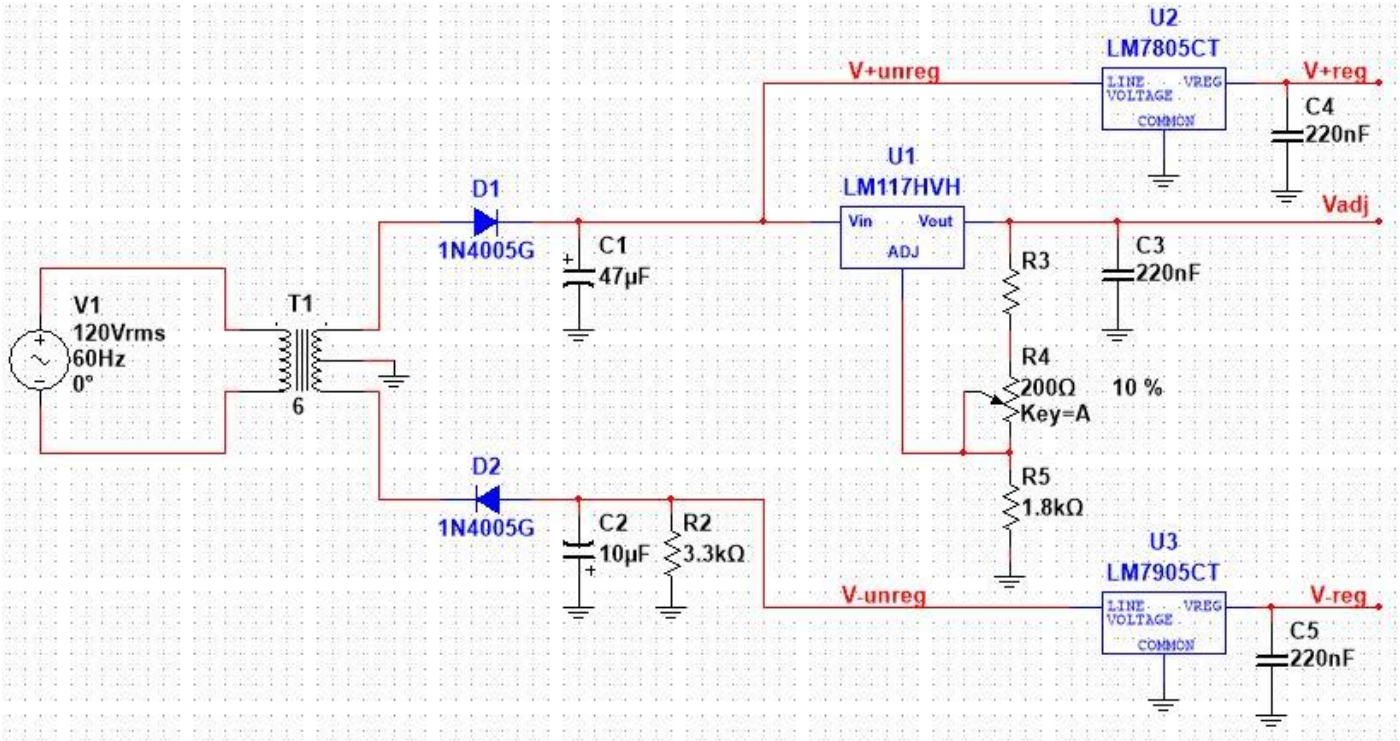
NOTE: The ground return is still connected to the centre-tap!

You have been randomly assigned an output voltage of 8 V from a selection of four possibilities. Use this value to find your answers.

12. In order to generate an output voltage of 8 V, what would be the ideal combined resistance for the resistors between Vout and Vadj? Provide your answer in ohms, not kohms. _____ Ω
13. Since R4 is a 200 Ω potentiometer, what is the biggest fixed resistor for R3, selected from the 10% resistor values available in your ETC Kit, that would allow for adjustment above and below the ideal resistance value? Provide your answer in ohms, not kohms. _____ Ω
14. Considering the "Load" to be the sum of the resistances in the properly-calibrated voltage-adjustment network, what is the expected load current? Provide your answer in milliamps, not microamps. _____ mA
15. What is the ripple voltage expected at the input to the regulator? _____ _____

Simulation -- Positive, Negative, and Regulated Supplies

Using Multisim, build and test the following circuit. Notes and further instructions are given below.



NOTES:

- You don't have to show the terminals or net labels seen in the schematic above -- they are given to help you with the analysis
- V1 is AC_POWER -- set its voltage and frequency appropriately
- T1 is TS_VIRTUAL from the BASIC_VIRTUAL library -- set its turns ratio appropriately

- C1 and C2 are CAP_ELECTROLIT
- LM117HVH is equivalent to the LT317 you've worked with in class
- R4 is a POTENTIOMETER from the "Basic" library -- set it to an increment of 0.1% for fine adjustment
- Use the R3 value needed to produce the voltage you were randomly assigned, 8 V

Construction and Testing

The recommended procedure for building and testing the circuit would be to build it in stages, as you have done in the circuit analysis above.

To test V+unreg by itself, you can load it with an 820 Ω resistor. Just make sure you remove this load resistor before adding the two regulators to the positive output, and record your answers for the completed circuit, not the preliminary test circut.

Once your circuit is complete, connect a Tektronix oscilloscope to the following places:

- Ch1 -- the top of the transformer
- Ch2 -- the bottom of the transformer
- Ch3 -- V+unreg
- Ch4 -- V-unreg

Also use probes to help you make and record the measurements below (most of the unit subscripts have been deliberately left off -- use the measurements you normally would for each of these).

16. Peak voltage at the top of the transformer: _____ V__
17. For V+unreg:
    1. Average voltage: _____ _____
    2. RMS voltage: _____ V__
    3. Ripple voltage: _____ _____
    4. Minimum voltage: _____ V__
    5. Frequency: _____ Hz
18. For V-unreg:
    1. Average voltage: _____ V__
    2. RMS voltage: _____ V__
    3. Ripple voltage: _____ V__
    4. "Minimum" voltage: _____ V__
19. For V+reg:
    1. Average voltage: _____ V__
    2. RMS voltage: _____ V__
20. For Vadj:
    1. Average voltage: _____ V__
    2. RMS voltage: _____ V__
    3. Overhead voltage: _____ V__
    4. If the ripple on the output of Vadj was 20 mV, what would the ripple rejection be, in decibels? _____ dB
21. For V-Reg:
    1. Average voltage: _____ V__
    2. RMS voltage: _____ V__

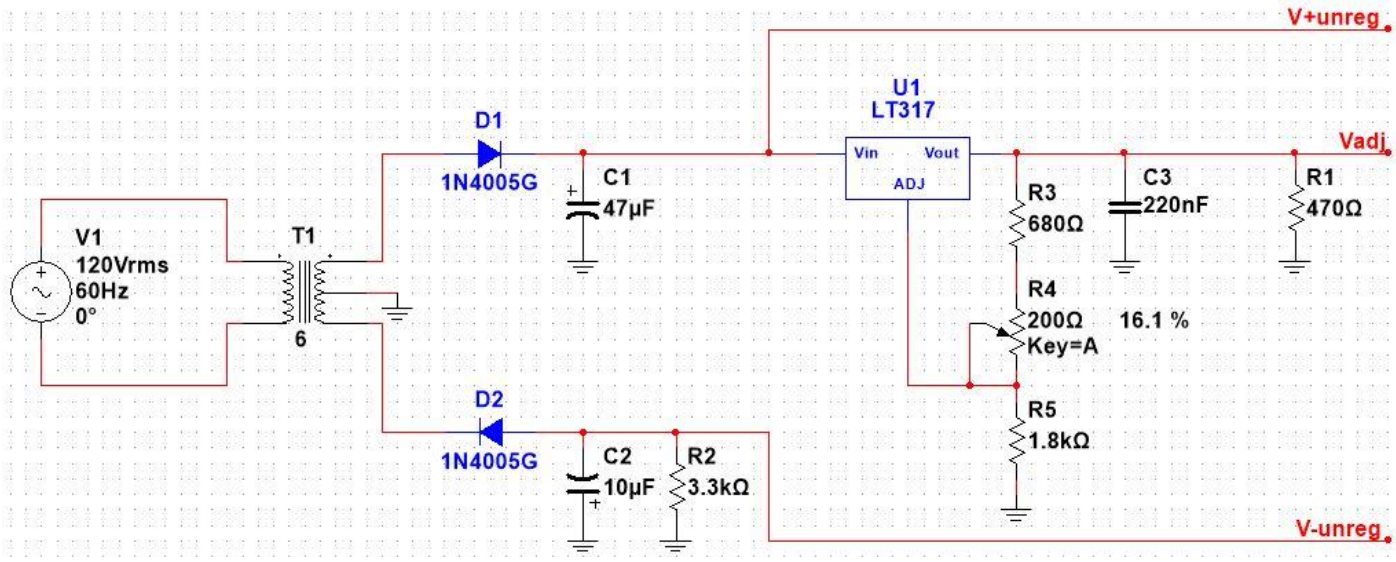
22. For a grade out of five marks, take a screen shot of your Multisim schematic and upload it here. Do not use any spaces or special characters in the filename, but make sure you personalize it so it's clear who it belongs to. Document Upload (Direct)
23. For a grade out of five marks, take a screen shot of your Multisim oscilloscope display. Make sure you've connected it and set it up as follows:

- Ch1 -- the top of the transformer
- Ch2 -- the bottom of the transformer
- Ch3 -- V+unreg
- Ch4 -- V-unreg
- The signal on Channel 1 should be maximized for proper viewing on the screen
- All the other channels should be set exactly the same as Channel 1, including the Zero Voltage Markers for each, for easy comparison of the signals.

  Upload your oscilloscope display screen shot here: Document Upload (Direct)

Question 3: (50 points)

On your breadboard, build the following circuit, and test it as indicated below.



NOTES:

T1 is the Global Village transformer used in previous exercises.

Pay careful attention to the orientation of the two electrolytic capacitors!

Make sure you wear your SAFETY GLASSES at all times

Make sure you use the correct pinout for the LT317. It doesn't match the arrangement on the schematic!

R4 is a multi-turn 200 Ω trim potentiometer. 

You may want to build this circuit in stages -- V+unreg first (in which case you might want to temporarily attach an 820 Ω load resistor, but make sure you remove it when you move on), V-unreg second, and Vadj last.

Once you have the circuit built and operating, adjust Vadj to be as close as possible to 4.00 VDC.

Now, use your oscilloscope to make and record the following measurements:

1. Peak voltage at the top of the transformer: _____ V_p
2. Peak voltage at V+unreg: _____ V_p
3. Average voltage at V+unreg: _____ _____
4. Ripple voltage at V+unreg: _____ _____
5. Average voltage at Vadj: _____ V__
6. Average voltage at V-unreg: _____ V__
7. Ripple voltage at V-unreg: _____ _____

Ask your instructor to inspect your circuit for a grade out of ten marks: _____

Ask your instructor to inspect your oscilloscope screen and settings for a grade out of five marks: _____

You have now completed this project. Once you submit your work, you will not be able to return to this page!

Online Homework System

Assignment Worksheet
5/20/22 - 9:27:20 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Bipolar Junction Transistors (BJT)

Question 1: (1 point)

Bipolar Junction Transistors (BJT)

The diode opened up a world of possibilities by being able to respond very differently to different circuit conditions -- conducting when forward biased and not conducting when reverse biased. The transistor takes that about an order of magnitude farther, because transistors can be externally controlled, and can provide a range of responses rather than just "on" (with a small voltage drop) and "off".

There are a number of different transistors -- to begin with, there are BJTs and FETs (next topic, and there are three main families of FETs). Then, in each group there are P-type and N-type devices. So, this isn't going to be quite as straightforward as diodes!

Introduction to Amplification

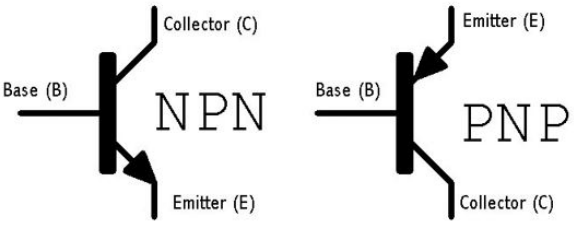
Transistors are designed for current amplification, which can be turned into voltage amplification and power amplification. Amplification means to turn a small signal into a large one. Clearly, that can't be done without the input of energy from outside the device. A transistor can be seen as a device that can "read" a small incoming signal and control a large external power source to produce a large output signal. Without the external power source, nothing happens.

It's like making a car move. You push down on the accelerator with just your foot, and the massive vehicle surges ahead -- but only if the engine is running. No power source, no response -- your foot didn't do the work; the engine did, but at the command of your foot.

BJTs respond to a very small input current by producing a much larger output current, if there's a DC power supply connected.

Transistors are three-pin devices: The big current from the power supply goes through two of the pins, and the third pin provides the control.

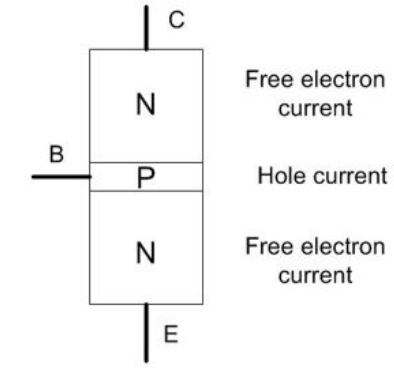
The schematic symbols for the two flavours of BJT are shown below.



In each of these, a large current can flow through the Collector-Emitter path, controlled by a small current injected at the Base. Notice the difference in the way the pins are drawn: The Collector and Emitter are drawn in-line with each other to show the primary current path, whereas the Base is off to the side to provide control. Also, the Emitter always has an arrow on it to show the direction of conventional current, whereas the Collector has no arrow.

Without getting into too much Quantum Physics, here's a brief explanation as to how the NPN version of the BJT works from the perspective of conventional current, and a similar explanation holds for the PNP, but from the point of view of electron current.

Picture the NPN transistor as three blocks of semiconductor material.



This transistor is called "bipolar" because it uses both hole and free electron current in order to conduct.

In its natural state, there are two P-N junctions, and therefore two barrier potentials to deal with.

Transistors are always biased so that the Base to Collector junction (B-C junction) is reverse biased. This naturally prevents the flow of current, so a BJT at rest doesn't conduct. In the case of the NPN, this biasing arrangement means that the Collector voltage, V_C, will always be the at the highest potential of the three, with the Emitter at a lower potential so current can flow from the collector to it. In the case of the PNP, V_C is always the lowest voltage and V_E is always the highest voltage.

The Base to Emitter junction is the one we control. If the B-E junction is not forward biased, the transistor does not conduct (unless you blast it with a higher external voltage than it can handle -- more on that later). When the B-E junction is forward biased, the amount of current flowing through it directly determines how much current flows from the Collector to the Emitter and out. This happens, roughly, because the layer of "P" material connected to the Base is really thin, and when current flows from Base to Emitter, it "erodes" the B-C junction, allowing current to cross over. The more Base current, the deeper the "erosion", and therefore the more current flows from the Collector.

This means that both the current from the Collector, I_C and the current from the Base, I_B end up flowing into and through the Emitter, so that $I_E = I_C + I_B$. Since the Base current is relatively tiny, I_C and I_E are pretty similar, with I_E being just a tiny bit bigger.

By the way, we don't make transistors by "attaching" three blocks of semiconductor material together. We start with a layer called the Substrate, say N material in the NPN transistor, sputter a thin layer of P material onto that, then sputter another layer of N material onto that. Next comes a metallization layer that allows us to make physical connections to the transistor. As a result, we can make these things so tiny that an Apple A13 microprocessor has 8.5 billion of them in a single layer in the area of about the size of your fingernail! These transistors are on the order of 7 nm in size!

Another thing to know is that the material used in the Collector is a bit different from the material used in the Emitter. The Emitter material is very heavily doped, the Collector material is heavily doped but not like the Emitter, and the Base material is lightly doped. So it matters which end is the Emitter and which is the Collector.

BJT Relationships

The BJT is, as mentioned, a Current-Controlled Current Source. A tiny Base current controls a large Collector current, and the two combine to produce the Emitter current.

$$I_E = I_C + I_B$$

The current gain, given the symbol β, tells us how much bigger the useful current -- usually I_C -- is than the controlling current, I_B.

$$\beta = \frac{I_C}{I_B}$$

or, more often this is written as $I_C = \beta I_B$

Sometimes β is referred to in a different system of "h-parameters" as h_{FE}. This is the only h-parameter you'll see in this course, but watch for it and remember that it's the same as β.

The efficiency of the device, given the symbol α, compares the total current to the useful current.

$$\alpha = \frac{I_C}{I_E}$$

This will always be slightly less than one, or, if we were to consider it in percents, less than 100%. (We actually don't ever convert it to percents, but this might help you remember it can't be greater than one.)

Since α and β are based upon the same current values, they are related to each other. If you want, you can do the math to prove these:

$$\alpha = \frac{\beta}{\beta+1}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

Time to play with the mathematical relationships.

A particular NPN transistor has a measured Collector current of 10.896 mA and a measured Emitter current of 11.205 mA.

1. What is the Base current, in microamps? _____ μA
2. What is α, to four decimal places? _____
3. What is β? _____

A PNP transistor has a current efficiency of 0.9965 and a measured Base current of 560 μA.

4. What is β? _____
5. What would the Collector current be, in milliamps? _____ mA
6. What would the Emitter current be, in milliamps? _____ mA

An NPN transistor has a current gain of 375 and a measured Base current of 220 μA.

7. What is the current efficiency, α, for four decimal places? _____
8. What would you expect the Collector current to be. in milliamps? _____ mA
9. What would you expect the Emitter current to be? _____ mA

Standard Transistor Nomenclature

Voltages

- Any singly-subscripted voltage (e.g. V_C, V_E, V_B) is the voltage at the labelled pin referenced to ground.
- Any doubly-subscripted voltage (e.g. V_{CE}, V_{BE}) is the voltage at the first labelled pin referenced to the second labelled pin. Mathematically, $V_{BE} = V_B - V_E$ and $V_{CE} = V_C - V_E$
- Any doubled subscript (e.g. V_{CC}, V_{BB}, V_{EE}) indicates an external power supply that powers a particular pin, either directly or indirectly. These power supplies are also referenced to ground.

Currents

The currents are labelled according to the pin they are flowing through: I_B, I_C, and I_E. When we draw an arrow on a diagram to indicate our intention in terms of the direction of current flow, we can simply use positive numbers.

However, on a lot of specification sheets, you will see positive and negative currents shown. The convention is this: If the doubly-subscripted voltage driving the current is negative, the current will be negative. So, for example, if V_{CE} is actually negative (V_E is more positive than V_C), then I_C will also be negative.

Since PNP transistors have their Emitters more positive than the Bases and Collectors, their standard V_{BE} and V_{CE} voltages will be negative, and so will be their I_C and I_B currents.

Biasing Resistors

Often, we use letter representations for the resistors that provide current limit or voltage referencing for the pins: R_C, R_E, and R_B. If more than one resistor is used in biasing a pin, they will be designated with a number in the subscript: R_{B1}, R_{B2}, R_{E1}, or R_{E2}.

BJT Modes of Operation

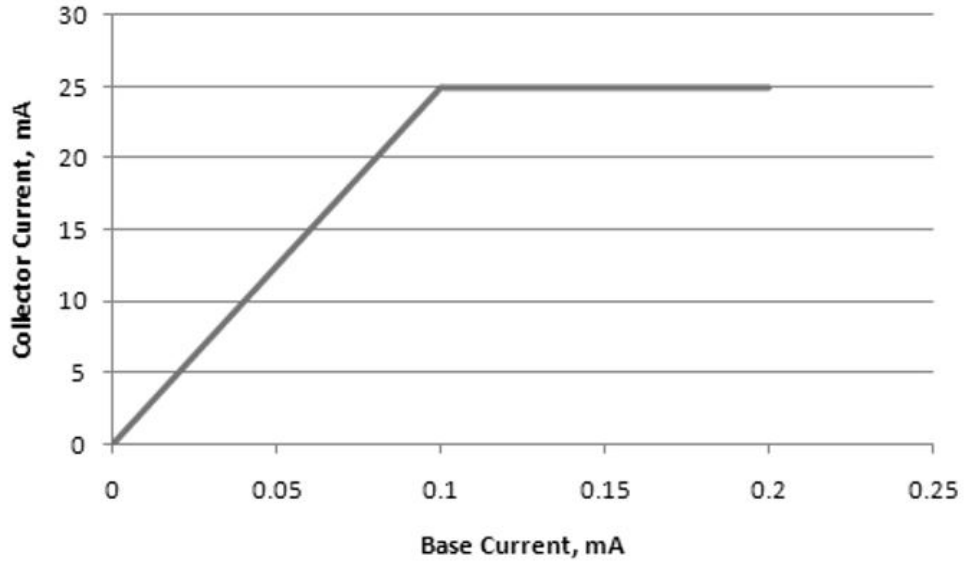
Like diodes, BJTs operate differently depending on the electrical conditions they are exposed to. The following terms describe the four most important conditions for BJTs.

1. ***Cut-off*** -- in this condition, the transistor does not conduct. The B-E junction is not forward biased, so there is no current between the Collector and the Emitter.
2. ***Active Mode*** -- in this condition, an increase in Base current results in an increase in Collector current, in the linear relationship defined by $I_C = \beta I_B$. Consequently, this is also called the ***Linear Active Region***.
3. ***Saturation*** -- In this condition, the transistor has reached the maximum current that can be supplied for the given circuit, and any further increase in Base current has no effect on the Collector current. In this condition, the voltage drop across the transistor from

Collector to Emitter (V_{CE}) is reduced very nearly to zero, and is called V_{CEsat}.

4. ***Reverse Breakdown*** -- like any insulator, the reverse-biased C-B junction can be forced to conduct with a high enough potential. Above the Reverse Breakdown voltage, the transistor will conduct with a similar tiny internal resistance as it would have in Saturation, and with significant current flowing as driven by a large voltage, the power will be significant and will likely result in Thermal Destruction.

The following graph shows the Transfer Characteristic (relationship between input current and output current) for a particular NPN transistor, and shows the first three of the conditions described above.



10. Use your mouse to identify the Cut-off Region.

null

11. Use your mouse to identify the Saturation Region.

null

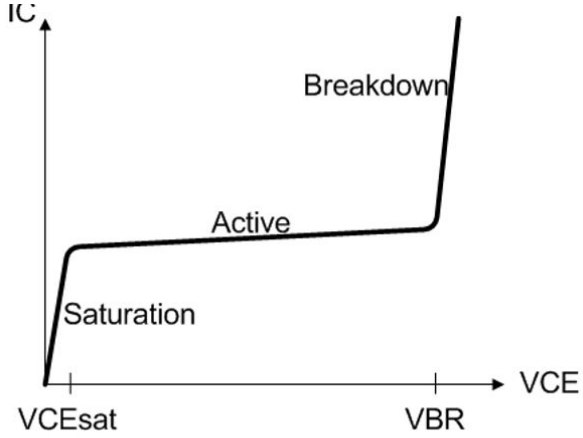
12. Use your mouse to identify the Active Region.

null

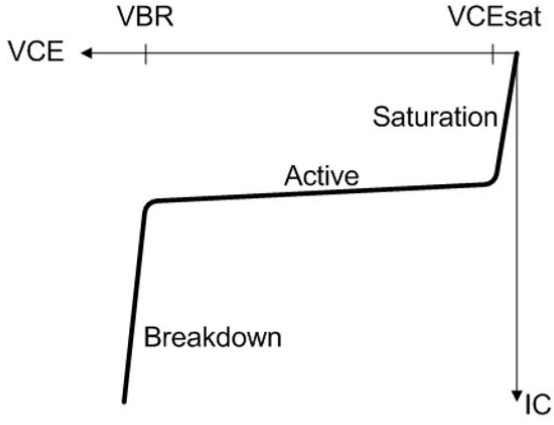
13. What is β in the Active Region? _____
14. Does this value of β apply in the Saturation Region? _____

BJT Characteristic Curves

When testing transistors, a piece of equipment called a ***Curve Tracer*** generates a display indicating how the transistor responds to changes in electrical conditions. The curve tracer applies a constant Base Current, then increases the voltage across the transistor, V_{CE}, to show how the transistor responds. For a single run, the following traces would be typical.



NPN Characteristic Curve



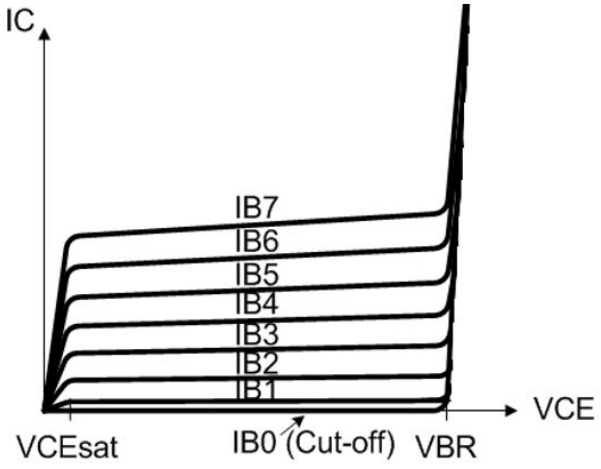
PNP Characteristic Curve

Notice that, for the NPN, V_{CE} and I_C are both positive, whereas for the PNP they are both negative, in keeping with the previous discussion.

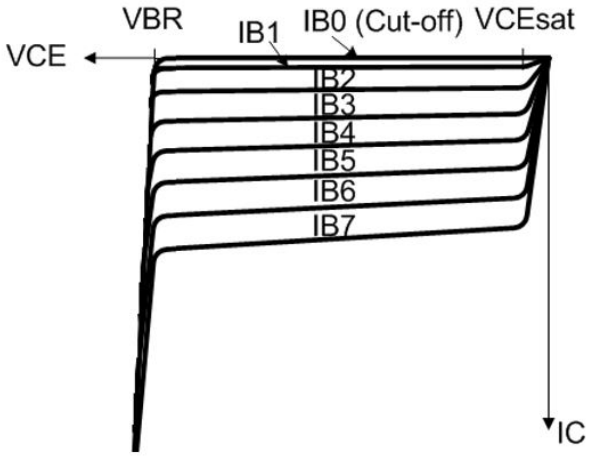
Here are some salient points to be made from these traces:

- In the Active region, I_C is very nearly constant. That's because the Base current is constant in this test, so we would expect $I_C = \beta I_B$. The fact that the line rises slightly as the voltage is raised across the transistor means that there is a large but not infinite internal impedance for this device. In other words, it is very nearly an Ideal Current Source, but not quite, because its current is affected by voltage. The flatter the line, the larger the internal impedance.
- In the very small region prior to entering the Active region, the transistor is allowing whatever current the supply can allow to flow through it. In other words, here it behaves as though it had a very small internal impedance, something you would expect from an Ideal Voltage Source. However, again the line is not straight up as it would be for a truly ideal voltage source. A transistor that allows any available current to pass through it is in Saturation.
- Related to the above discussion, notice that V_{CEsat} is a very small number, usually even smaller than it appears on this diagram.
- Beyond the Reverse Breakdown Voltage, V_{BR}, the transistor again conducts as with a small internal resistance, and the current rises rapidly, very likely leading to Thermal Destruction.

In reality, the Curve Tracer can be set up do draw a number of traces, each for a different constant Base Current. The following shows the "Family of Curves" produced.



NPN Family of Curves



PNP Family of Curves

Here, you can see that as I_B increases, I_C also increases. And, since the spacing between the curves is essentially constant, the relationship between I_B and I_C must be fairly constant.

In addition, we now can see all four of the transistor conditions:

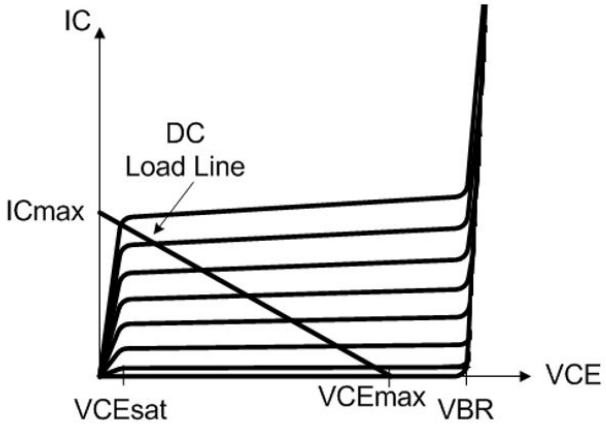
- The I_{B0} curve shows that with no Base current in, there is no Collector current out -- the transistor is not conducting, and is in ***Cut-off***.
- When the transistor is conducting freely with only a tiny voltage drop across it, it is in ***Saturation***.
- Once the transistor begins to act as a Current source, the output is linearly related to the input, so it is in the ***Active Region***.
- When the voltage exceeds the transistor's ability to control the current, the transistor enters ***Reverse Breakdown***.

DC Load Line

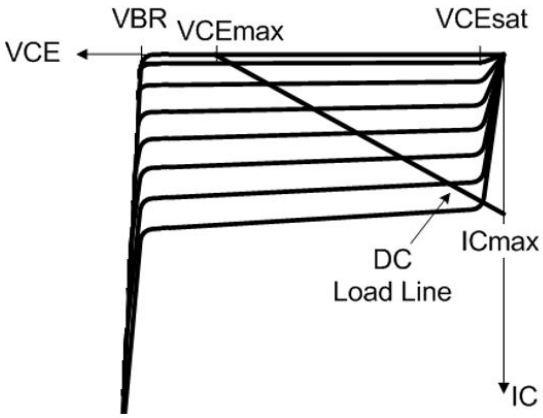
We're going to do one more thing to this set of graphs. As you will soon be learning, the power supplies and resistors used to bias the transistor in a circuit also define limits on what the maximum current through the circuit can be and what the maximum voltage across the transistor can be.

When the transistor is not conducting at all, the maximum Supply Voltage will appear across it, and no current will flow through it. That defines the Cut-off conditions for the circuit.

If we consider the tiny voltage across the transistor as negligible, we can determine the maximum current through the circuit based upon the resistors only, This defines the ideal Saturation conditions for the circuit. And, since the relationship between I_B and I_C is considered to be constant, we can draw a straight line between these two endpoints and call it the DC Load Line. For the circuit as wired, this DC Load Line defines all the possible values for I_C as controlled by I_B and their corresponding values of V_{CE}, or the voltage across the transistor in that circuit.



NPN Curves with DC Load Line



PNP Curves with DC Load Line

Question: In a particular circuit, an NPN transistor is powered by V_{CC} = 20 V_{DC}, and the transistor is biased by a 1.0 kΩ R_C resistor.

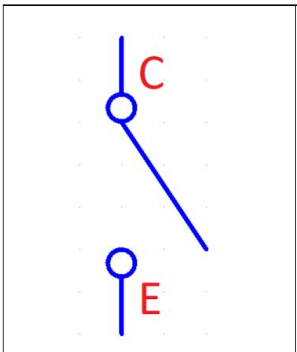
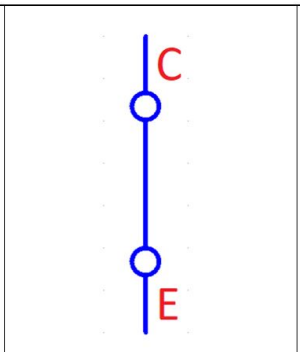
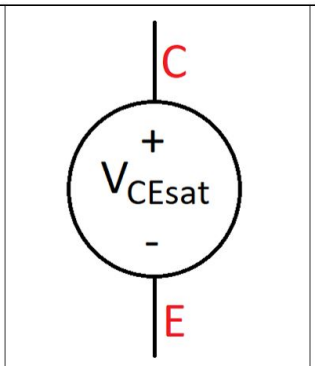
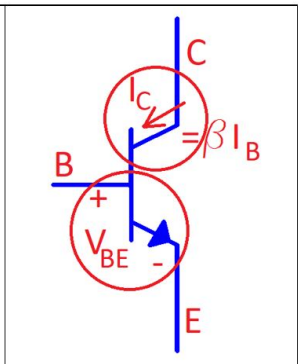
15. What is V_{CEmax}? _____ V
16. What is I_{Cmax}? _____ mA
17. When I_C = 10 mA, what do you expect V_{CE} to be? _____ V

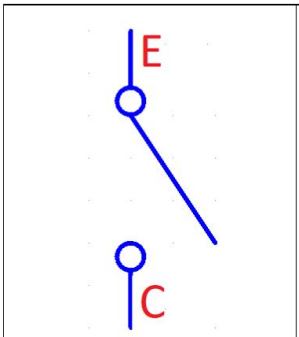
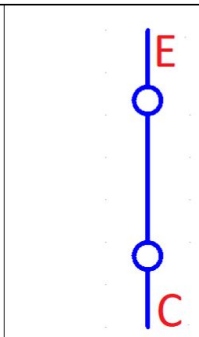
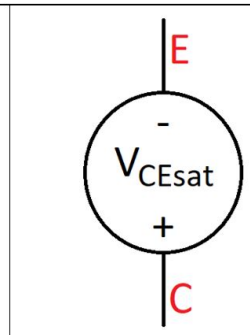
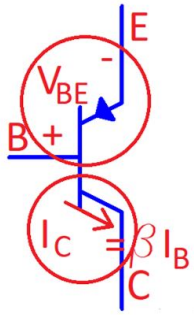
Now that we've done all the hard work on figuring out how transistors behave, it's time to create some simple models to help us predict how they will respond in different circuits

Question 2: (1 point)

BJT Models

Since transistors are fairly complex devices with lots of characteristics we haven't discussed (temperature dependency, internal capacitance, saturation storage time, differences in DC and AC characteristics, etc.), there are quite a few models around. This author has developed his own models to help with a basic understanding of transistors to help predict reasonably accurately how they will behave in the circuits you are likely to encounter. You won't see these models in any other textbooks.

			
NPN Cutoff	NPN Saturated, Ideal	NPN Saturated, Practical	NPN Active

			
PNP Cutoff	PNP Saturated, Ideal	PNP Saturated, Practical	PNP Active

These models help with the analysis of DC biasing circuits for transistors.

Since there are three distinct modes of operation, there are three distinct models -- Cut-off, Saturation, and Active. There are times when the small voltage drop for a saturated transistor is significant, so we have two saturation models -- Ideal and Practical.

Cut-off should be the easiest one to spot and to use. If there is no way of generating Base current, there will be no Collector current, and the transistor will behave as an open in the circuit -- hence the open switch model.

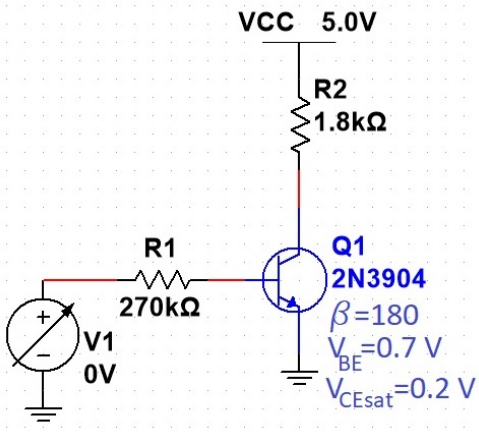
Saturation isn't as easy to spot, but it's fairly easy to use. It's analysis is essentially like that of a forward-biased diode, except that V_{CEsat} is typically much smaller than the diode's barrier potential.

Active -- in the Active region, the transistor is treated as an Ideal Current source, in which $I_C = \beta I_B$. If we can determine I_B we can analyze the output. To help us determine I_B, the model reminds us that there is a forward-biased P-N junction between the Base and the Emitter when the transistor is conducting. The only other thing to remember is the the Collector current and the Base current combine to become the Emitter current.

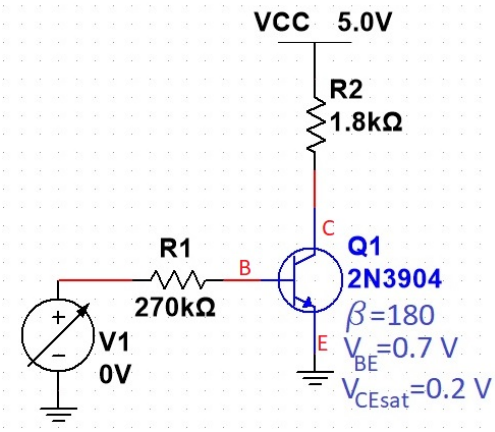
The problem comes in trying to determine if a transistor that's conducting is in the Active mode or in Saturation. The best we can do to distinguish these is to analyze the circuit as if it were in the Active mode, and if the answers don't make sense (i.e. if they go off the Saturation end of the DC Load Line), then the transistor must be saturated; throw away the Active model results and use the Saturation model instead.

Here are a few worked examples and questions to get you used to applying these models.

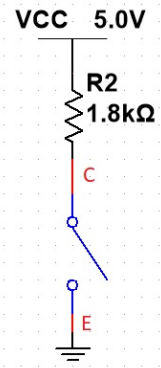
We'll start with an easy one.



Always start by labelling the pins on the transistor -- this will prevent you from confusing the Collector and Emitter if you're in too much of a hurry.



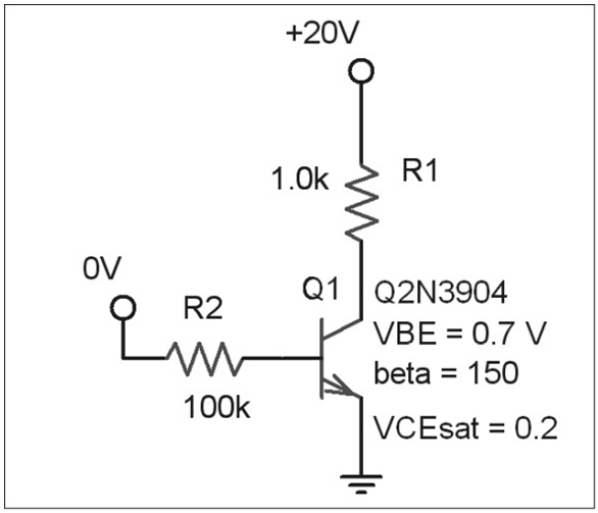
The first thing to notice about this circuit is that V_{BB} = 0 V and the Emitter is grounded. With no potential difference between these two voltages, there is no chance of current flowing through R1. This means that the transistor is in Cutoff. We immediately replace the transistor with the Cutoff Model, and proceed.



From this, we can answer all the necessary questions about this circuit:

- I_B = 0 mA (that was the basis for choosing this model)
- I_C = 0 mA (open switch)
- I_E = 0 mA (I_C + I_B)
- V_B = 0 V (no drop across R_B because there's no I_B)
- V_E = 0 V (connected directly to ground)
- V_C = 5 V (no drop across R_C because there's no I_C)
- V_{CE} = 5 V (V_C - V_E)

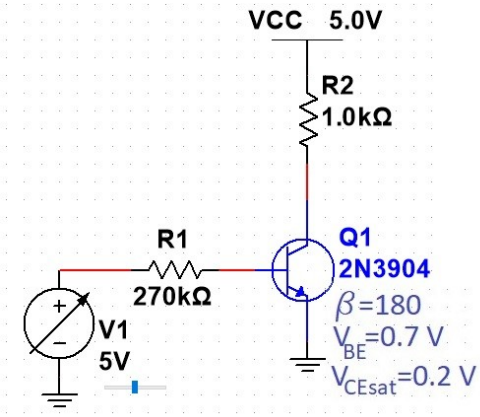
Give it a try!



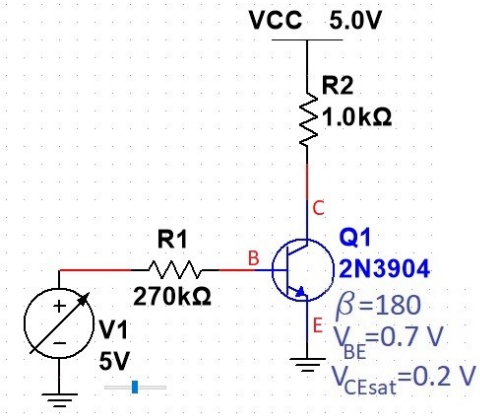
1. Is it possible for current to flow from V_{BB} to V_{EE}? _____
2. What condition is this transistor in? _____ Draw the appropriate model before answering the following questions, and label the transistor pins.

3. If no current is flowing through R_C, what is V_C? _____ V
4. What is V_E, by inspection? _____ V
5. Therefore, what is V_{CE}? _____ V

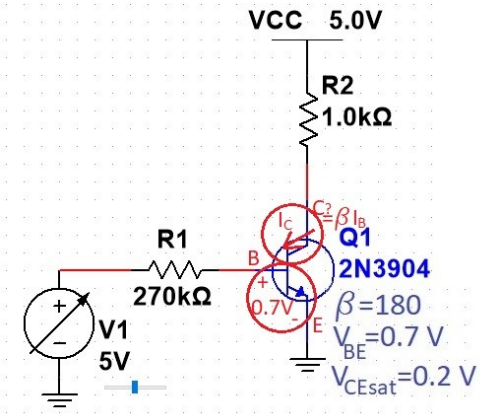
Here's another example.



Again, start by labelling the pins.



This time, V_{BE} is higher than V_{EE}, so current will flow through the forward-biased B-E junction. Since the transistor isn't in cutoff, we start with the Active Model, but keep an eye open for indications that it may not be the correct model. Notice the question mark over the '=' sign -- put it there to remind yourself that this may not be the right model.



The Current Source in the Collector is a good thing -- ideal current sources have infinite internal impedances, so, for all intents and purposes, the circuit involving the Base and Emitter is isolated (effectively disconnected) from anything on the Collector side of the circuit. That means we can just use KVL to determine what the Base current will be:

$$I_B = \frac{\Delta V_{R_B}}{R_B}$$ = (5 - 0.7)/270 kΩ = 15.9 μA

Now, we can use the transfer function to determine what Collector current is predicted using the Active Model:

$I_C = \beta I_B$ = 180*15.9 μA = 2.87 mA

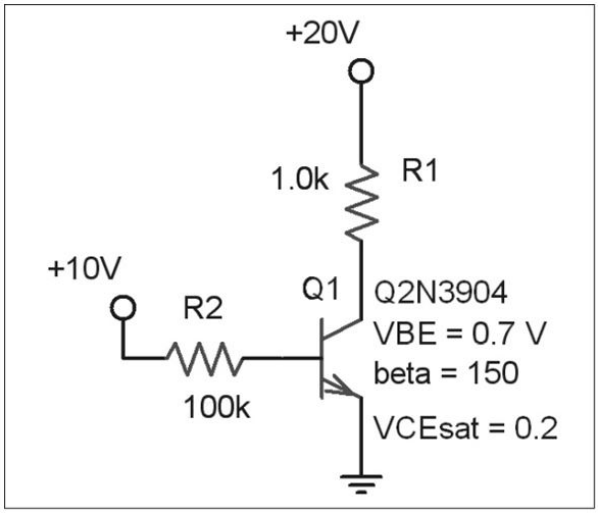
We're still not sure if this is the correct model, but we can check now. The maximum current that could flow in this circuit would exist if the transistor was completely shorted. In this case, the entire V_{CC} would appear across R_C:

$$I_{Cmax} = \frac{V_{CC}}{R_C} = 5.0/1.0\ k\Omega = 5.0\ mA$$

Since the predicted I_C is less than the maximum I_C, the model has predicted a reasonable value. Therefore, the Active Model was the right choice. We'll continue on with the analysis. We now have enough information to determine all of the characteristics of this circuit:

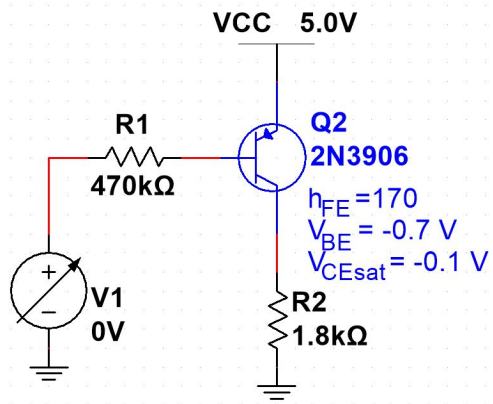
- V_E = 0 V (connected to ground)
- V_B = 0.7 V (V_E + V_{BE})
- V_C = V_{CC} - $I_C R_C$ = 2.13 V (**watch this one! Make sure you're clear that V_C is referenced to ground!)
- V_{CE} = 2.13 V (V_C - V_E)
- I_E = 2.89 mA (I_C + I_B)

Your turn.

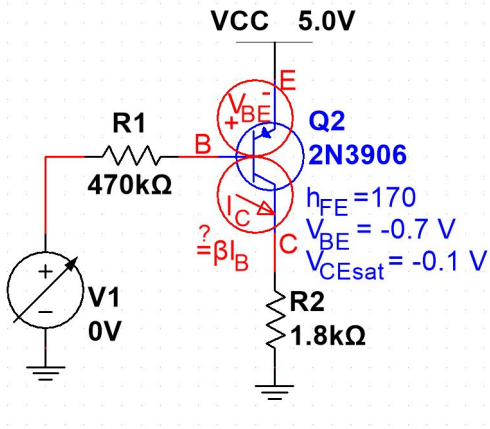


6. Is it possible for current to flow from V_{BB} to V_{EE}? _____
7. Following the discussion above, draw the model needed to continue the analysis of this circuit. What would the voltage at the Base, V_B, be? _____ V
8. What current would flow through the Base resistor? _____ μA
9. What does the model you've chosen predict as the Collector current? _____ mA
10. If the transistor was shorted (0 V drop), what is the maximum current that could flow through R1? _____ mA
11. Has the model you chose predicted a possible result for the Collector current? _____
12. Assuming your answer was "Yes", what voltage drop would appear across R_C? _____ V
13. What, then, would the Collector voltage be? _____ V
14. What would V_{CE} be? _____ V
15. Looking back, what condition is this transistor in? _____

Let's try a couple with PNP transistors.



Notice that V_{BB} is considerably less than V_{EE}, (make sure you know which pin is the Emitter -- label them right away, as in the diagram below) so current can flow through the forward-biased Emitter to Base junction. Therefore, the transistor is not in Cutoff, so we'll start with the Active Model, again checking to see if anything we discover indicates otherwise. In the following diagram, the labels have been added and the Active Model has been drawn over the transistor. Notice that the Emitter is at the top -- that establishes all the relationships we will be investigating. Also notice the use of h_{FE} -- that's just β.



Notice that the power supply is labelled "V_{CC}". It should, strictly speaking, be "V_{EE}", because it's powering the Emitter. However, in a schematic package, it's not possible to use different labels for the same power supply, so, if other components in the circuit are using "V_{CC}", we have to live with it even for PNP devices.

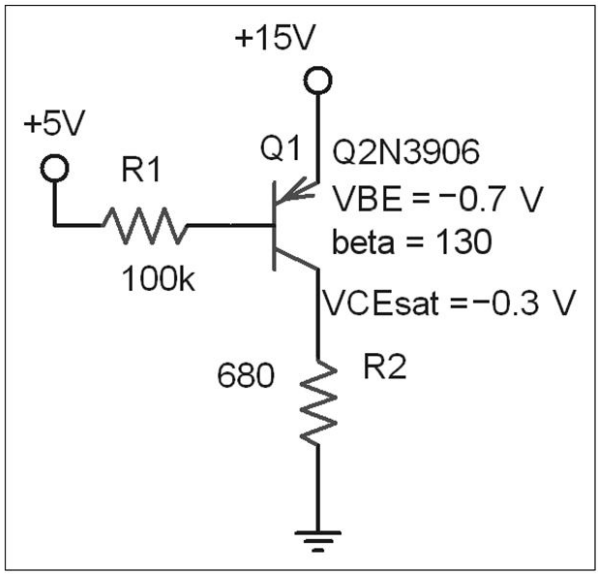
The negative sign on V_{BE} indicates that the Base voltage is below the Emitter voltage. That also shows up in the orientation of the signs in the V_{BE} symbol in the model. All it means is the Base voltage is less than "V_{CC}",or maybe better put, less than "V_E".

- V_E = 5.0 V (directly connected to "V_{CC}")
- V_B = 4.3 V
- $I_B = V_B/R_B$ = 9.15 μA (R_B is connected to ground, so V_B appears across it)
- I_C is predicted to be 1.56 mA by the Active Model. It's time to check to see if this is the right model.

If the transistor was completely shorted, we'd be left with 5.0 V across R_C, so I_{Cmax} = 5/1.8 kΩ = 2.78 mA. So, since the Active Model predicted a current that's less than the maximum current, that's a reasonable result, confirming that the Active Model is the right choice. So we can continue with the results we've gotten so far.

- $V_C = I_C*R_C$ = 2.80 V (R_C is connected to ground this time, so V_C appears across it in this example)
- $I_E = I_C + I_B$ = 1.56 mA (rounds to the same value as I_C because β is so big)
- $V_{CE} = V_C - V_E$ = -2.2 V (because the Collector voltage is less than the Emitter voltage)

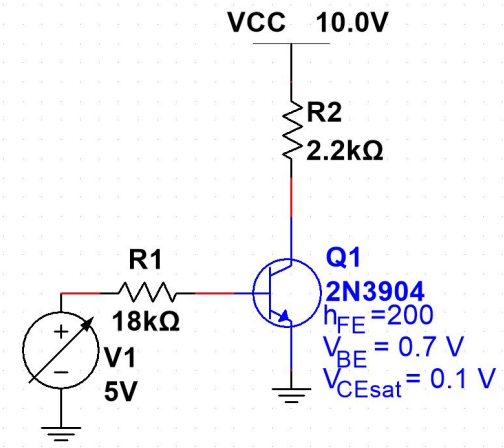
Your turn again.



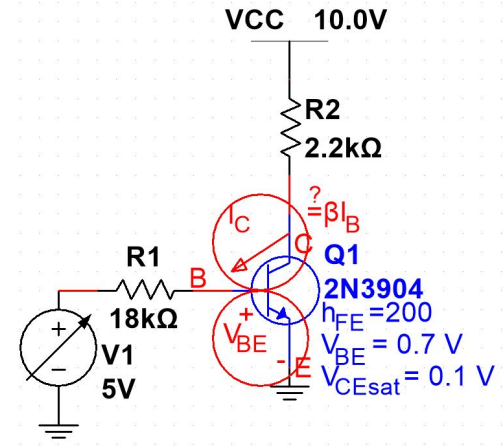
16. Is it possible for current to flow between V_{BB} and V_{EE}? _____
17. If so, in which direction? _____
18. Replace the transistor with the appropriate model, and determine the magnitude of I_B. _____ μA

19. What does your chosen model predict for the magnitude of the Collector current? _____ mA
20. Which direction does the Collector current flow? _____
21. If the transistor were shorted out, what is the maximum current that could flow in the circuit? _____ mA
22. Is the Active Model the correct choice? _____
23. What is V_E?_____ V
24. What is V_B? _____ V
25. What is V_C? _____ V
26. What is V_{CE}? _____ _____ V
27. What is the magnitude of I_E? _____ mA
28. Looking back, what condition is this transistor in? _____

So far, the examples have been either in Cutoff or in the Active Linear Region of operation. Let's check out the following circuit.



To begin, V_{BB} is higher than the Emitter voltage, so current can flow. That means it's not in Cutoff, so we start with the Active Model, again keeping in mind that it might be the wrong model.



We can get some of the basics down right away:

- V_E = 0 V (connected to ground)
- V_B = 0.7 V (V_E + V_{BE})

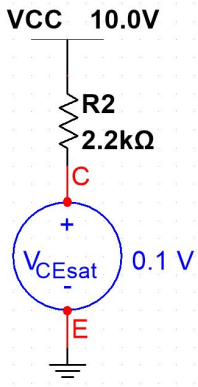
Using KVL, we determine I_B:

- $I_B = \Delta V_{RB}/R_B$ = (5 - 0.7)/18 kΩ = 239 μA

Now we move over to the collector side, and check to see if the prediction made by the Active Model makes sense:

- The model says $I_C = \beta I_B$ = 47.8 mA
- I_{Cmax} = 10 V/2.2 kΩ = 4.55 mA

The Active Model is clearly wrong, because it predicted a current that's much higher than the maximum current that could flow in this circuit. So, we toss out the Active Model and use the Saturated Model instead. For this course, we'll usually use the Practical Model, but in the future, you'll probably discover that the Ideal Model is usually good enough.

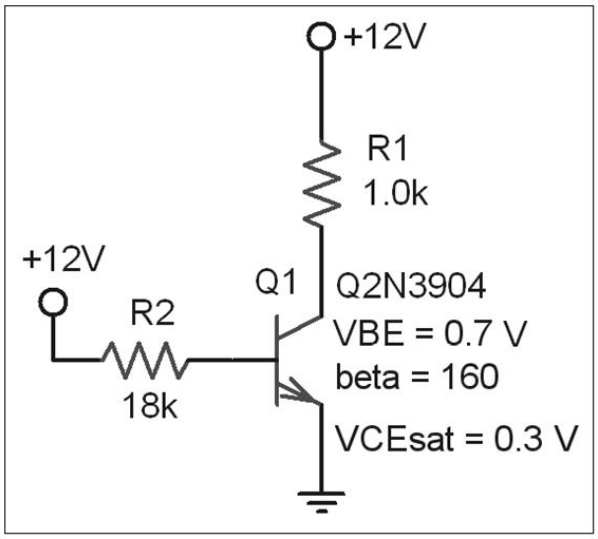


From this, we can determine the rest of the circuit's characteristics:

- $V_{CE} = V_{CEsat} = 0.1$ V
- $V_C = 0.1$ V ($V_E + V_{CE}$)
- I_C (which can also be called I_{Csat}) = $\Delta V_{RC}/R_C = (V_{CC} - V_C)/R_C = 4.50$ mA
- $I_E = 4.74$ mA ($I_C + I_B$)

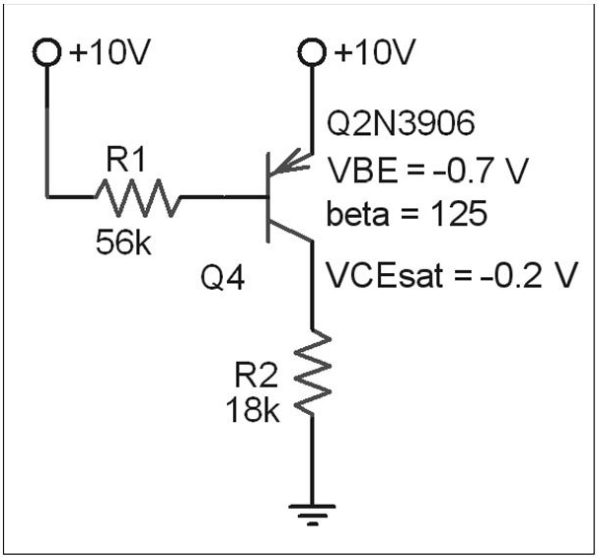
The Saturation Model predicts a reasonable current, since I_C is slightly less than I_{Cmax}.

Your turn.



29. Is Base current possible? _____
30. What is V_B? _____ V
31. Choose a suitable model, then follow the steps required to predict the Collector current using that model. _____ mA
32. What is the maximum possible Collector current, based on only the Collector resistor? _____ mA
33. Has the model you've chosen predicted a plausible Collector current? _____
34. Proceed with the appropriate model. What is V_{CE}? _____ V
35. What is V_C? _____ V
36. What is I_C? _____ mA
37. Looking back, what condition is this transistor in? _____

By now, you should be getting familiar with using the models, so try this one on your own.



39. Is the flow of Base current possible? _____
40. What is V_B? _____ V
41. What is I_C? _____ mA
42. What is V_C? _____ V
43. What is V_{CE}? _____ _____ V
44. Looking back, what condition is this transistor in? _____

You have now learned how to apply a simple set of transistor models to help you predict the DC characteristics of various transistor circuits. What you have learned here will continue to be useful to you as you learn how to make simple transistor logic switches, transistor current switches, and transistor amplifier biasing circuits.

Online Homework System

Assignment Worksheet
5/31/21 - 1:11:24 PM MDT

Name: _____ **Class:**

Class #: _____ **Section #:** _____

Instructor: Ross Taylor **Assignment:** BJT Switch Circuits

Question 1: (1 point)

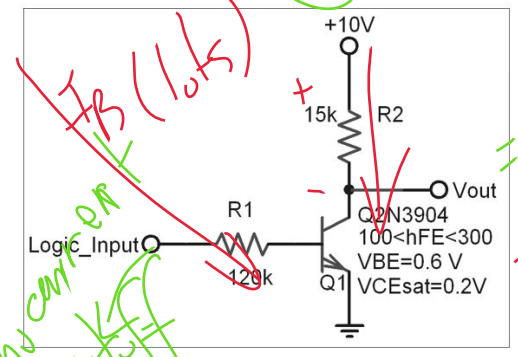
BJT Switch Circuits

The BJT can be used as either a Logic Switch or as a Current Switch. In either operation, we want the operation to be ***Binary***, in other words, with only two possible outcomes. That means that we don't want to have a range of possibilities, such as would be expected in the Linear Active Region.

That leaves Cut-off and Saturation as the two modes used in switching.

BJT Logic Switch

In this mode, we want the transistor to provide us with a Logic HIGH (e.g. +5 V) and a Logic LOW (e.g. 0 V). To do this, we simply put a resistor in series with the "current source" in the Collector, and ensure that we provide enough Base current to drive it into saturation when it is turned on. It will be in Cut-off when it's turned off.



Notice a few things about this schematic. V_{BE} is given at 0.6 V; β is called h_{FE} and is given as a range of values rather than a single number. This is because transistors are extremely variable from one batch to the next, so manufacturers specify a range within which their devices are guaranteed to fit; V_{in} would best be called V_{BB} for this circuit; and V_{out} is actually V_C.

If the Logic Input was a LOW (assume 0 V):

1. What condition would the transistor be in? _____
2. What would be the current through R2? _____ mA
3. Based on your answer to the previous question, what would the output voltage be? _____ V
4. What logic level would this output voltage be best described as? _____

If the Logic Input was a HIGH (assume +5 V):

5. Is Base current possible? _____
6. If so, replace the transistor with the appropriate transistor model for further analysis. What would the Base current be? _____ μA
7. Using the model you chose, determine the lowest possible Collector current predicted for this circuit. _____ mA
8. Your answer probably seems reasonable. However, it's always good to do a Load-Line check. What is the maximum current that could exist if the transistor was completely shorted out? _____ mA
9. From your last two answers, what transistor model should you be using for this analysis? _____
10. What value for V_{CE} does this model predict? _____ V
11. What, then, is the output voltage predicted to be? _____ V
12. What logic level does this represent? _____
13. Fill in the following Truth Table for this circuit.

IN, Binary Logic	OUT, Binary Logic
0	_____

1	_____

14. Which Logic Gate is this? _____

You'll discover that often, when a resistor is used in a circuit as a current-to-voltage converter, the result is an inversion, as seen in this circuit.

Let's use this circuit to learn a few more things about the transistor switch.

15. Notice that there's considerably more Base current that is needed to put the transistor into saturation. What is the predicted Saturation current, using the Saturation model? (It will be slightly less than the maximum current on the DC Load Line.) _____ mA
16. From this, determine the smallest Base current that would saturate the transistor. _____ μA
17. Use this smallest Base current to determine the biggest Base resistor that would allow for saturation. _____ kΩ
18. With the biggest Base resistor in place, what would the output voltage be, if the input voltage was only 3.3 V? _____ V
19. We'd expect this inverter to produce a Logic LOW. Would the value you just calculated be considered a LOW? _____
20. With the original resistor, would the output voltage be a clear Logic LOW? _____

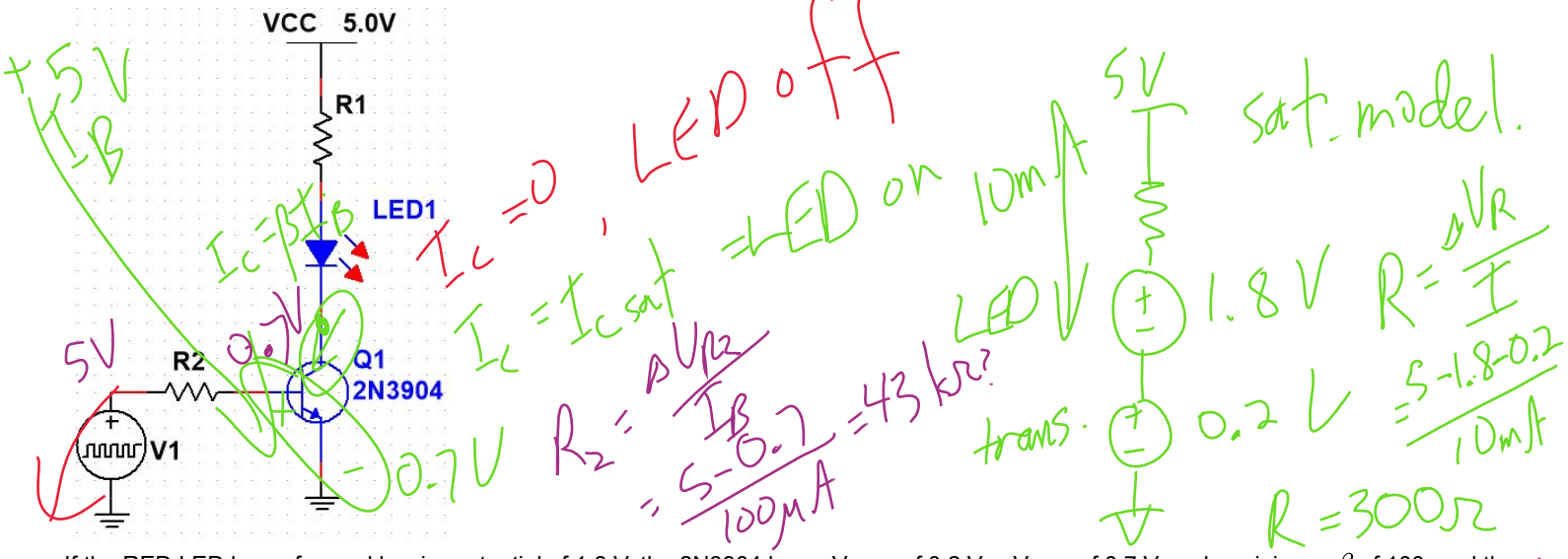
Typically, we pick a Base resistor that's ***one half to one fifth*** of the biggest value for saturation to ensure that the transistor will saturate even if the input voltage levels aren't ideal. That's particularly useful to know if you're using standard TTL Logic ICs, which only guarantee an output HIGH to be 2.4 V or higher. For consistency, in our lab work we'll use approximately ***one half*** in choosing a suitable resistor.

21. Following that train of thought, pick a suitable resistor from the 10% list of resistors (see the Course Formula Sheet) for this circuit. _____ kΩ (The 120 kΩ in the schematic is about the lowest resistor value we would want to use.)

BJT Current Switch

Since transistors are, by nature, current amplifiers, it makes sense to use them to turn current on or off. In this case, the circuit will ***NOT*** be an inverter in terms of the existence or absence of current.

One typical application is the ***LED Driver***, shown below.



If the RED LED has a forward barrier potential of 1.8 V, the 2N3904 has a V_{CEsat} of 0.2 V, a V_{BEon} of 0.7 V, and a minimum β of 100, and the LED requires about 10 mA to glow well:

22. Choose a suitable 10% value resistor for the Collector resistor. 330 Ω (We usually choose a bigger resistor on the Collector side of a transistor circuit.)
23. If the input signal switches between 0 V and +5 V, determine the theoretical maximum resistance for the Base resistor. 43 kΩ
24. Using our previous guidelines, choose a suitable 10% value resistor for the Base resistor. 18 kΩ (We usually choose a smaller resistor at the Base side of a transistor circuit.)
25. When is the LED on? When the input is High

$I_B = I_C / \beta = 10mA / 100 = 100\mu A$

Note: a bigger resistor at the Collector forces the transistor into saturation sooner, and a smaller resistor at the Base provides more current, ensuring saturation, hence the choices indicated above.

Note also that, as a current switch, the transistor is not an inverter -- it's a ***Buffer***, which is something that provides the required output while protecting the controlling signal at the input. A logic-generating device, such as a microcontroller or PLD, cannot produce a lot of current at its outputs. Our MC9S12XDP512 is capable of driving 10 mA at each of its output pins, but its total current output cannot exceed about 50

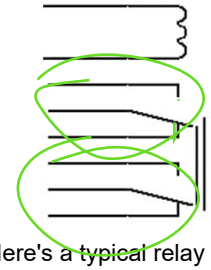
mA. So, if more than four or five LEDs are to be driven by this device, the outputs need to be buffered using transistors or other current drivers. And, clearly, if the intent is for the microcontroller to drive something that requires an amp or two, a transistor buffer is a necessity.

Level Translator

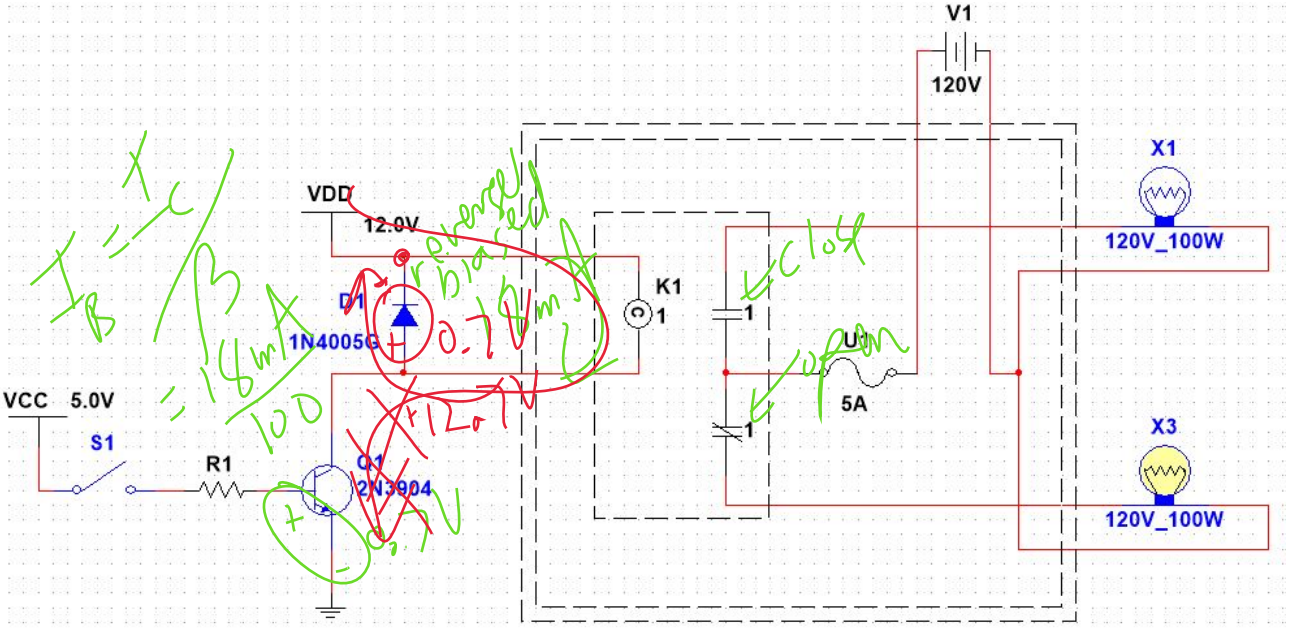
Transistors can also be used as Level Translators -- devices that convert logic at one set of voltage levels, for example 3.3 V TTL, to another set of voltage levels, for example 5 V TTL. In our first example, the transistor was used to convert 5 V TTL to 10 V CMOS. The output voltages may be stepped up or down to whatever values are desired.

Relay Driver

A Relay is an electromechanical device in which current through an electromagnet is used to activate a mechanical switch, usually in another electrically-isolated circuit. The relay coil introduces a new problem: inductive current and the voltage spikes generated when a switch is suddenly opened. The following is a picture of a relay you should have in one of your kits, along with a schematic of what's inside. This is a fairly complicated relay, with two independent double pole switches controlled by a single coil (DPDT switch).



Here's a typical relay circuit, using 5 V TTL to control a 12 V relay coil which activates a switch in a 120 VAC circuit.



Notice two things to begin with: The 120 VAC circuit is electrically-isolated from the logic circuit -- there are no electrical connections between them, and activation occurs entirely by means of an electromagnet closing a switch; there's a diode in the circuit that we hadn't mentioned before -- more on that to come!

26. The relay coil draws 18 mA when powered from 12 VDC. How much Base current is required, if the worst β for this transistor is 100? _____ μA
27. Given that V1 represents 5 V logic and assuming a V_{BEon} of 0.7 V for the transistor, what is the biggest value allowed for R2? _____ kΩ Pick a suitable 10% resistor value, given our previous guidelines. _____ kΩ

28. Given that the upper set of contacts in the relay switchin side is normally-open (N.O.), when the input is HIGH the 120 VAC lamp connected to that switch will be ON

Now, for the diode in the schematic.

29. Given its orientation, it is normally reverse biased, and therefore has no effect on the transistor circuit.
30. In an inductor, such as the electromagnet in the relay, which electrical characteristic cannot be instantly changed? current

When the transistor suddenly goes into Cut-off, there is no path for the current from the coil, and the coil, acting as a nearly-ideal current source, will instantly increase the voltage to the point at which it will find a path for the current. If the relay was in a circuit controlled by a regular switch instead of a transistor, there would be a spark or series of sparks across the contacts of the switch as the relay coil current dissipated. However, in our case, the only path for that current is through the transistor. Without the diode, the voltage would rise until it reaches transistors breakdown, at which point the current would flow under the influence of a high voltage, resulting in considerable power since $P = IV$. If the current surge lasts long enough, the transistor will be damaged or destroyed.

If, however, the diode is present, the voltage generated by the coil current will rise until Diode's forward bias, which will put the anode of the diode at a voltage of 12.7 V in this circuit. The transistor will be protected, and the diode will provide a path for the current at a very small voltage drop across the diode of 0.7 V, and little power will be generated.

Key take-away: always put a protection diode across the coil of a relay or any other inductive load that's being switched by a transistor!

like a motor

Online Homework System

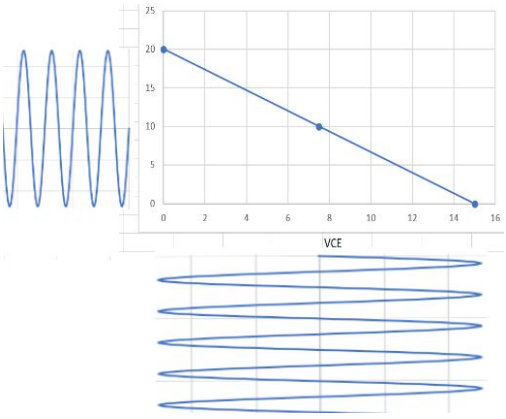
Assignment Worksheet
5/20/22 - 9:28:22 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** BJT Amplifier Biasing Circuits

Question 1: (1 point)

Transistor Amplifier Biasing

In the previous topics, we needed to design our switch circuits to switch from Cut-off to Saturation, completely avoiding the Linear Active Region. However, when it comes to Linear Amplifiers, we need to be in the Active Region, and preferably pretty close to the middle of the Active Region so that we can vary the output in both directions without hitting the non-linearity of either Saturation or Cutoff.



The point in the middle of the Load Line above is called the "Quiescent Point" or "Q-Point". It would be the actual DC conditions for the biased circuit. If it is designed to be in the middle, as shown, then if we superimpose an AC signal on top of the DC Q-Point, as the Collector current drops V_{CE} rises, and as the Collector current rises, V_{CE} drops. In the example shown, the current and voltage both vary sinusoidally, which turns this into a linear amplifier.

If the Q-point was too close to either Saturation or Cutoff, the sinewave would end up being truncated or "chopped off", resulting in a distorted signal.

1. If the Q-point was too close to Saturation, V_{CE} would be distorted at the _____ end. If the Q-point was too close to Cut-off, V_{CE} would be distorted at the _____ end.

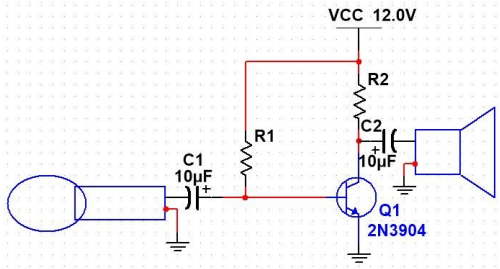
So, it is important to be able to carefully control the Q-point conditions by choosing the correct resistors and, as you will see, picking the best biasing circuit.

Base Bias or Fixed Bias

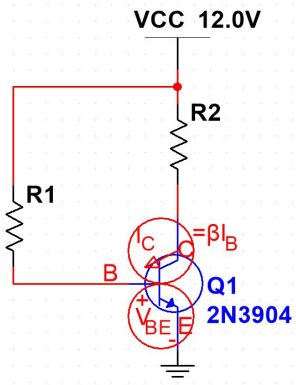
The simplest Biasing arrangement is one we've been using, but as a switch by forcing it into Saturation or Cut-off. Here, we will attempt to put the Q-Point in the middle of the DC Load Line.

Here's a worked example to show you how the analysis goes, then we'll do one to investigate the beta dependency of this biasing arrangement.

In one (fairly poor) system, the following amplifier circuit was used as an interface between a microphone and a powered speaker (i.e. containing its own power amplifier).



The microphone and the speaker are "AC-Coupled" to the amplifier by two capacitors which block the DC levels seen at the Collector and Base of the transistor. This means we can ignore the microphone, speaker, and capacitors when we're doing an analysis of the biasing arrangement. Here's just the DC biasing part of the circuit, with the pins labelled and the Active Model imposed on it.



For this design, R2 was chosen to be 560 Ω to match the input impedance of the powered speaker.

Since we want V_{CE} to be $V_{CC}/2$, and since V_E is ground (0.0 V), that means that V_C should be 6.0 V.

To find I_C, we calculate using the voltage across R_C: $I_C = (V_{CC} - V_C)/R_C$ = 10.7 mA.

Using the Transfer Function, we determine that $I_B = I_C/\beta$. The Data Sheet for the 2N3904 tells us that beta could be anywhere from 100 to 300, so we'll assume β = 200. That means that I_B = 53.6 μA.

Since V_E = 0.0 V, $V_B = V_{BE}$. Our experience in the lab indicates this is probably going to give us V_B = 0.7 V. So, R_B would need to be as close as possible to R_B = (12 - 0.7)/53.6 μA = 211 kΩ. The closest 10% standard value to this is 220 kΩ, so we pick that for R_B. Notice we pick the ***closest***, not half or anything else -- we want the current to be as close as possible to the desired value so that the Q-Point is as close as possible to the middle of the DC Loadline.

Since our chosen resistor isn't the Ideal value, we need to do a Theoretical prediction to see how our actual circuit will behave.

I_B = (12 - 0.7)/220 kΩ = 51.4 μA

$I_C = \beta I_B$ = 200 * 51.4 μA = 10.3 mA

$V_C = V_{CC} - I_C R_C$ = 12 V - 10.3 mA * 560 Ω = 6.25 V

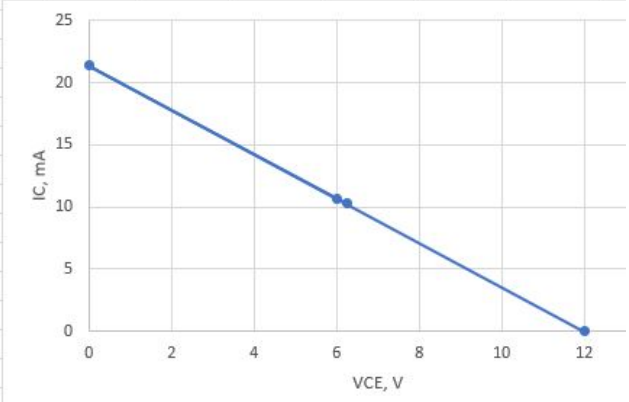
Since V_E = 0.0 V, $V_{CE} = V_C - V_E$ = 6.25 V.

Let's see where that puts us on the DC Loadline.

If the transistor was "open" the current would be zero and the voltage across it would be V_{CEmax} = 12 V.

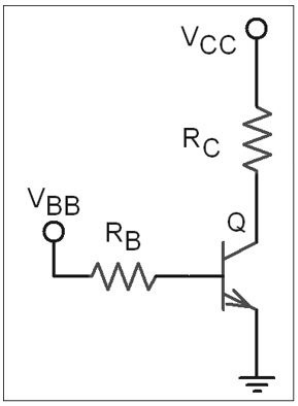
If the transistor was shorted, the voltage across it would be zero and the current would be at a maximum: I_{Cmax} = 12/560 = 21.4 mA. This gives us the following DC Loadline, with two Q-Points on it: The Ideal (exactly in the middle) and the Theoretical (based upon the actual resistors chosen).

	A	B	C	D	E	F	G	H	I	J
1		VCE	IC							
2	VCEmax	12	0							
3	ICmax	0	21.4							
4	Ideal	6	10.7							
5	Theoretical	6.25	10.3							
6										
7										
8										
9										
10										
11										
12										
13										
14										



This shows us that our circuit's predicted Q-Point is close to the middle of the DC Loadline, where we want it to be. It's slightly toward the Cutoff end. In reality, it would be better if it were closer to the Saturation end, but we won't go into the reasons for that.

Let's now investigate a similar circuit, and in the process discover the reason why we consider Self Bias or Fixed Bias not to be a good biasing arrangement.



Assume that V_{BB} and V_{CC} are the same supply, +10 V_{DC}, that V_{BEon} is 0.7 V, and that β ranges from 100 to 300.

2. To put the Q-Point in the middle of the DC Load Line, V_{CE} should be _____ V_{DC}
3. If the Q-Point current is to be 10 mA, what should R_C be, ideally? _____ Ω
4. Pick the ***closest*** 5% resistor value. _____ Ω
5. Use the average value for β, 200, to determine the Base current required. _____ μA
6. Determine the ideal value for R_B _____ kΩ, the pick the ***closest*** 5% resistor value _____ kΩ

Since the resistors chosen aren't exactly what we wanted, we need to determine the actual theoretical circuit characteristics for our circuit.

7. What is the theoretical value of the Collector current? _____ mA
8. What is the theoretical value of V_{CE}? _____ V (Remember to subtract the voltage across the resistor from the supply to get the voltage across the transistor.)

The problem with this circuit is that it is highly β***-Dependent***, which means that variations in transistor characteristics affect it significantly.

9. Using the same circuit components but using the worst transistor available -- β = 100 -- recalculate the Collector current _____ mA and V_{CE} _____ V
10. Using the same circuit components but using the best transistor available -- β = 300 -- recalculate the Collector current _____ mA and V_{CE} _____ V
11. On a piece of paper, draw the DC Load Line: V_{CEmax} = _____ V and I_{Cmax} = _____ mA. Plot the three Q-points for the three transistors on your DC Load Line.
12. This transistor circuit is highly dependent on the β of the transistor.

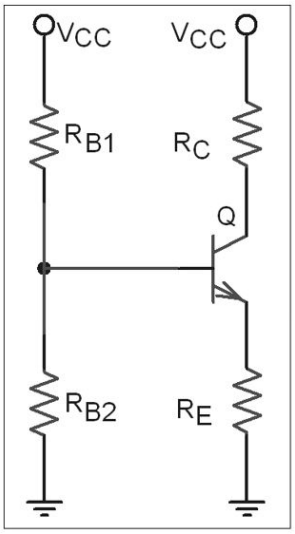
    (a) True

    (b) False

Question 2: (1 point)

BJT Voltage Divider Bias

To deal with the problem of β-Dependency, a circuit with ***negative feedback*** has been designed. This is a surprisingly difficult circuit to design and analyze completely accurately, so in this course we will provide some limits to the design characteristics which will give us a good approximation of the actual performance of the circuit. Here's the circuit:

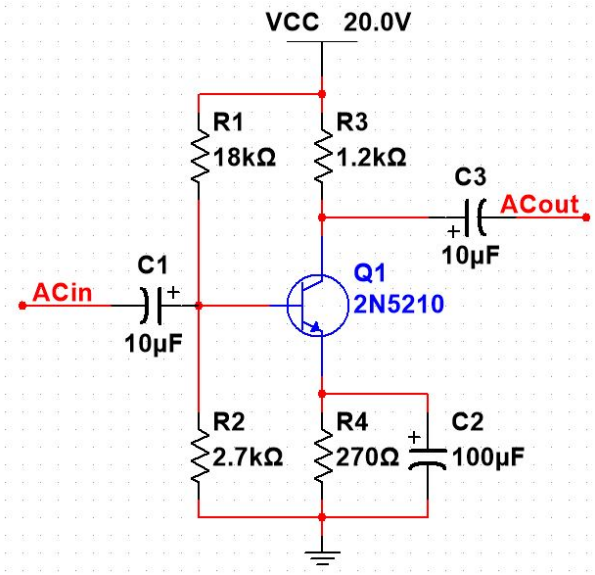


Here are the guidlines for a suitable design, and the results expected.

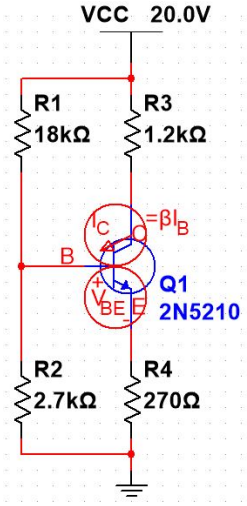
- Pick a transistor with a β greater than 100.
- Choose a value for R_E that will make V_E approximately 1/10th of V_{CC}.
- Make $V_{CE}=V_{CC}/2$.
- Choose a value for $R_{B2} = 10R_E$.
- Calculate a value for R_{B1} that will set V_B to $V_E + V_{BE}$.

The results should be within 10% of the actually-measured (empirical) values.

We'll start with a quick worked example in which we will analyze an existing circuit, then we'll move into a design-oriented question. The following schematic is a workable amplifier, again with DC-blocking capacitors C1 and C3 to isolate the AC signals at the input and output from the DC biasing voltages at the Base and Collector. C2 actually provides an AC short to ground which removes the negative feedback but only for the AC signal, allowing this "Common Emitter" amplifier to have a fairly large signal gain. But you don't need to know any of that, because we don't do transistor amplifiers in the course. All you need to know is the DC biasing part, which exists inside the big capacitors.



Here's just the DC-biasing part of the circuit, again labelled and with the Active Model superimposed over it. We'll discover that the only part of the Active Model we need in our simplified analysis is V_{BE}.



Let's check to see that the circuit meets the requirements specified above:

- The Data Sheet (https://media.digikey.com/pdf/Data%20Sheets/ON%20Semiconductor%20PDFs/2N5210,MMBT5210.pdf) for the 2N5210 says that beta ranges from 250 to 900 -- that's much greater than 100
- R_{B2} is ten times the size of R_E

We'll have to do some calculations to check the other conditions.

Assuming that the current through R_{B2} is much greater than the Base current, we can treat R_{B1} and R_{B2} as a simple voltage divider: V_B = 20(2.7k)/(18k + 2.7k) = 2.61 V. Now we can determine V_E and see if it's close to ideal:

- $V_E = V_B - V_{BE}$ = 2.61 - 0.7 = 1.91 V, which is pretty close to one tenth of V_{CC}.

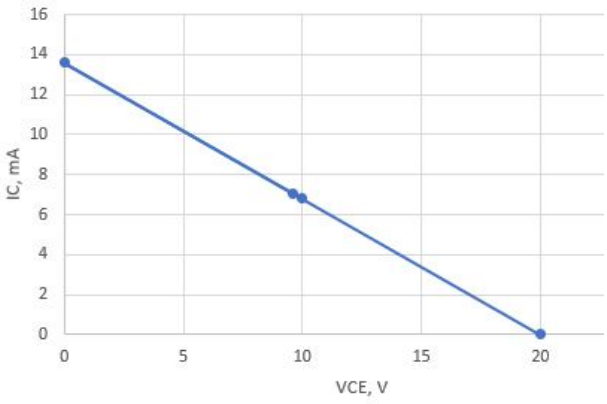
Again, we'll need to do some calculations to determine V_{CE}. $I_E = V_E/R_E$ = 1.91/270 = 7.07 mA. Since we assume there's no appreciable Base current, we can say that I_C = 7.07 mA. That means that $V_C = V_{CC} - I_C R_C$ = 20 - 7.07 mA*1.2 kΩ = 11.5 V. So...

- $V_{CE} = V_C - V_E$ = 11.5 - 1.91 = 9.6 V, which is about one half of V_{CC}.

Now for the DC Loadline analysis.

When the transistor is "open", the voltage across it will be 20 V. When it is shorted, the current will be I_{Cmax} = 20/(1.2 kΩ +270 Ω) = 13.6 mA.

	VCE	IC
VCEmax	20	0
ICmax	0	13.6
Ideal	10	6.8
Theoretical	9.6	7.07



Now for a design-oriented question.

For the circuit given, let V_{CC} = +15 V_{DC}, and the transistor characterics be those of the 2N3904 we've been working with. Again, work towards having a quiescent Collector current of 10 mA.

13. Determine an ideal value for R_E. _____ Ω
14. Assuming the Collector and Emitter currents are basically the same, determine an ideal value for R_C. _____ Ω
15. Determine an ideal value for R_{B2}. _____ kΩ
16. Determine an ideal value for R_{B1}. _____ kΩ

17. Now pick the closest 5% resistor values for each of these: R_E = _____ Ω, R_C = _____ Ω, R_{B2} = _____ kΩ, and R_{B1} = _____ kΩ.

Again, since the chosen resistors are not exactly the ideal values, we need to analyze the theoretical conditions of our actual circuit.

18. V_B = _____ V
19. V_E = _____ V
20. I_E = _____ mA
21. Assuming I_C and I_E are the same, what is V_{CE}? _____ V
22. Check back: did you use β in any of your calculations? _____

This circuit is not β-Dependent, so picking different transistors will have very little effect on the circuit biasing characteristics.

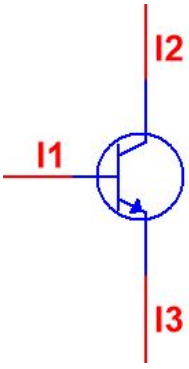
Online Homework System

Assignment Worksheet
5/31/21 - 9:42:24 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA06 BJT Theory Quiz

Question 1: (4 points)

Use the transistor shown to answer the questions that follow. For all questions, I_2 is 425 μA and I_3 is 427 μA.



In microamps, what is I_1? _____ μA.

What is the current efficiency, α? _____

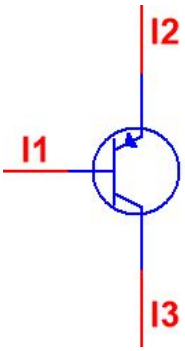
What is the current gain, β? _____

For the transistor shown, the current labelled I_1, using conventional current notation, would flow OUT of the transistor pin it is associated with.

(a) True
(b) False

Question 2: (4 points)

Use the transistor shown to answer the questions below. In each case, I_1 is 30 μA and I_2 is 4.35 mA.



What is I_3, in milliamps? _____ mA

What is the current efficiency, α? _____

What is the current gain, β? _____

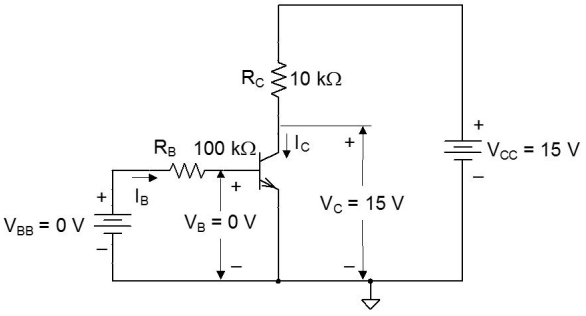
For the transistor shown, the current labelled I_1, using conventional current notation, would flow OUT of the transistor pin it is associated with.

(a) True

(b) False

Question 3: (1 point)

The transistor in the schematic shown is in which mode of operation?



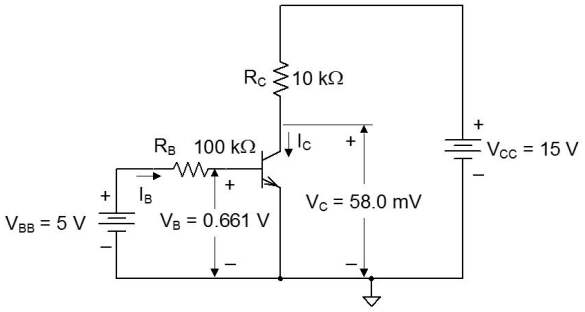
(a) Active

(b) Cut-off

(c) Saturation

Question 4: (1 point)

The transistor in the schematic shown is in which mode of operation?



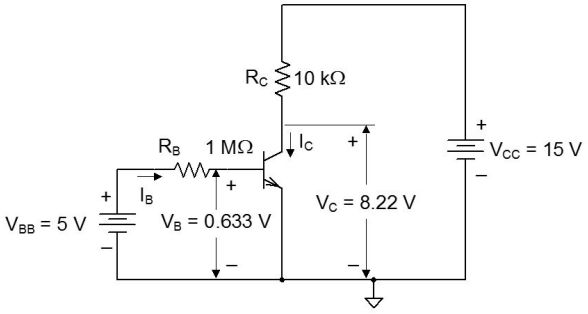
(a) Active

(b) Saturation

(c) Cutoff

Question 5: (1 point)

The transistor in the schematic shown is in which mode of operation?



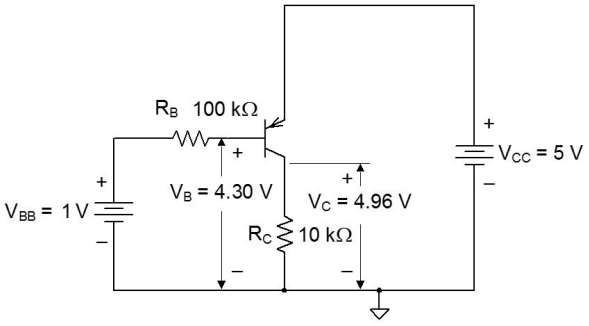
(a) Active

(b) Cut-off

(c) Saturation

Question 6: (1 point)

The transistor in the schematic shown is in which mode of operation?



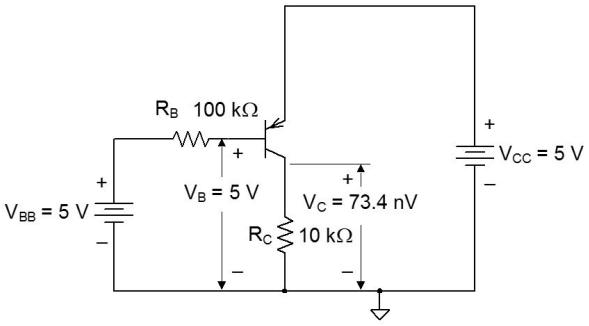
(a) Active

(b) Cut-off

(c) Saturation

Question 7: (1 point)

The transistor in the schematic shown is in which mode of operation?



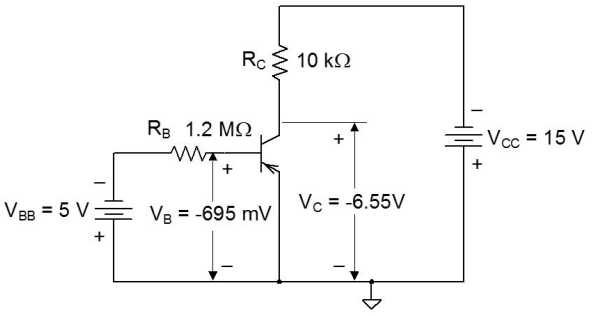
(a) Active

(b) Cut-off

(c) Saturation

Question 8: (1 point)

The transistor in the schematic shown is in which mode of operation?



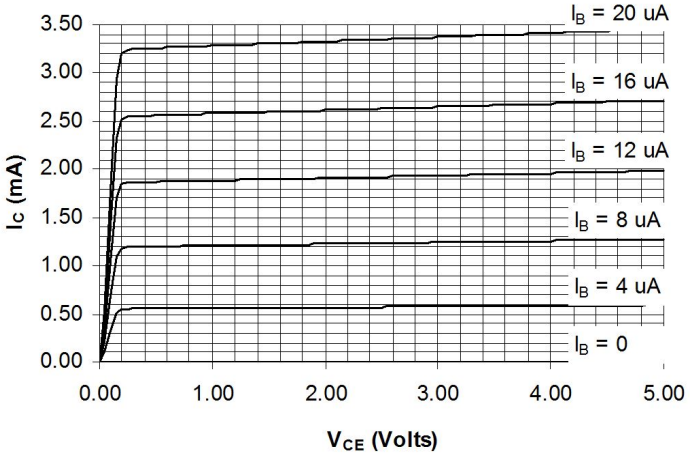
(a) Active

(b) Cut-off

(c) Saturation

Question 9: (1 point)

Given the convention that current flowing into a device pin is positive, what type of BJT would produce the following family of curves?



(a) NPN

(b) PNP

Online Homework System

Assignment Worksheet
6/7/22 - 10:48:51 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Lab04 BJT Switching and Biasing

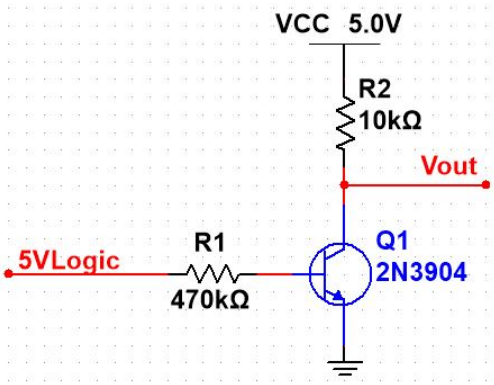
Question 1: (10 points)

Lab 04 Pre-Lab Activity

Note: Do not move on to the "Next" page until you have completed your Pre-Lab. The next page is the Lab Activity, and once you move to that page, you will not be able to return to the Pre-Lab page!

Transistor Switch

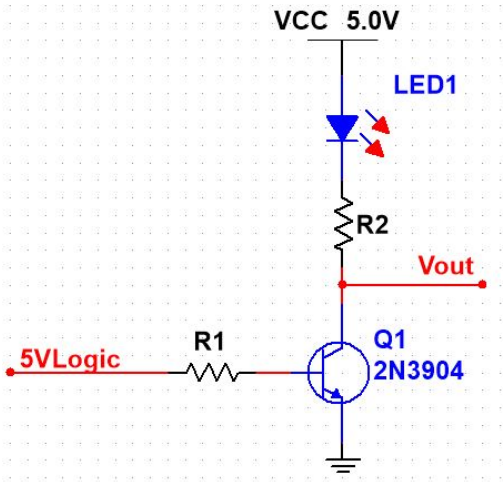
Use the following schematic to answer the questions below. Assume the transistor has a worst-case β of 100, a V_{BEon} of 0.7 V, and a V_{CEsat} of 0.2 V.



1. Follow the process to determine what the Active Transistor Model predicts as the Collector current for this circuit when the input is HIGH. _____ μA
2. Use the Saturation Transistor Model to predict the saturation value for the Collector current when the input is HIGH. _____ μA
3. Based upon your results, this transistor is in which condition? _____

LED Driver -- Current Switch

Use the schematic below to answer the questions that follow. Assume the transistor has a worst-case β of 100, a V_{BEon} of 0.7 V, and a V_{CEsat} of 0.2 V. Also assume that the RED LED has a forward barrier potential of 1.8 V.

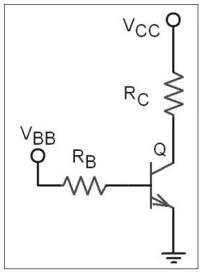


4. Assuming the transistor is saturated, determine an ideal value for R2 to allow a current of 12 mA to pass through the LED. _____ Ω

5. Determine the maximum value for R1 that will still saturate the transistor when it is turned on, if the LED current is 12 mA. _____ kΩ
6. Using guidelines from the Online Lessons, pick a suitable 10% resistor value for R2. _____ Ω
7. Also using guidelines from the Online Lessons, pick a suitable 10% resistor value for R1. _____ kΩ

Fixed Bias Circuit

Use the following schematic diagram to answer the questions below.



$V_{CC} = V_{BB} = +12$ V

Q = 2N5210

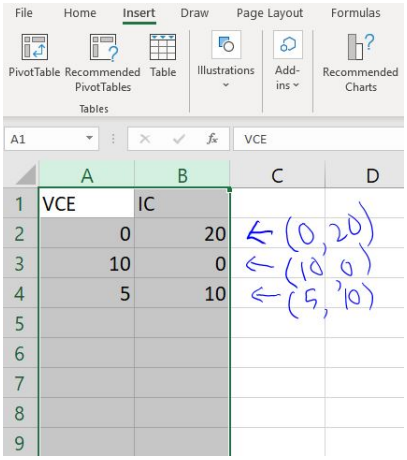
$\beta = 250$

$V_{BEon} = 0.7$ V

$R_B = 390$ kΩ

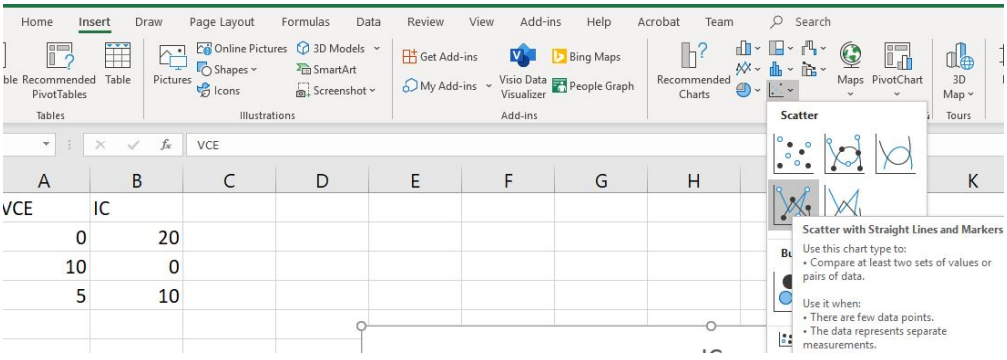
$R_C = 820\ \Omega$

8. Determine the theoretical I_B. _____ μA
9. Determine the theoretical I_C. _____ mA
10. Determine the theoretical V_{CE}. _____ V
11. For the DC Load Line, determine I_{Cmax} for the biasing circuit. _____ mA
12. For the DC Load Line, determine V_{CEmax}. _____ V
13. Use Excel to create a plot of your DC Load Line, to which you can add future values, as follows:
    1. Set up two columns, one for V_{CE} and one for I_C, and enter the coordinates of the endpoints of the DC Load Line as shown here: $(0,I_{Cmax})$ and $(V_{CEmax},0)$. Enter your calculated values, not the ones shown in this picture. Also, include the "ideal" Q-Point, right in the middle of the DC Load Line (half of V_{CEmax}, half of I_{Cmax}).



Note: Your values will be different! These are examples only!

    2. Select the entire first two columns (not just your data) by dragging your mouse across the A and B at tops of the columns.
    3. Under Insert > Scatter Plot, select a scatter plot with straight lines and markers, as shown in this picture.

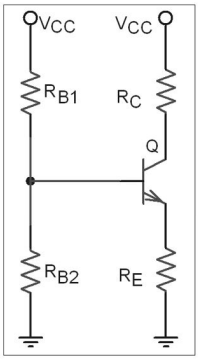


    4. Right-click the line in your new graph and select "Add Trendline ..." then make sure it's set to "linear", and check "Display Equation on chart".
    5. Now, under the entries in Columns A and B for the three existing points on your DC Load Line, enter the coordinates for your predicted Q-Point. If all goes well, this point should show up on the DC Load Line. Take a screenshot of the results and upload it here for two marks, using the usual guidelines for naming the file. Document Upload (Direct)

6. Save your Excel file using a descriptive name with no spaces -- you will be using this in the activity, and will submit it with your results.

Voltage Divider Bias

Use the schematic diagram below to answer the questions that follow.



V_{CC} = +12.0 V
Q = 2N5210
β = 250
V_{BEon} = 0.7 V
R_{B1} = 56 kΩ
R_{B2} = 10 kΩ
R_C = 3.9 kΩ
R_E = 1.0 kΩ

14. Determine the theoretical value of V_B, ignoring any current into the Base. _____ V
15. Determine the theoretical value of V_E. _____ V
16. Assuming I_B is negligible, determine I_C. _____ mA
17. Determine the theoretical V_{CE}. _____ V
18. Create a new Excel file (or a new tab in your old file) for this question, and create the DC Load Line as for the previous question. You will need to determine the values for I_{Cmax} and V_{CEmax}, and for the ideal Q-point. Add your calculated Q-Point coordinates to the graph, take a screenshot, and upload it here for two marks. Document Upload (Direct)
19. Save your Excel file(s) for use in the Lab Activity.

You have now completed the Pre-Lab. You may Save and Close or move on to the Lab Activity page, but do not "Submit" until you have completed the Lab Activity!

Question 2: (10 points)

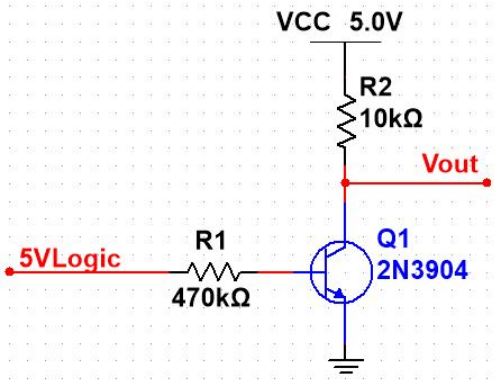
Lab 04 Activity

Since all these activities involve signals with DC components, make sure your oscilloscope is DC coupled. In fact, your oscilloscope should always be DC coupled (DC = Direct Coupling, not direct current) regardless of the type of signal you are investigating, unless you have a clear reason to block the DC component, something we rarely need to do.

(If you want to try this activity at home, make sure the Analog Discovery 2 has the BNC breakout board installed, that the oscilloscope channels are DC coupled (jumpers on the breakout board), and that the signal generator channels are set to zero ohm output impedance (jumpers on the breakout board). Don't use the flywires!)

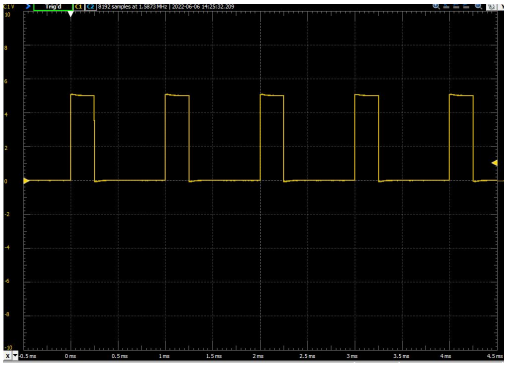
BJT Transistor Switch

On your breadboard, build the circuit below and use it to answer the questions that follow. Use a DC power supply to supply VCC and use a signal generator to generate the input signal. (More to follow.)



1. The input signal from a signal generator must be a 5 V logic pulse, NOT a "true" square wave, but with a generally square appearance.
    - Set the frequency to 1 kHz
    - set the duty cycle to 25%
    - adjust the signal so that it switches between 0 V and +5 V (NOT between -2.5 V and +2.5 V, - 5.0 V and +5.0 V, or any other combination of common mistakes made in setting up this signal).

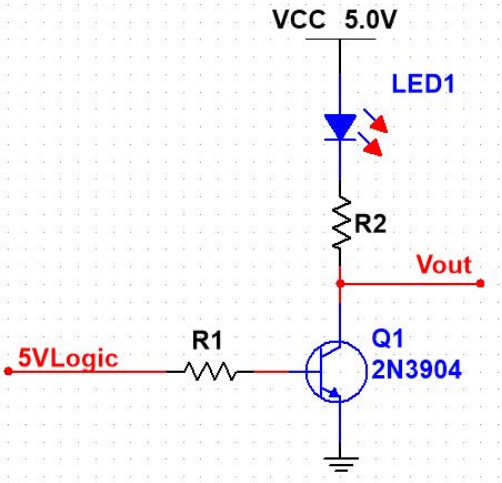
Here's what it should look like:



2. Use Channel 1 of the oscilloscope to verify that your input pulse does, indeed, match all the characteristics specified above. Make sure you optimize the display for proper visualization and accurate measurement.
3. Use oscilloscope channel 2 to observe the output signal. When the input signal is HIGH, the output is _____
4. Measure and record the output HIGH voltage. Use your oscilloscope's Measure functions to get an accurate value. _____ V
5. Measure and record the output LOW voltage. _____ V
6. For a grade out of three, ask your instructor to inspect your circuit and oscilloscope settings. _____

BJT LED Driver (Current Switch)

On your breadboard, build the circuit below and use it to answer the questions that follow. Use R_1 = 15 kΩ and R_2 = 270 Ω.



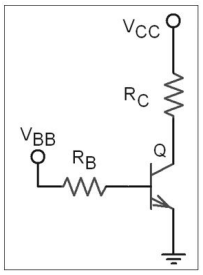
7. Use the signal generator to generate a pulse similar to the one above, but this time change the frequency to 0.5 Hz, not 1 kHz, so you can observe the LED. Connect your oscilloscope to observe the input on Channel 1 and the output on Channel 2. You will

need to adjust the Horizontal timebase to display this very slow signal.

8. The LED glows when the input signal is _____
9. When the LED is glowing, V_{out} is _____ V
10. This means that when the LED is glowing, the transistor is _____
11. Move your Channel 2 probe to the other side of R_2, and record the voltage when the transistor is turned on. Use the difference between this voltage and the voltage you recorded above (at the other end of R_2 when the LED was glowing) to determine the current through R_2. _____ mA

Fixed Bias Circuit (Base Bias)

On your breadboard, build the circuit in the schematic diagram below, and answer the questions that follow. Use the same DC power supply to provide V_{CC} and V_{BB}. In other words, since they're both +12 V, they can be supplied from a single source.



$V_{CC} = V_{BB} = +12$ V

Q = 2N5210

$\beta = 250$

$V_{BEon} = 0.7$ V

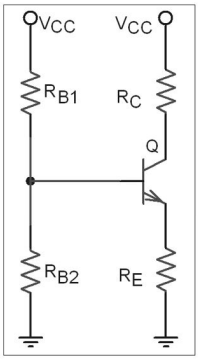
$R_B = 390\ k\Omega$

$R_C = 820\ \Omega$

12. Use your DMM for this part, since all we're looking for is DC Quiescent conditions. Measure the following:
    1. V_B = _____ V
    2. V_C = _____ V
    3. V_E = _____ V
13. From these values, determine V_{CE} _____ V and I_C (be careful to determine this from the voltage drop across the resistor, not directly from V_C, since V_C is across the transistor, not the resistor). _____ mA
14. Now, replace your 2N5210 with a 2N3904 (same pinout). From this, determine V_{CE} _____ and I_C _____ mA
15. Open the Excel spreadsheet you created earlier for the Fixed Bias circuit. Under the existing values, enter the coordinates for the 2N5210 Q-Point and the coordinates for the 2N3904 Q-Point. Your calculations above are correct if these two land on the previous line without affecting it. Note: you should have only one graph with multiple Q-point coordinate pairs on it! Take a screenshot of the Excel spreadsheet and upload it here for two marks. Document Upload (Direct)
16. Your two new points should be quite different from each other and from the predicted Q-Point. This means that this circuit is very _____

Common Collector Bias

Build the circuit in the schematic diagram below, and answer the questions that follow.



$V_{CC} = +12.0$ V

Q = 2N5210

$\beta = 250$

$V_{BEon} = 0.7$ V

$R_{B1} = 56\ k\Omega$

$R_{B2} = 10\ k\Omega$

$R_C = 3.9\ k\Omega$

$R_E = 1.0\ k\Omega$

17. Use the DMM to measure the following DC Quiescent conditions:
    1. V_B = _____ V
    2. V_C = _____ V
    3. V_E = _____ V

18. From these values, determine V_{CE} _____ V and I_C (be careful to determine this from the voltage drop across a resistor; assume that I_C is very similar to I_E, or prove this by doing calculations with both resistors). _____ mA
19. Now, replace your 2N5210 with a 2N3904. From this, determine V_{CE} _____ and I_C _____ mA
20. Open the Excel spreadsheet you created earlier for the Common Collector Bias circuit. Under the existing values, enter the coordinates for the 2N5210 Q-Point and the coordinates for the 2N3904 Q-Point, all on the same graph. Your calculations above are correct if these two land on the previous line without affecting it. Take a screenshot of the Excel spreadsheet and upload it here for two marks. Document Upload (Direct)
21. Your two new points should be quite similar to each other and to the predicted Q-Point. This means that this circuit is very _____

You have now completed this Lab. You will not be able to return to it after you submit it for grading!

Online Homework System

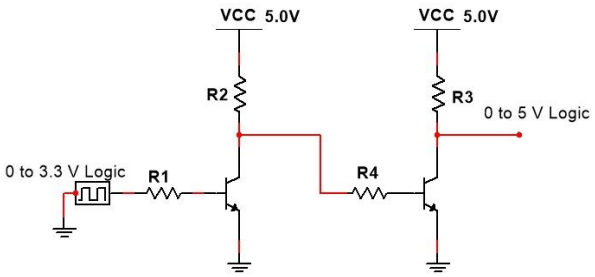
Assignment Worksheet
6/7/22 - 1:16:28 PM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA07 Level Translators Activity

Question 1: (10 points)

Frequently, there's a need to interface digital devices that use different voltage levels to represent logical values. One typical situation is interfacing 5.0 V TTL or CMOS logic with 3.3 V logic – for example, interfacing an Arduino or Raspberry Pi with the microcontroller kit used in future courses.

Perhaps the easiest circuit to conceptualize is a double-inverter using NPN transistors, shown below.



Use 1 kΩ for both of the Collector resistors. If the input is 3.3 V logic, determine the maximum resistance for resistor R_1, based upon β = 100, V_{BEon} = 0.7 V, V_{CEsat} = 0.1 V. Now pick the resistor from your parts kit that is slightly less than half the calculated value.

_____ kΩ

In Multisim, build this circuit using 2N3904 transistors, 1 kΩ resistors for R_2 and R_3, and your chosen value for both R_1 and R_4. Set up the generic function generator to produce a +3.3 V logic PULSE:

- the frequency is to be 500 Hz
- the Duty cycle is to be 75%
- the Amplitude is to be 1.65 V_p (i.e. 3.3 $V_{p\text{-}p}$)
- the Offset is to be 1.65 V_{DC} (this will raise the signal so that its LOW level will be zero and its HIGH level will be 3.3 V)

Use the Tektronix oscilloscope to verify that the circuit properly translates 3.3 V logic to 5.0 V logic. Use Channel 1 to observe the input, and Channel 2 to observe the output. Set up the two channels ***identically***, including the zero position markers, with the larger of the two signals maximized on the screen. With your circuit and oscilloscope visible, do a screen capture and upload it here for a possible six marks. Do not use any spaces or special characters in the filename, but include something to personalize it.

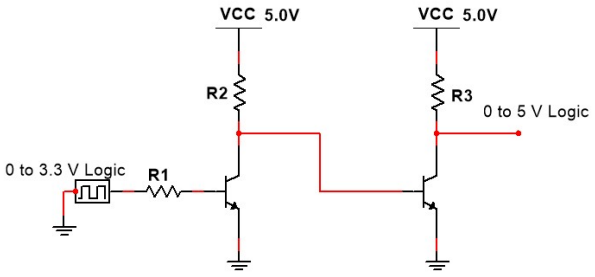
Document Upload (Direct)

Now, make all the necessary changes to your function generator to produce 5.0 V logic at the input. Make sure the LOW level is zero and the HIGH level is 5.0 V. Keep the timing characteristics the same as before.

Change V_{CC} to 3.3 VDC. Verify that your circuit properly translates 5.0 V logic to 3.3 V logic, and take another screen capture to demonstrate the results. Upload it here for two marks.

Document Upload (Direct)

Since R_2 can provide current limiting to both the Collector of the first transistor and the Base of the second transistor, R_4 can be eliminated if we change all the resistor values, as shown below.



Start again with choosing 1 kΩ for R_3. When the first transistor is turned off, R_2 becomes the Base resistor for the second transistor. Using the transistor characteristics given previously, choose a resistor from your kit that is just less than half the maximum value for R_2 as the Base resistor for the second transistor.

_____ kΩ

When the first transistor is turned on, R_2 becomes its Collector resistor, and no current goes through the Base of the second transistor. Using the value you chose for R_2 as the first transistor's R_C, choose a resistor from you kit that is just less than half the maximum value for R_1.

_____ MΩ

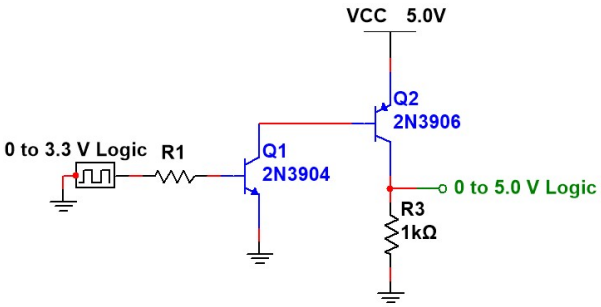
Set up your function generator as before to produce 3.3 V logic and set V_{CC} to 5.0 V_{DC}. Verify that this circuit properly translates 3.3 V logic to 5.0 V logic. Arrange your circuit and oscilloscope to show your results, do a screen capture and upload it here for two marks.

Document Upload (Direct)

Now, set up the function generator for 5.0 V logic and the power supply for 3.3 VDC, and verify that this circuit properly translates 5.0 V logic to 3.3 V logic. Arrange your circuit and oscilloscope to show your results, do a screen capture and upload it here for two marks.

Document Upload (Direct)

With a bit of creative transistor theory we've been able to reduce the number of resistors from four to three. By using one NPN transistor and one PNP, we can reduce the number of resistors to two, using the following arrangement.



First, determine the Base current for Q_2, assuming that the characteristics for the 2N3906 are equivalent to those of the 2N3904 given previously. Use this Base current as the Collector current for Q_1, and determine the maximum resistance of R_1. Now, choose a resistor from your kit that is just less than a **quarter** of the maximum resistance (to compensate for variations in two transistors).

_____ MΩ

Since we have a good, simple circuit, we'll actually build it on the breadboard and test it.

- make sure you've got a 2N3904 NPN transistor and a 2N3906 PNP transistor
- make sure you know what's E, B, and C for each of the devices, and the correct pinout for each -- print the schematic above, and label each pin correctly to help you with this; put the pin numbers on the schematic so you can't go wrong
- use a +5 VDC power supply for VCC
- use a signal generator to create the pulse:
  - amplitude switching from 0 V to +3.3 V
  - frequency of 500 Hz
  - duty cycle of 75%

Use the two oscilloscope channels to observe the signals at the input and output of your circuit.

- verify that the input signal is actually switching between 0 V and +3.3 V
- verify that the output signal is switching between 0 V and +5.0 V

If you are completing this exercise at home, once you are satisfied that your circuit and equipment are working as they should, set up your oscilloscope to show your results properly, do a screen capture, and upload it here for two marks. In the lab, ask your instructor to grade your work.

Document Upload (Direct)

Now, change the DC supply voltage to +3.3 V and the pulse so it switches between 0 V and +5.0 V. Verify that this circuit properly translates 5 V logic to 3.3 V logic.

Set up your oscilloscope to show your results properly, do a screen capture, and upload it here for two marks, or ask your instructor to grade your work.

Document Upload (Direct)

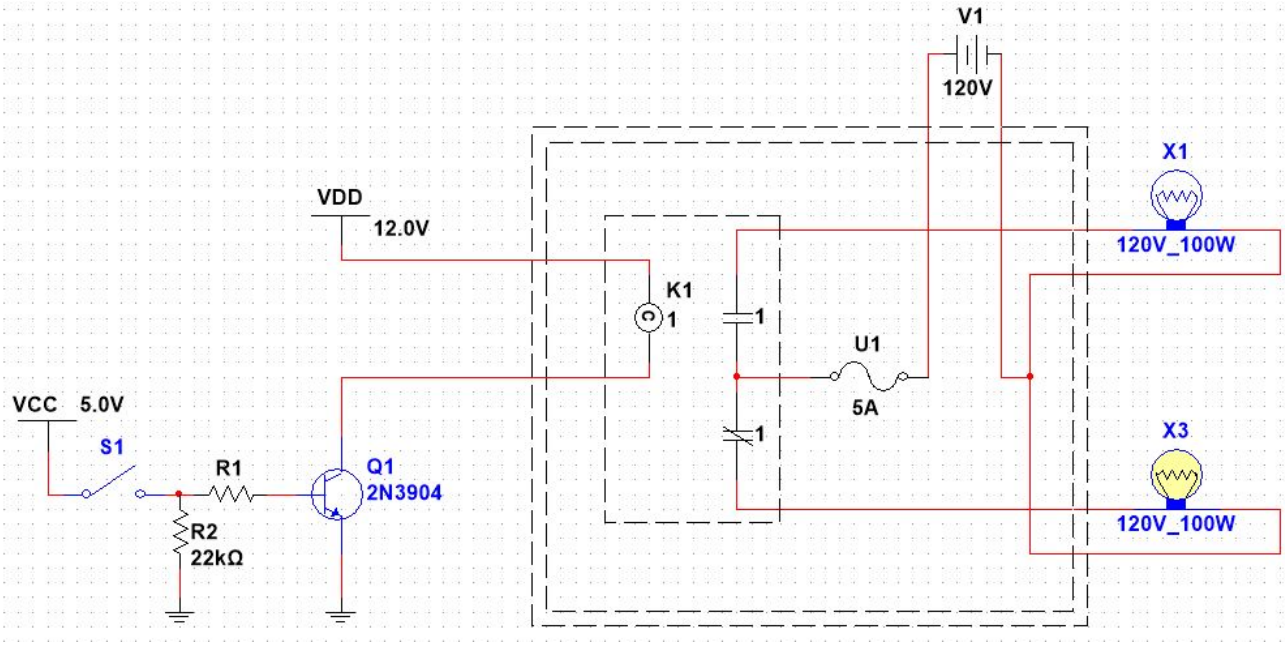
Online Homework System

Assignment Worksheet
12/20/22 - 4:27:06 PM MST

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA08 BJT Relay Driver Activity

Question 1: (10 points)

The following circuit shows the contents of a relay kit designed for this and other AC-controlled devices. It also shows the transistor drive circuit you will need to partially design.



This circuit has no protection for the transistor -- we'll fix that later.

Given that the relay coil draws close to 50 mA, and that a 2N3904 transistor has a minimum beta of 100 and an ON V_{BE} of about 0.7 V, determine a suitable Base current-limiting resistor. (Choose a value that's just less than half the calculated maximum value to ensure saturation.)

_____ kΩ

Construct the circuit on your breadboard, and attach the 12 V jumper connections to the relay switch box available in the lab.

Attach two lamps to the duplex receptacle. The two outlets are isolated from each other, with one driven by the N.O. (normally-open) contacts and one by the N.C. (normally-closed) contacts.

Close and open the switch, and ensure that the system is working, and that the lamps alternate being ON and OFF. When the switch is closed, _____

Use the oscilloscope as follows:

- Use channel 1 to observe the input to your transistor switch (between the switch and the Base resistor)
- Use channel 2 to observe the voltage at the collector
- Set the Horizontal time base to 500 μs/div
- In the TRIGGER section

- choose Channel 1 as the source
- change the trigger mode to "Normal"
- set the slope to "Falling"
- set the trigger level to about 2.5V.

In this configuration, the scope should only display signals when the switch is opened, which is when we are in danger of damaging the transistor. With no protection diode, the voltage generated by the inductive spike from trying to stop the current instantly will be fairly large, so adjust the channel 2 vertical attenuation until you can actually see the top of the signal. The inductive coil may go into a high-voltage oscillation.

TRUE/FALSE: The Collector voltage never rises above approximately 12 V.

(a) True
(b) False

In the manufacturer's specification sheet, the reverse breakdown for the 2N3904 (which we normally try to avoid) is listed at 30 V, so this means the transistor is entering reverse breakdown, where it conducts with a relatively low resistance and is in danger of being burned out.

Protection Diode

Now, place a diode (1N4005), reversed biased (i.e. Cathode to +12V) across the relay coil.

Adjust the time base until you can see the entire "bump" that settles to +12 V after the transistor shuts off. Observe and record the "Maximum" voltage now. Record your results below.

_____

The maximum voltage with the diode in place is controlled by

(a) The diode's forward barrier potential, referenced to ground

(b) The diode's reverse breakdown voltage

(c) The diode's forward barrier potential, referenced to V_{DD}

(d) The transistor's reverse breakdown voltage

Adjust your oscilloscope settings so that:

- the signal across the transistor is maximized for viewing
- the input signal channel settings are identical to the transistor signal channel settings for quick comparison
- The maximum voltage across the transistor is displayed in the measurement area

Ask your instructor to give you a grade out of five marks. _____

After Notes

You may notice that the input signal at the Base resistor plunges well below zero when the switch is opened. This is part of recovery from saturation, as the Carriers in the Base to Emitter P-N junction are displaced while the junction returns to its normal OFF condition. If the Base resistor was closer to the theoretically-calculated value, this negative spike would not be so pronounced, as the transistor would not be so deeply saturated. You might want to play with that.

Also, you may want to change the trigger to Rising Edge to see what happens when the switch is closed, as well as when it is opened. You should discover that there is no inductive spike when turning on a relay -- just when trying to turn it off instantly.

The configuration of your oscilloscope's trigger described above is typical for capturing "transient" events -- ones that are not periodic, and therefore unlike most of the signals you've used an oscilloscope for up to this point.

Online Homework System

Assignment Worksheet
5/20/22 - 9:28:49 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Totem Pole and H-Bridge Configurations

Question 1: (1 point)

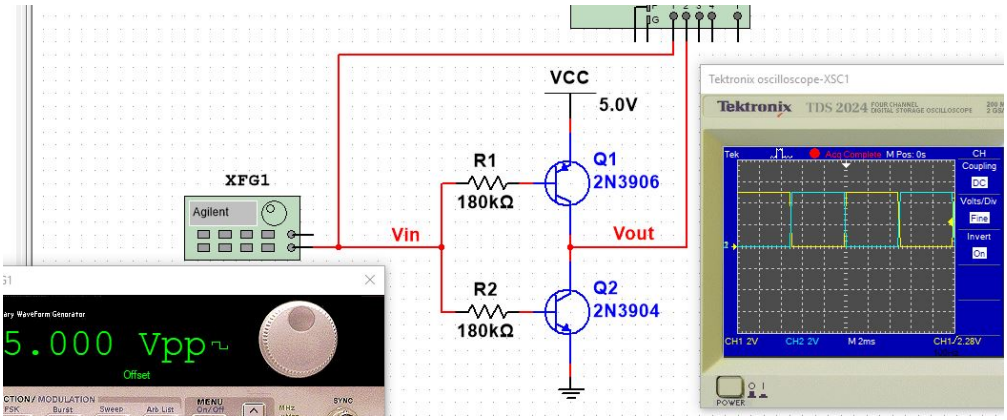
Totem Pole and H-Bridge Configurations

Up to this point, every circuit we've designed using semiconductor devices has had something to limit the current in series with the diode or transistor, since the resistance of a conducting semiconductor device is very low, and could allow a dangerous flow of current, usually resulting in thermal destruction of the semiconductor device.

The Totem Pole configuration, and the related H-Bridge bidirectional device driver, do not have resistors in series with the transistors. Instead, current is controlled by having one or the other of two series transistors turned off at any given time.

Totem Pole

Build the following circuit using Multisim, and verify its operation as indicated below.



Be very careful with the orientation of the two transistors -- the PNP transistor's Emitter is at the top!

Also, be careful with the setup of the function generator -- it's producing a square 0 to +5 V pulse, which, for the Agilent generator, requires an amplitude of 5 $V_{p\text{-}p}$ and a DC offset of 2.5 V_{DC}.

1. When the input voltage (Channel 1) is at 0.0 V, what is the output voltage? _____ V
2. When the input voltage is at +5 V, what is the output voltage? _____ V
3. From a logic perspective, what is this circuit? _____

Remove the oscilloscope and the function generator, and instead connect V_{in} to ground and place a current and voltage (AV) probe on the wire between the Collectors of the two transistors.

4. How much current is flowing through the transistors, to the nearest microamp? _____ μA

Now, connect V_{in} to +5 V instead.

5. How much current is flowing through the transistors now, to the nearest microamp? _____ μA

Place a current probe on the wire to R_2.

6. How much Base current is flowing to the NPN transistor? _____ μA

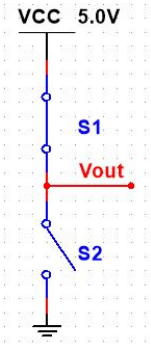
Analysis

What we have built is a logic inverter (inverting transistor switch) that doesn't draw any current through what would normally be considered its main circuit path. Let's determine why.

7. When the input signal is at ground, how much Base current can flow through Q_1, the PNP transistor, assuming V_{BEon} is 0.7 V for both transistors? _____ μA

8. If current is flowing through Q_1's Base, it is likely to be _____ , and can be pictured as a(n) _____
9. When the input signal is at ground, how much Base current can flow through Q_2, the NPN transistor? _____ μA. This means that Q_2 can be pictured as a(n) _____

With the input signal at ground, we can model our transistors as in the following picture:



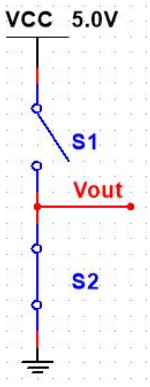
It should be fairly clear from this model that:

- V_{out} is directly connected to V_{CC}, so it will be +5 V
- No current can flow because Q_2 is in cutoff.

Let's investigate the opposite condition.

10. When the input signal is at +5 V, how much Base current can flow through Q_1, the PNP transistor, assuming V_{BEon} is 0.7 V for both transistors? _____ μA
11. With no current flowing through Q_1's Base, it will be _____ , and can be pictured as a(n) _____
12. When the input signal is at +5 V, how much Base current can flow through Q_2, the NPN transistor? _____ μA. Assuming the transistor will be either saturated or cut off (not in the active region), this means that Q_2 can be pictured as a(n) _____

With the input signal at +5 V, we can model our transistors as in the following picture:



It should be fairly clear from this model that

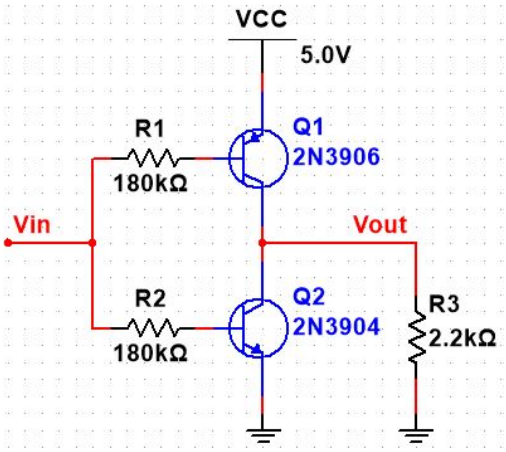
- V_{out} is connected directly to ground and is therefore at 0 V
- No current can flow because Q_1 is in cutoff

The Totem Pole arrangement therefore provides us with a clear voltage output, suitable for digital logic, without requiring any current through the main path of the transistors. Unfortunately, there is still some Base current required to saturate the "on" transistor in each case. When we study Field Effect Transistors, we'll discover that they also eliminate the need for any controlling current, and are therefore even more efficient than the BJT Totem Pole.

Totem Pole Device Driver

In and of itself, the Totem Pole configuration has no current path. However, when it is connected to a load, current will flow through that load when the Totem Pole creates a potential difference across the load. Since the transistors act as current sources, they can be designed to provide considerable current when required.

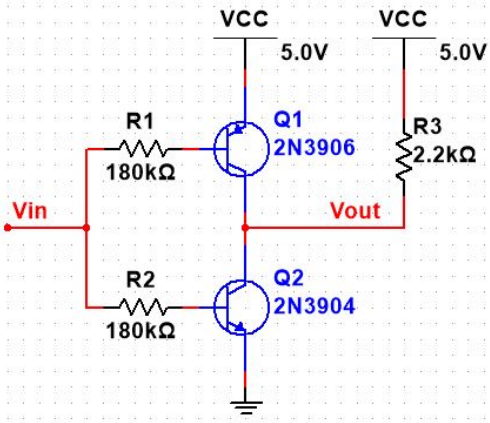
Let's go back to our original circuit, but this time with a load to ground.



In this case, current will flow through the load when V_{in} is LOW, because at that point V_{out} will be HIGH (at +5 V), so a potential difference will exist across the load resistor.

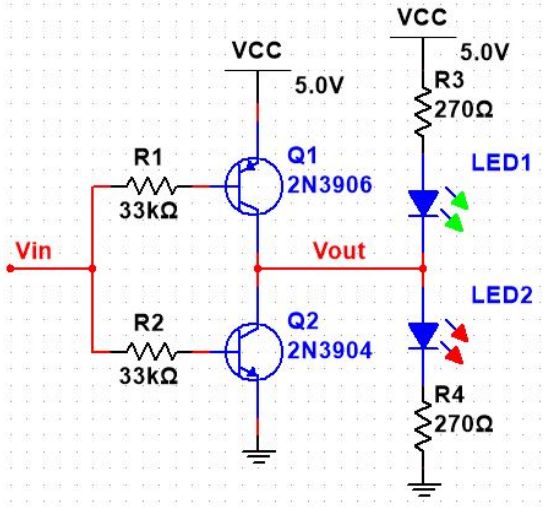
13. How much current will flow through the load when V_{out} is at +5 V? _____ mA
14. Given that the Base current for Q_1 is 23.9 μA from previous calculations, what current gain (β) would be required to produce this load current? _____ Since this is within the specified range of values for the 2N3904 and 2N3906, the transistors will still saturate when so needed.
15. When V_{in} is HIGH, how much current will flow through the load resistor? _____ mA

Now, consider the following arrangement:



16. This circuit will draw current through the load resistor when V_{in} is _____ because V_{out} will be LOW, providing a potential difference from +5 V to ground across the load.

Here's an interesting variation on the circuit. Try this in Multisim. It seems that, having two properly-biased LEDs connected together between +5 V and Ground, both of them should glow dimly -- until you consider the action of the Totem Pole transistors.



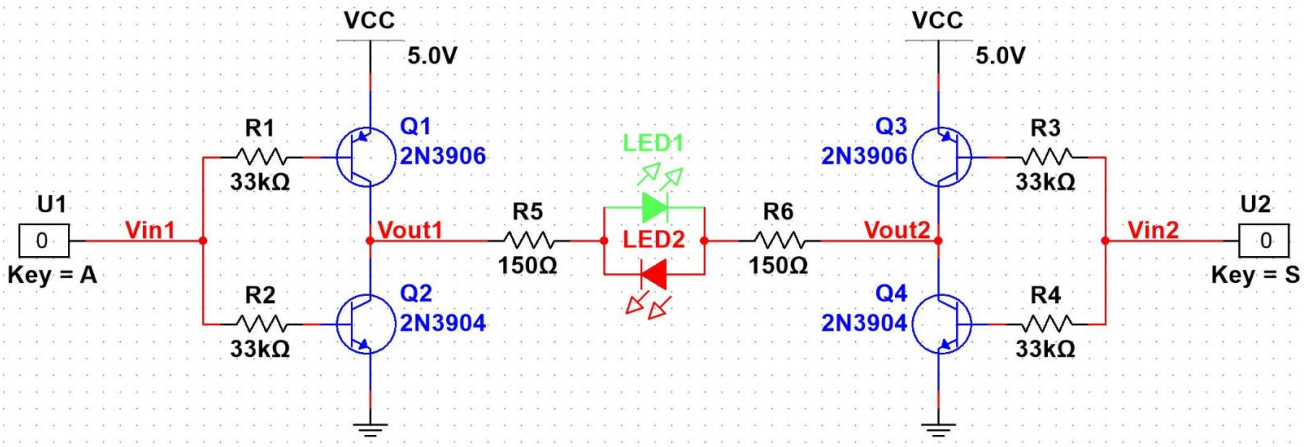
17. Assume that the forward barrier potential of each of the LEDs is 2.0 V. When V_{in} is LOW, V_{out} is HIGH. How much current will flow through the Green LED, LED1? _____ mA
18. When V_{in} is LOW, how much current will flow through the Red LED, LED2? _____ mA
19. So, when V_{in} is LOW, _____
20. When V_{in} is HIGH, V_{out} is LOW. How much current will flow through the Green LED? _____ mA
21. When V_{in} is HIGH, how much current will flow through the Red LED? _____ mA
22. So, when V_{in} is HIGH, _____

Notice that the Base resistors are considerably smaller in this example, in order to provide sufficient current to drive the LEDs. If you want, you can double-check to see if they provide sufficient Base current to saturate the transistors.

From this example, we've discovered that the Totem Pole configuration can selectively activate one of two connected circuits. The H-Bridge takes this control one step further.

H-Bridge Bidirectional Device Driver

The H-Bridge is made of two Totem Poles with a load between them, often a reversible DC motor. In the circuit below, two LEDs, mounted in opposite directions, will be used instead to show the direction of current flow.



Again, you can build this circuit in Multisim to verify its operation. If you want, you can use an "INTERACTIVE_DIGITAL_CONSTANT" for each of V_{in1} and V_{in2}.

23. From what we learned about this device before, we should be able to fill in the following table.

V_{in1}	V_{in2}	V_{out1}, V	V_{out2}, V	$V_{out2} - V_{out1}$, V	LED1	LED2
LOW	LOW					
LOW	HIGH					
HIGH	LOW					
HIGH	HIGH					

Note that there are two possible combinations for turning off both the LEDs, or in a motor H-Bridge, to turn off the motor: 00 and 11. This mirrors the operation of an Exclusive OR, with the exception that the two "True" output conditions are electrically opposite to each other.

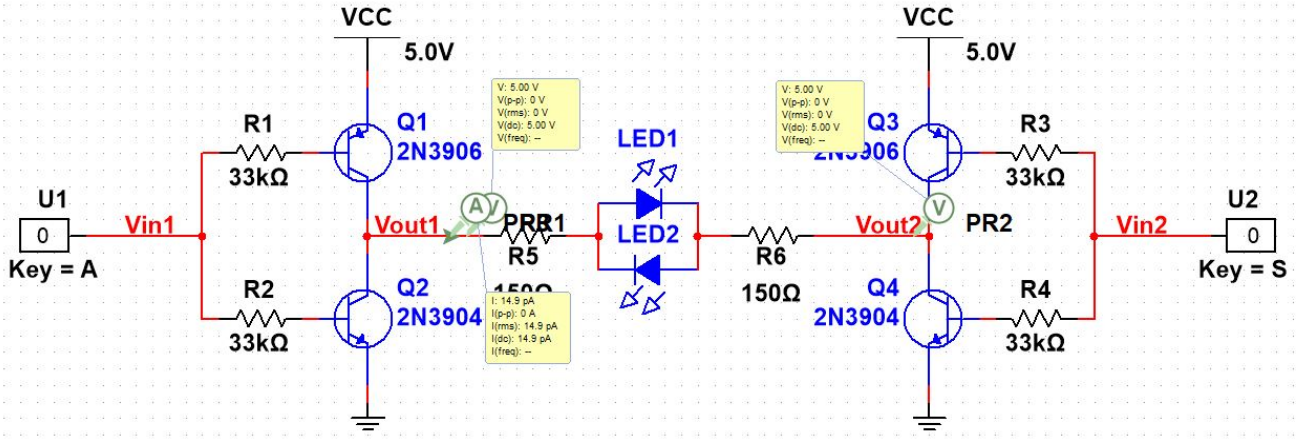
In an H-Bridge used to drive a bidirectional motor, there would need to be protection for the transistors against the inductive currents generated by the motor when the transistors attempt to turn the motor off. In this case, unlike in the case of the relay driver, we can't simply put a diode across the motor, because in one direction it would conduct, taking all of the current away from the motor and likely burning out. Instead, either of three techniques are employed:

- a ***Snubber Capacitor*** is typically placed across the motor to prevent the voltage from rising instantly by temporarily storing the charge and restoring it to the motor coils where the energy can be dissipated as heat.
- ***two zener diodes***, in series back to back, allow for the normal operating voltage, as the zener breakdown is chosen to be greater than the power supply voltage; however, the inductive spike will cause the reverse-biased zener to break over, thereby conducting through the forward-biased zener, effectively holding the spike voltage to $V_Z + V_D$ in either direction.
- ***protection diodes*** mounted in reverse-bias across all four of the transistors will also provide paths for the inductive current, although the path will vary depending upon which way the motor was turning when the transistors were turned off and which transistors were turned off.

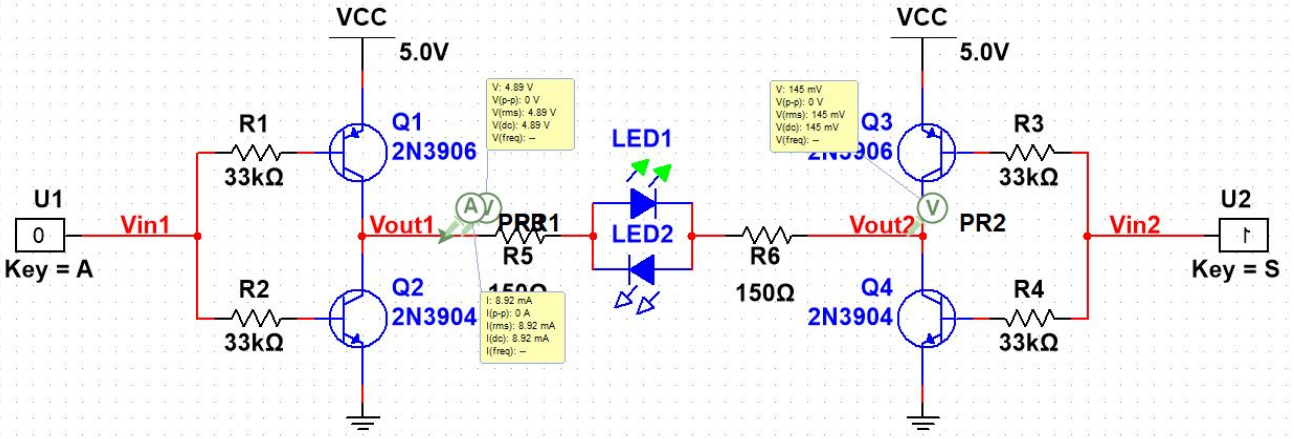
The following images are screenshots showing the voltages and currents for the circuit above, for the four possible logic combinations. Look particularly at:

- Voltage levels in combination with the input levels
- Current flow and direction
- Which LEDs are glowing

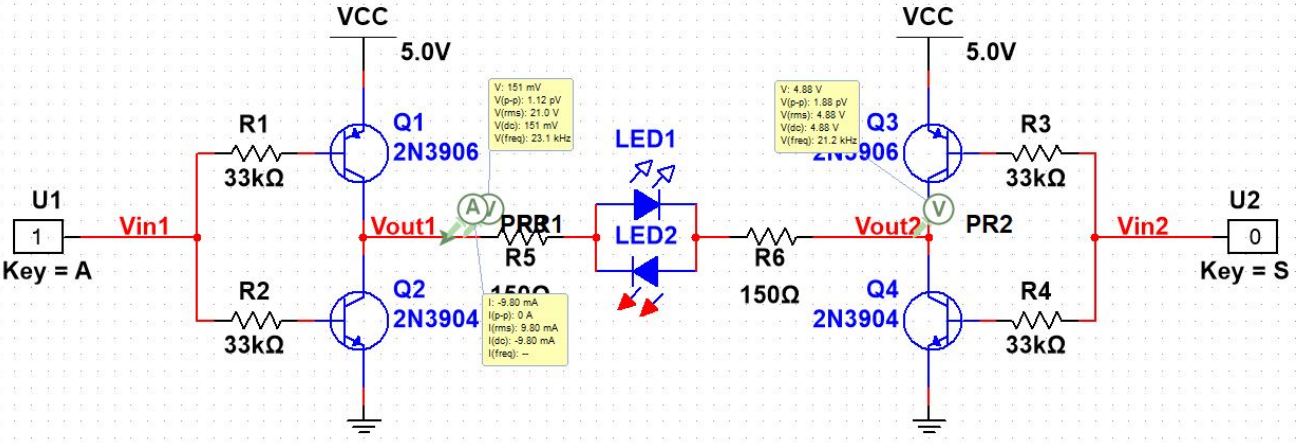
Inputs 00



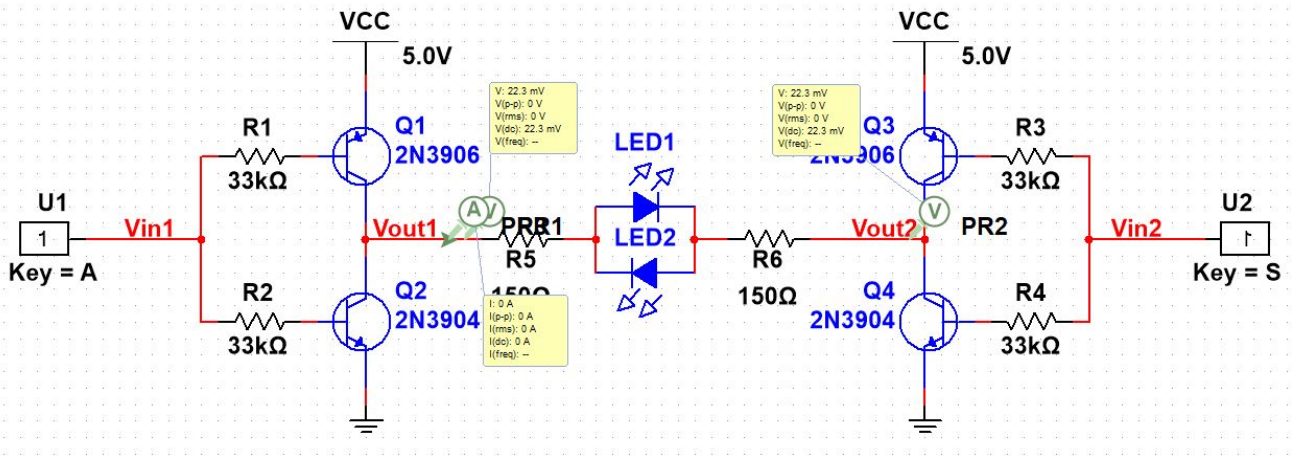
Inputs 01



Inputs 10



Inputs 11


VCC
5.0V
R1
33kΩ
Q1
2N3906
U1
1
Vin1
Key = A
Vout1
R2
33kΩ
Q2
2N3904
R5
LED1
LED2
R6
150Ω
VCC
5.0V
Q3
R3
33kΩ
Vout2
PR2
Q4
2N3904
R4
33kΩ
Vin2
U2
1
Key = S

Online Homework System

Assignment Worksheet
2/13/23 - 12:10:37 PM MST

Name: _____ **Class:**

Class #: _____ **Section #:** _____

Instructor: Ross Taylor **Assignment:** Project 2 Totem Pole and H-Bridge Configurations

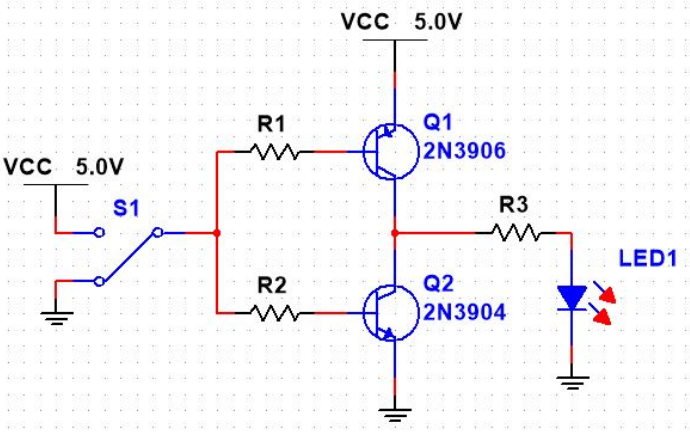
Question 1: (50 points)

Project 2 Preparation

Note: Do not move on to the "Next" page until you have completed this question. The next page is the Practical Activity, and once you move to that page, you will not be able to return to this page!

Totem Pole

Consider the partially-complete schematic diagram below to answer the following questions.



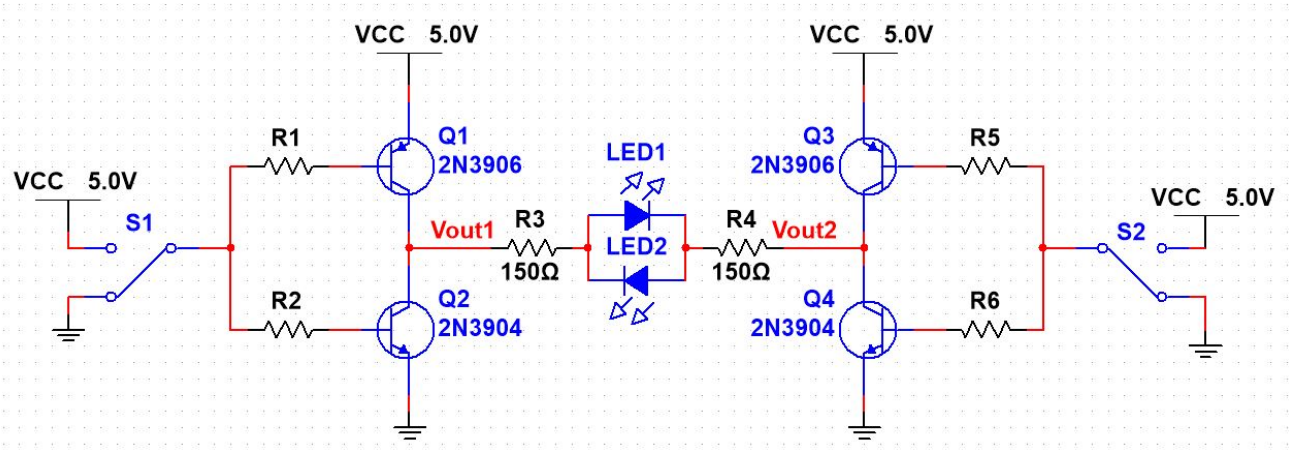
1. Assume the following: When the LED is ON, it is being powered from +5 V through a single transistor's V_{CEsat} which we will consider to have a magnitude of 0.1 V; its forward barrier potential is 1.8 V; the current required is 12 mA. What ideal resistance for R_3 would provide this current? (Don't pick a standard value yet.) _____ Ω
2. Pick the next biggest standard 10% resistor value for R_3 (the list is at the end of the formula sheet in Moodle; these are also the values that are in you ETC component kit). _____ Ω
3. Assuming that β=100 (worst case for the 2N3904 and 2N3906 transistors), what Base current is required to produce a 12 mA Collector current? _____ μA
4. Assuming that V_{BEon} for the transistors has a magnitude of 0.7 V, what ideal resistance would provide the required Base current? (They should be the same -- you could verify that, if you wish.) _____ kΩ
5. Pick a standard 10% resistor value for R_1 and R_2 that's just ***less*** than half of the ideal resistance, to ensure that the transistors saturate. _____ kΩ

Verify the Design

6. Determine the Base current using the Base resistor you chose. _____ μA
7. Determine the Collector current predicted using the Active Transistor Model: _____ mA
8. Determine the maximum Collector current, given the Diode resistor you chose, V_{CEsat}, and the forward barrier potential of the LED: _____ mA
9. Based upon this information, the transistor you've been analyzing would be _____
10. If the V_{CEsat} for the transistors has a magnitude of 0.1 V, using the appropriate model, the highest voltage expected at the junction of the Collectors would be _____ V and the lowest would be _____ V
11. The LED should glow when the input switch is connected to _____

H-Bridge

Consider the schematic below to answer the questions that follow.

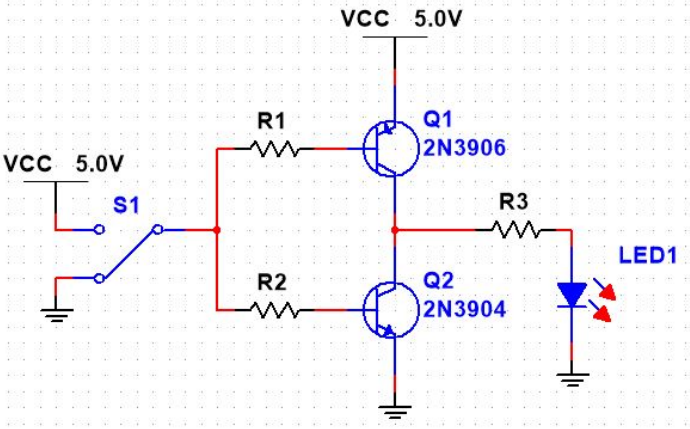


12. Fill in the following table to predict the behaviour of this circuit.

S1, V	S2, V	LED1	LED2
0 V	0 V	_____	_____
0 V	+5 V	_____	_____
+5 V	0 V	_____	_____
+5 V	+5 V	_____	_____

Simulation

In Multisim, build the Totem Pole circuit you analyzed earlier, shown here again for convenience:



- The switch is "SPDT"
- Make sure you know which pins are which on the two transistors, and that you have them connected correctly

13. Place one voltage probe at the input (i.e. at the switch) and one at the two Collectors. Verify the following: When the input is HIGH, the output is _____ and the LED is _____ .
14. Take a screen-shot of your simulation showing the conditions in the question above for a grade out of three marks. Document Upload (Direct)

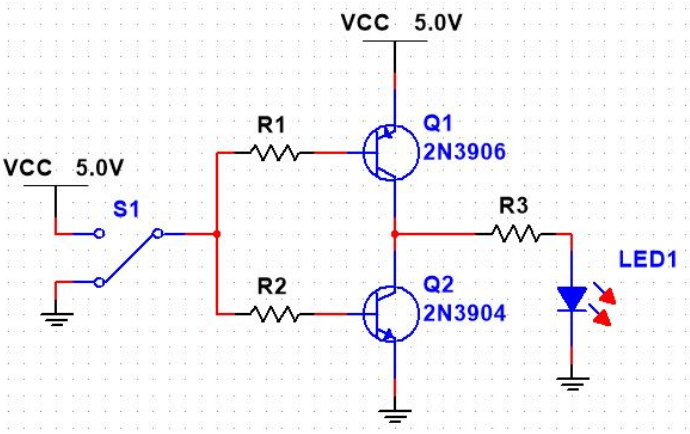
You have now completed the Preparation and Simulation. You may Save and Close or move on to the Practical Activity page, but do not "Submit" until you have completed the Practical Activity!

Question 2: (50 points)

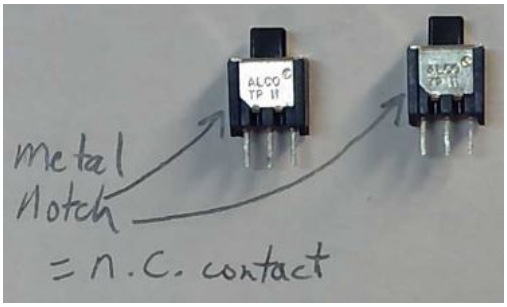
Project 2 Practical Activity

Totem Pole

Using your breadboard, build the circuit below, using the resistors from the Preparation Activity (you may want to verify these with your instructor). More instructions to follow.



- Use a DC power supply for VCC.
- The switch is a push-button SPDT (single pole double throw) switch from your "CNT Year 1 Kit", shown below. Note that it has three pins, as indicated in the schematic.



- Make sure the three pins are in separate vertical rows on your breadboard before you connect anything to them! Connect Ground to the N.C. contact (N.C. = normally closed), Connect +5 V to the pin on the other side (normally open or N.O. contact), and use the middle pin as your input to the Base resistors.
- Be very careful to connect the transistors correctly:
  - take special note of which one is 2N3904 and which is 2N3906
  - look up the pinout so you know which pins are which
  - make sure the emitter of the PNP device is "up" and the emitter of the NPN device is "down", as shown on the schematic.

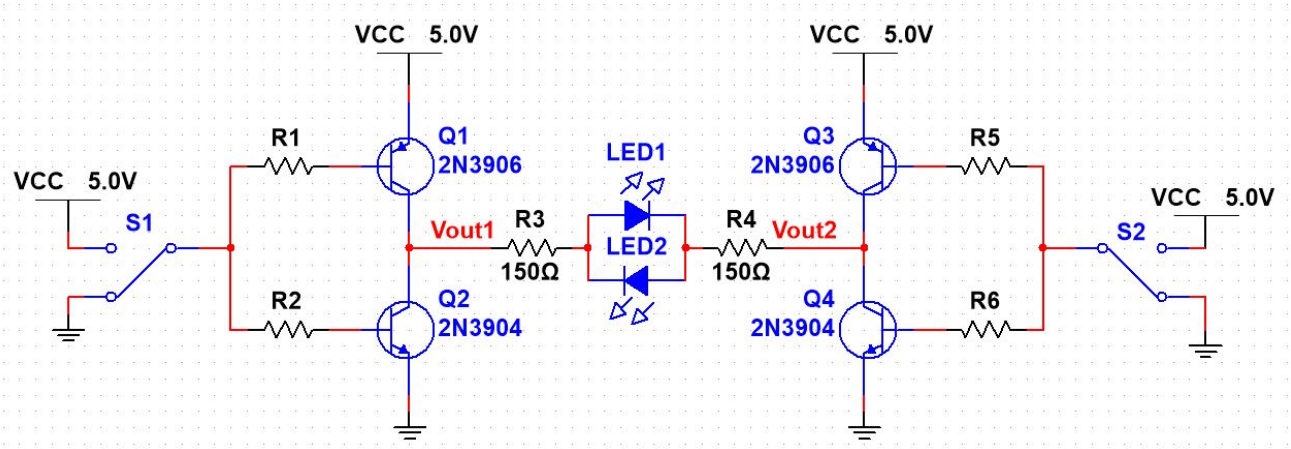
1. Use your DMM to measure and record the following voltages, where V_{out} is measured at the node containing the two transistor Collectors.

Pushbutton	V_{in}, V	V_{out}, V	LED
Released	_____	_____	_____
Pressed	_____	_____	_____

H-Bridge

Modify your circuit to create the following H-Bridge. You may not have enough of one of the resistor values, in which case make two of them the next smaller value. You can choose whether to put the two different values on the same Half-Bridge or on the two 2N3906 transistors -- it doesn't make a lot of difference where they go, as there's a lot of freedom in resistor choice for transistor switches. PNP transistors are a bit harder to switch than NPN, so driving them harder into saturation is probably the best choice.

Note that the LED current-limiting resistor has been split into two resistors that add up to slightly more than the chosen value -- this wasn't really necessary, but it's *so* much more symmetrical!



Fill in the following table to verify your circuit's operation. Consider LED1 to be "forward" rotation of a motor, and LED2 to be "reverse" rotation of the motor.

S1	S2	LED1	LED2
Released	Released	_____	_____
Released	Pressed	_____	_____
Pressed	Released	_____	_____
Pressed	Pressed	_____	_____

For a grade out of six marks, ask your instructor to verify the operation of your circuit. _____

You have now completed this Practical Activity. Once you submit your results, you will not be able to access this activity again.

Online Homework System

Assignment Worksheet
5/20/22 - 9:29:21 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Field Effect Transistors (FET)

Question 1: (1 point)

Field Effect Transistors

Some of you may remember from your Biology classes that scientists make a distinction between "homologous" traits that can be shown to be related, and "analogous" traits that have the same functionality but are in no way related. In our study of BJTs, the PNP and NPN devices could be considered "homologous" in that they were clearly related in the way they were made and in the way they operated. When it comes to comparing BJTs and FETs, however, there is no "relatedness" between the way these devices are made, and yet, in a general sense, their behaviour is "analogous", in that they both respond to a manipulated input in order to control current flowing from a large DC source. And that's about all they share in common.

BJTs were Current-controlled Current Sources, where a small current injected into the Base controlled a large Collector to Emitter current.

FETs are Voltage-controlled Current Sources -- a voltage applied to a Gate controls a large Drain to Source current.

With the BJT, we could perhaps picture the action as using a small flow of water to erode a dam to let a large flow of water through. With a FET, we instead picture a clamp squeezing a pipe to stop the flow of water through the sluice. Nothng about the clamp ends up "getting wet" -- it is entirely outside of the conductive flow.

This is a good time to once again try to refine your understanding of the two basic elements of electricity: Current and Voltage. Current refers to the movement of electrical charge carriers through a conductor, whereas Voltage refers to electrical pressure or force. The two are not interchangeable, and should never be confused: Voltage is a potential difference between two points that could cause a current to flow. Voltage exists whether or not current is flowing. Current only flows if there is a conductive path from a higher potential to a lower potential. It is possible to have a very high potential difference with no current because the resistance is effectively infinite, and it is possible to have a huge current flowing with an almost unmeasurably small voltage if the resistance is nearly zero -- that's the scenario that exists for a few milliseconds when a mechanic drops his wrench across the terminals of a car battery: a dead short across the battery terminals will mean essentially zero volts, but the current will be hundreds of amps before the wrench explodes in a shower of molten iron.

Field Effect Transistors use an electric field (in essence, a potential difference or voltage) to control a current through a conductor by external means.

The simplest of these is the JFET, which can be pictured as in the meme below:

"Big Sister" is crimping the garden hose, and is about to let it go to allow a spray of water to hit her unsuspecting little brother's face. "Big Sister" doesn't get her hands wet because she is applying an external force (analogous to voltage) to the garden hose to prevent the flow (analogous to current). The natural condition of a garden hose it to allow water to flow; only by applying an external force can the current be stopped. That's the JFET.

The most common FET is called an Enhancement-Only MOSFET (E-MOSFET), and it is more like a spring clamp on the IV tubing in a hospital: Its natural condition is to prevent the flow of current, and a counteracting force needs to be applied to open up the channel to allow current to flow.

In between these two is an almost-nonexistent FET called the Depletion and Enhancement MOSFET (D-MOSFET) which behaves a lot like the JFET in that current normally flows and an external voltage needs to be applied to reduce or stop that flow, but putting a counteracting voltage across the device will allow even more than the normal current to flow.

_____

Question 2: (1 point)

Junction Field Effect Transistors

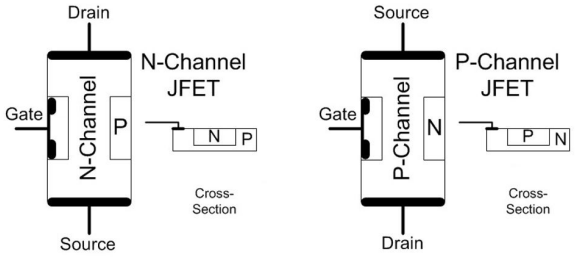
As previously mentioned, JFETs are almost entirely different from BJTs. They would be as different as a mouse and a huge beetle: both have hard skeletons, but one is internal, the other external; both can walk, but there are no similar parts to their legs; even the number of legs is different.

Here's a table of contrasts between the BJT and JFET:

BJT	JFET
Made of three layers	Made of two layers
Two P-N Junctions	One P-N Junction
Hole and Electron Carriers	Hole or Electron Carrier
Normally OFF	Normally ON
Base Current turns ON current	Gate Voltage turns OFF current
Linear Transfer Function	Parabolic Transfer Function
Base, Collector, Emitter	Gate, Drain, Source

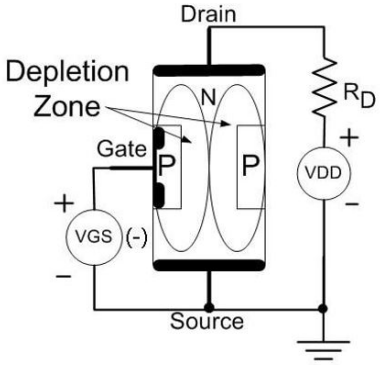
The JFET isn't a very good transistor, and it's not very commonly used. However, in order to understand how FETs work, the JFET is a good starting point. (We're on a journey from a not-very-good transistor to a practically-nonexistent transistor before we can get to the took-over-the-world transistor; so stay tuned!)

Although the JFET has only one P-N Junction, there are three metal connections to the material. Two of them are connected to the opposite ends of one of the types of material, and the third metal connection is to the other material, which is "wrapped around" the other material, as shown below.



FETs use the term "Channel" to describe the path for current through the device, and that makes sense when you look at these block diagrams. The N-Material in the N-Channel JFET is just a good conductor with a metal connection on either end -- ready to conduct if a potential difference is placed across it. That explains why its normal condition is "on". Of course, there will be a depletion region around the P-N Junction that has no carriers in it, which will somewhat narrow the channel, but the channel is open for current flow.

However, if the P-N Junction is reverse biased, the depletion region will get larger, thereby narrowing the channel and restricting current flow. At some point, the depletion region will completely take over the channel, and no further current will flow. That is shown in the following biased diagram of an N-Channel JFET.

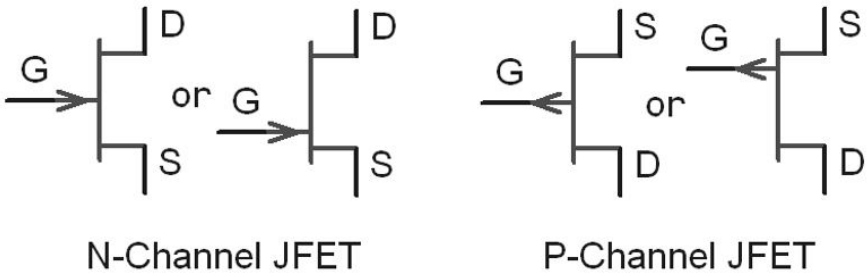


In order for the P-N junction to be reverse-biased, the P material (the Gate) must be at a lower potential than the N-Material in the channel. Of course, when the transistor is conducting, there's not much difference between the two ends of the channel; but when the channel is no longer conducting, there's a big difference. Therefore, we reference the Gate's voltage to the voltage at the Source, and the

controlling voltage is called V_{GS}. In this block diagram, V_S is at ground, or 0 V, therefore to reverse bias the P-N Junction, the Gate voltage must be negative. Since V_{GS} means V_G - V_S, this means that V_{GS} must be negative for an N-Channel JFET. If the P-N Junction was ever forward-biased, it would just turn this device into a very poor diode, since the Gate is not designed to handle any current.

Notice that the labelling convention we used for the BJT carries on here -- a doubled subscript V_{DD} to indicate a power supply that biases the Drain, R_D to indicate a resistor biasing the Drain, and a double subscript V_{GS} to show the difference in potential between two pins on the device.

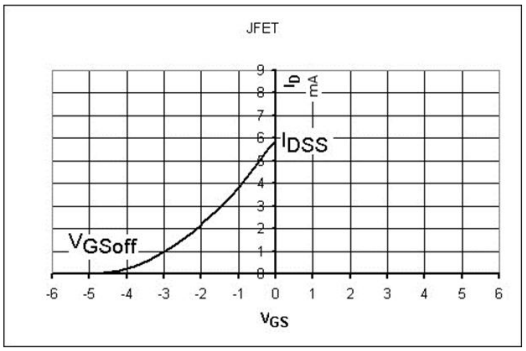
In a schematic diagram, the following symbols are used for JFETs:



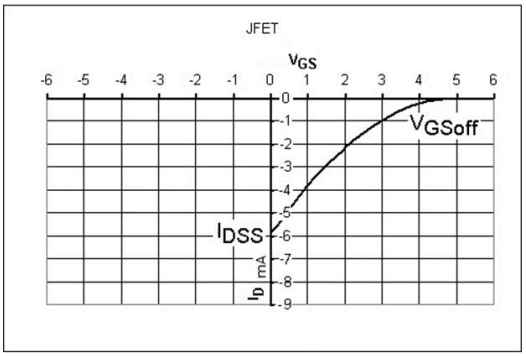
N-Channel JFET P-Channel JFET

The symbols are based upon the construction of the devices: The vertical bar is the Channel, with the metal connections for the Drain and Source attached. The Gate is shown influencing the channel through a P-N junction, where the arrow indicates which material is P and which is N, just as in the diode. Often the Gate is shown closer to the Source to help us remember that V_{GS} is the controlling voltage.

As mentioned before, the Transfer Function for the JFET is non-linear; parabolic, in fact, as shown below.



N-Channel



P-Channel

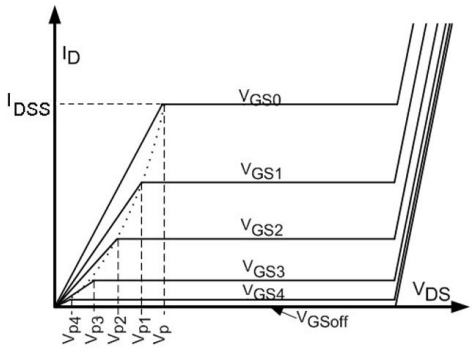
To be more specific, the Transfer Functions are half-parabolas that terminate at two points: V_{GSoff} and I_{DSS}. It probably comes as no surprise that the graphs for the N-Channel devices and the P-Channel devices are inverted to each other. Here's a bit of a summary:

Characteristic	N-Channel	P-Channel
V_{GS} - controlling input voltage	Negative	Positive
I_D - controlled output current	Positive	Negative
V_{GSoff} - voltage at which I_D becomes zero	Negative	Positive
I_{DSS} - maximum current that can flow	V_{GS}=0	V_{GS}=0
Forbidden input voltage range	V_{GS}>0	V_{GS}<0

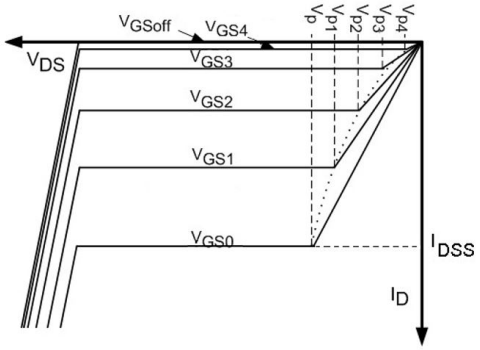
V_{GSoff} and I_{DSS} are transistor characteristics given in the specification sheet, just as V_{BEon}, α, and β were given for the BJT.

If V_{GS} goes past V_{GSoff}, the transistor remains off -- the parabola doesn't rise up again as it would mathematically. In other words, the parabolic shape only helps us predict voltages and currents between V_{GSoff} and I_{DSS}.

When put on a Curve Tracer that holds V_{GS} constant while increasing the voltage across the transistor, V_{DS}, we get a family of curves similar to those for the BJT, with some very noticeable differences.



N-Channel JFET



P-Channel JFET

First, it may be noticeable that the flat lines in the Active Region are really flat, which means that these devices have a very high internal impedance when they are working as Current Sources. That's what JFETs do best -- act as almost-ideal current sources, holding the current constant regardless of the voltage across the device, at least between what's called the "Ohmic Region" and Reverse Breakdown.

Second, the spacing between the different traces isn't constant as it was for the BJT -- it increases in size in proportion to the square of the input voltage.

Third, the voltage at which the device enters the Active Region isn't a tiny little voltage like V_{CEsat} was for the BJT. In fact, V_p could be 2 V, 3 V, even values like 10 V, which doesn't make the JFET a very good switch. Switches are supposed to have essentially zero volts across them.

Finally, the points at which the device enters the Active Region fit into a half-parabola, which just so happens to match the half-parabola in their Transfer Functions.

Questions:

In one JFET circuit, V_G = +10 V, V_S = +10 V, and V_D = 0 V.

1. If this device is wired properly, is it N-Channel or P-Channel? _____
2. V_{GS} = _____ V; would you expect to see maximum current or zero current? _____
3. Would you have to raise or lower V_G to change the current? _____

In another JFET circuit, I_D is positive.

4. If this device is wired properly, is it N-Channel or P-Channel? _____
5. Would V_{DS} be positive or negative? _____
6. Would V_{GS} be positive or negative? _____
7. To make maximum current flow, if V_S=0, what should V_G be? _____ V

Question 3: (1 point)

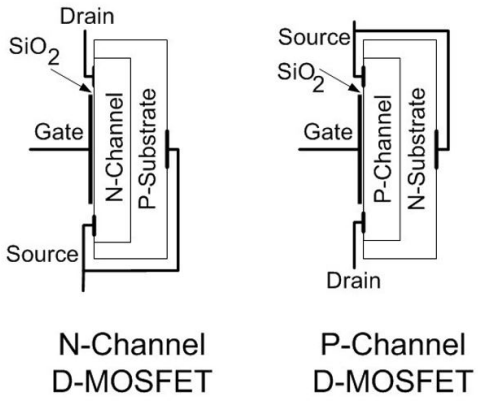
Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

Remember our analogy of comparing a mouse to a very large beetle? One of the biggest differences between the two, biologically, is that one is a vertebrate, and one is an invertebrate. However, when it comes to invertebrates, there are differences that are even more extreme than between the mouse and the beetle -- there are worm-like invertebrates, insect-like invertebrates, starfish-like invertebrates, clam-like invertebrates, and so on. The same is true, in a sense, for Field Effect Transistors.

A very different configuration for controlling a single channel of semiconductor material was invented, and the result is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). And, it this general category, there are a number of types of devices, generally arranged in two groups -- D-MOSFET and E-MOSFET.

D-MOSFET

We'll start with the Depletion and Enhancement MOSFET, because this will help us understand how the E-MOSFET works; the D-MOSFET isn't even a transistor you can buy as a component, so it's not something you will likely ever have any experience with. But unless you understand the concept of Enhancement, the operation of the E-MOSFET, which makes up by far the bulk of the transistors ever made, will be a mystery.



As with the JFET, the Drain and Source are connected to the two ends of one piece of material, which becomes the channel. However, unlike the JFET, the Gate is not connected to the other semiconductor material. Instead, it is simply a piece of metal separated from the channel by a thin layer of oxidized silicon, SiO_2, which is the same material sand is made of, and is a really good insulator. This is where the name comes from: Metal to Oxide to Semiconductor FET.

The biggest difference between the JFET and the MOSFET is that forward-biasing the Gate to Source potential does not turn this device into a poor diode, as it would have done in the case of the JFET, because no current can flow through the insulating layer at the Gate. Therefore, there is no "forbidden voltage range", other than going beyond the maximum voltages possible for the device.

There is a second metal connection that keeps the Substrate potential the same as the Source potential. This way, as V_{GS} changes, an electric field, or potential, is developed across the P-N junction without a physical connection to the Gate.

As with the JFET, when the P-N Junction is reverse-biased, the depletion region increases in thickness, reducing the Channel and thereby reducing the current. At some point, the Channel will be reduced to nothing, and the Channel will be turned off. As with the JFET, this will be V_{GSoff}.

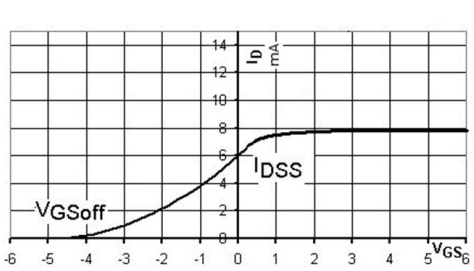
When V_{GS}=0, again a large amount of current will flow, and this will be called I_{DSS}. Incidentally, the term means "I_D when the Gate is Shorted to the Source", which is how they determine what I_{DSS} is. Of course, that same amount of current flows when the Gate and Source voltages are the same, whether or not they are physically shorted together.

However, in the case of the D-MOSFET, this isn't the maximum current that can flow, because we can take V_{GS} to the other side of the y-axis, since forward biasing doesn't damage the transistor. When we do this, the depletion region is actually decreased, which results in the widening of the channel, in turn resulting in more current than I_{DSS} flowing through the device. This widening of the channel is called ***Enhancement***. Enhancement can extend past simply reducing the depletion region to zero -- by forcing carriers of the opposite kind into existing semiconductor material, it can actually make a region of N-Material behave like P-Material or *vice versa*.

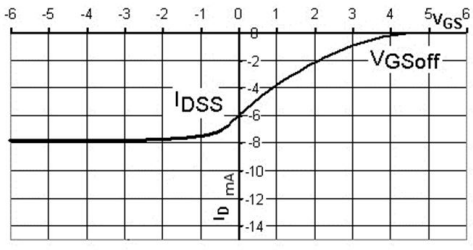
- ***Depletion*** referred to reducing the current by increasing the depletion region
- ***Enhancement*** refers to increasing the current by decreasing the depletion region and even pushing carriers past the original physical junction, creating new conductive material.

Consequently, this device is called the Depletion and Enhancement MOSFET, or simply D-MOSFET to try to keep the acronym small.

Here are the Transfer Functions for the only D-MOSFETs this author could find any information on, and they are buried inside an Integrated Circuit.



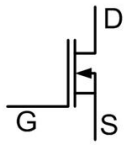
N-Channel D-MOSFET



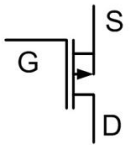
P-Channel D-MOSFET

Not very pretty -- most textbooks will show the enhancement-side of these curves as being a nice continuation of the parabola, but this doesn't appear to be the case. However, it shows that I_{DSS} and V_{GS}=0 are not the limits of operation for D-MOSFETs.

In a schematic, the following symbols are used:



N-Channel D-MOSFET



P-Channel D-MOSFET

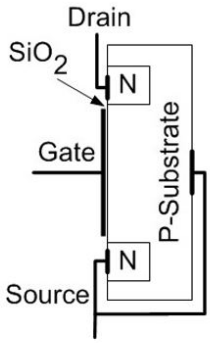
Again, the symbols are based upon the physical structure of the devices. The vertical bar is the channel, with metal connections to the Drain and Source. The Gate is shown as a metal layer physically separated from the channel by the thin layer of oxide, and the substrate connection indicates which material is P and which is N, with a metal connection typically between the Source and the substrate internal to the device.

Often, the Gate is shown with its connection close to the Source to remind us that V_{GS} is the controlling voltage.

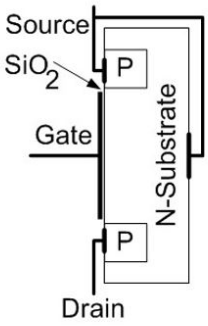
E-MOSFET

Finally! Now that we know what Enhancement is, we can get to the most common transistor ever made: the Enhancement-only MOSFET.

In an E-MOSFET, no channel exists in the resting state -- just two stubs of the channel material with a gap between them, filled with the substrate. This means that the P-N junctions around these stubs prevent the flow of current in the resting state, so, like the BJT, these devices are normally OFF, not ON as was the case for the JFET and the D-MOSFET.



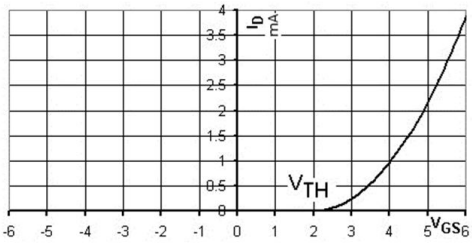
N-Channel E-MOSFET



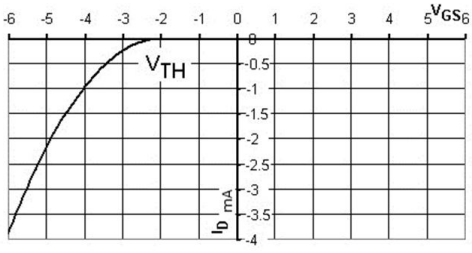
P-Channel E-MOSFET

Of course, reverse biasing these devices would simply further turn them off, which has no effect. However, forward biasing the Gate to Source potential actually pushes the carriers in the substrate away from the Gate, eventually to the point where the substrate begins to behave as an extension of the stubs of the channel; a channel is created where no channel existed before, and current begins to flow.

The Transfer Characteristics show this effect:



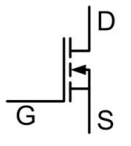
N-Channel E-MOSFET



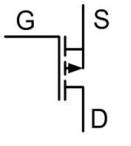
P-Channel E-MOSFET

Instead of V_{GSoff} we now have a threshold voltage, V_{TH} that must be overcome before the transistor will begin to conduct.

The schematic symbols for this device again show the physical characteristics of the device:



N-Channel E-MOSFET



P-Channel E-MOSFET

Notice that the Channels start off as broken lines -- they don't exist in the resting state, and only appear when the Gate to Source voltage is forward biased.

The E-MOSFET is more closely analogous to the BJT than the other FETs. Back to our biology analogy, we've come to, let's say, the octopus which, with its two big eyes and eight "legs" is more like the mouse than a clam would be; but they're really not at all related: they just both hide if you try to sneak up on them.

The E-MOSFET has the following characteristics that need to be considered when using it:

- Its output is non-linear, so it is best used as a switch rather than as an amplifier, unless it is used in a switch-mode (Class D) amplifier
- Its threshold voltage can be much higher than the 0.7 V required to turn on a BJT
- Its "On Resistance" is typically much lower than that of a BJT, usually in the milliohms
- Its "On Voltage" (V_{DSon}) is typically very close to zero, since there are no junctions to cross in the channel
- There is never any continuous Gate current, due to the insulating layer of SiO_2
- Unfortunately, the insulating layer is rather fragile, and can be damaged by Electrostatic Discharge (ESD), so FET devices need to be handled carefully and stored on static-dissipating foam
- Also unfortunate is the capacitance arising from the Gate-to-Channel separation, which results in an inrush current when the FET is turned on, a discharge current when the FET is turned off; the capacitance also may introduce a delayed response, since capacitors do not allow for instantaneous changes in voltage

Questions:

1. In one circuit, V_S = 0 V and V_D = +12 V. I_D increases continuously as V_G changes from negative to positive. What type of device is this? _____ _____
2. In another circuit, V_S = 0 V and V_D = -9.0 V. When V_G = 0 V, no current flows. However, as V_G passes -2.4 V, current begins to flow. What type of device is this? _____ _____
3. A technologist built a circuit using an N-Channel E-MOSFET. She applied +1.2 V between Gate and Source, but measured no current flowing through the Channel from Drain to Source. What is the most likely reason for this? _____
4. Our technologist from the previous question fixed her circuit. Being curious, she measured the Gate current. What do you predict she discovered? _____ μA

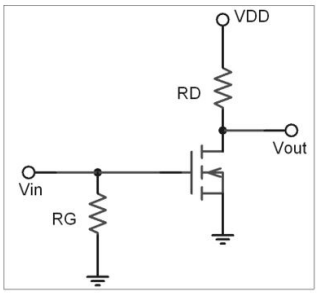
Question 4: (1 point)

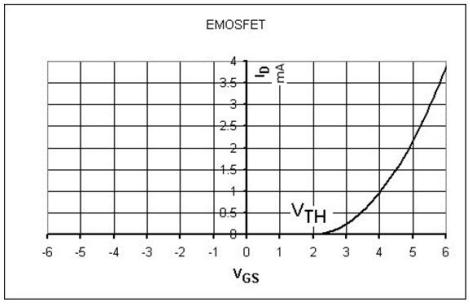
E-MOSFET Switching Circuits

As mentioned before, E-MOSFETs are best used as switching devices. They are typically used in either of two ways: as single transistor switches and as Complementary switching pairs in CMOS logic.

Single Transistor Switch

The component arrangement for a single transistor E-MOSFET switch is pretty similar to the BJT. However, the design must be based upon V_{GS} instead of I_B, as was the case for the BJT. Here's an example that will help us determine what we need to do to make a simple logic switch work.





1. If the minimum guaranteed input voltage is +3.5 V, what Drain current should be used when designing this circuit? _____ μA
2. If V_{DD} is +5.0 V, determine the minimum value for R_D _____ kΩ, then choose an available 10% resistor value that is close to double your calculated value to ensure the transistor saturates: _____ kΩ

3. When V_{in} is LOW (0 V), what voltage do you expect to see at V_{out}? _____ V
4. When V_{in} is HIGH (>3.5 V), what do you expect to see at V_{out}? _____ V
5. What logic function does this switch perform? _____
6. What would the output voltage be if the input was +2.75 V? _____ V. Is this a clear logic level? _____

Notice that we didn't have to do any calculations for R_G. That's because there is no Gate current, so the value of this resistor doesn't have any bearing on the basic design of the circuit. However, we usually put one, and sometimes two, Gate resistors into our design.

Pull-up or Pull-down Resistor

The resistor shown above is a pull-down resistor. If, for some reason, V_{in} was not connected, with no other components at the Gate any small residual charge or accumulated charge from static electricity would generate an unexpected and unpredictable V_{GS}, which could turn on the transistor. We didn't need to worry about that with our BJT switches, because their natural condition was OFF, and with no source of current connected, there was no chance of the BJT turning on.

The pull-up or pull-down resistor provides a path to either a positive voltage source or ground that will dissipate any charge on the Gate and provide a known input voltage. Using a resistor allows us to connect the signal source and over-ride the pull-up or pull-down resistor.

7. In the circuit above, the pull-down resistor establishes an input _____ if the signal source isn't connected.

Capacitive Surge Current Resistor

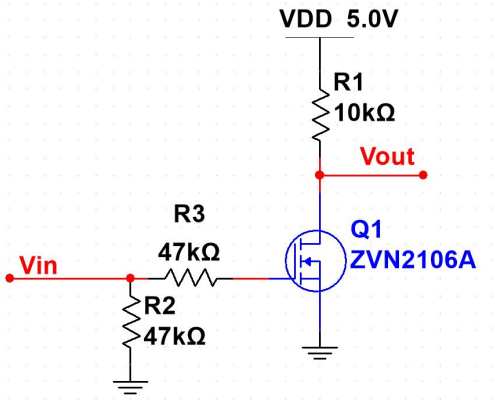
The other resistor that is frequently used at the Gate is put in ***series*** with the input voltage and the Gate. As you know, the voltage of a capacitor cannot be instantaneously changed, and the faster the rate of change of voltage the higher the current required to charge the capacitor. The surge current-limiting resistor provides the exponential charge characteristic you learned about in a previous course which slows down the response but protects the equipment.

For small FETs like the ones we use, this surge current is pretty minimal, and the resistance in the wires or PCB traces can be enough to limit the surge current. However, for bit power FETs, the capacitance can be pretty big, even to the point of necessitating BJT drive transistors to turn them on fast enough for applications like power inverters.

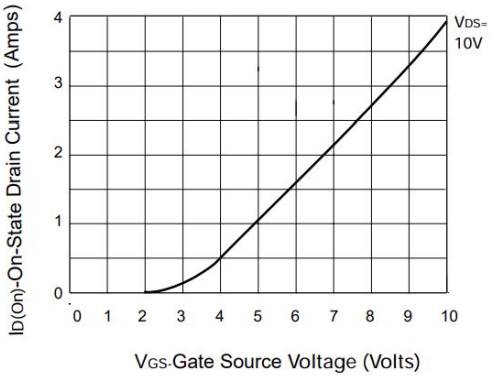
If you install both a surge current resistor and a pull-up or pull-down resistor, put the surge current resistor on the Gate side of the pull-up or pull-down resistor.

N-Channel E-MOSFET Logic Switch

Here's a worked example using an N-Channel E-MOSFET that's pretty close to the ones in your component kit. In this case, it's operating as a simple inverter.



The input for this circuit is 3.3 V TTL logic, switching between 0.0 V and 3.3 V. The first question we need to ask is whether this transistor will switch appropriately. Here's a tranfer curve from the data sheet:



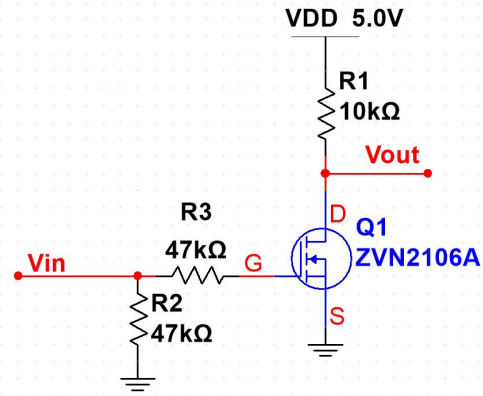
Transfer Characteristics

The first thing to notice is that I_D is in amps! This little transistor can handle a lot of current!

More to the point, if V_{GS} is 3.3 V, the transistor can pass about 400 mA, so there's no problem with us using it in our circuit. Proof?

I_{Dmax} = 5 V / 10 kΩ =500 μA, which is about a thousandth of the current that could be provided by the transistor.

We should always label the pins so we don't get confused. Here's the labelled diagram:



When V_{in} is 0.0 V (LOW), V_G = 0 V and V_S = 0 V (grounded), so V_{GS} = 0 V and I_D will be 0 mA. With no voltage drop across R_D, the output will be at +5.0 V (HIGH). The transistor behaves as an open switch.

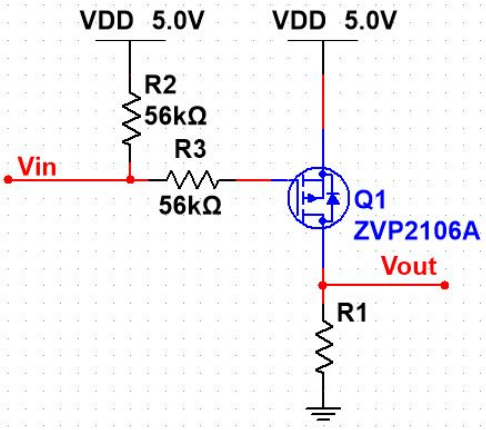
When V_{in} is 3.3 V (HIGH), V_{GS} = 3.3 V which is past the threshold shown on the graph and also past the highest (worst) value for V_{TH} given in the Data Sheet (https://www.diodes.com/assets/Datasheets/ZVN2106A.pdf) as 2.4 V, so the transistor will be turned on. From our previous discussion, it will be saturated, so its on resistance, given in the data sheet as 2 Ω, will result in V_{DS} = 500 μA * 2 Ω = 1 mV, or practically zero (LOW). The transistor behaves as a short or a closed switch.

If V_{in} is accidentally left disconnected, R2 will dissipate to ground any charge that might collect on the Gate, pulling the Gate to 0.0 V and turning the transistor off (output will be HIGH).

When V_{in} switches from LOW to HIGH, the Gate capacitance will charge through R3, and when V_{in} switches from HIGH to LOW, the Gate capacitance will discharge through R3.

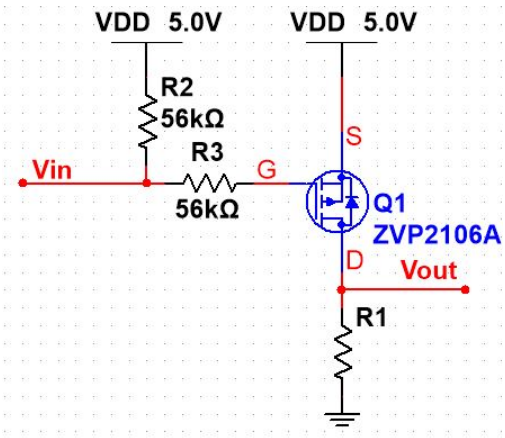
P-Channel E-MOSFET Logic Switch

Now, let's do a P-Channel E-MOSFET switch.



Notice that the symbol for this transistor contains a protection diode, reverse-biased across the device. The same protection would be found in the ZVN device in the previous question, but the library designers left it out.

Before we get too far, we'd better label the pins. Note that the Source is "up" and the Drain is "down", as would be expected for a P-Channel device.



We'll design this switch to be low-power: only about 250 μA in the ON condition. Since the voltage drop across the transistor V_{DS} will be very small (the Data Sheet (https://www.diodes.com/assets/Datasheets/ZVP2106A.pdf) indicates an ON resistance of 5 Ω, so V_{DS} = -1.25 mV (negative because D is below S)), we can treat the transistor as a short or closed switch. In other words, essentially the full 5 V will appear across R1, so R1 = 5 V / 250 μA = 20 kΩ. Since we only have 10% standard values, we'll pick 22 kΩ (larger to force saturation).

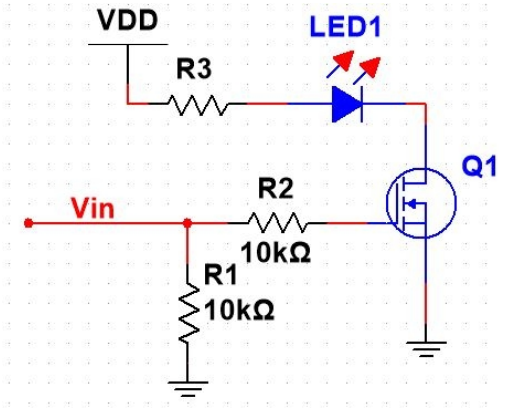
We'll check to see if the transistor will really saturate. The data sheet says that the worst value for V_{TH} is -3.5 V. So, if Vin is zero, V_{GS} = V_G - V_S = 0 - 5.0 V = -5.0 V. That's considerably bigger than V_{TH}, so the transistor should be ON. From the graph of the transfer function, at -5.0 V I_D could be as big as approximately -400 mA, so the transistor will definitely be able to supply the 250 μA we are designing for. Actually, the theoretical current for the resistor we chose will be 5 V / 22 kΩ = 227 μA.

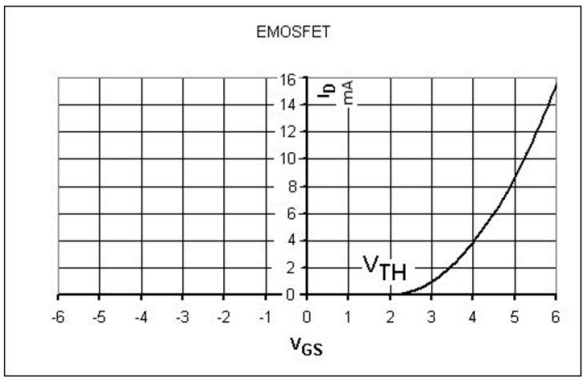
As with the PNP BJT switch, the problem with this circuit will be turning it off, as we will have to raise the Gate voltage high enough to ensure we're above the threshold. The data sheet indicates that it's possible for a transistor to be as good as having V_{TH} = -1.5 V, so to turn the transistor off, we need an input voltage of greater than 5 V - 1.5 V = 3.5 V (from V_G = V_S +V_{GS}). So, this circuit would not work reliably with a 3.3 V logic input. It would be fine, however, with 5 V TTL logic.

If the input was accidentally left disconnected, R2 would pull the Gate HIGH, resulting in V_G = 5.0 V. In this case, V_{GS} = V_G - V_S = 5 V - 5 V = 0 V, so the transistor will be off. With no current through R_D, the output would be at 0.0 V, or LOW.

E-MOSFET Current Switch

As with the BJT, we can use the FET as a switch to turn a current on or off to control LEDs, lights, relays, heater elements, motors, etc. Here's a simple LED driver using a transistor with significantly less current handling capacity than the ones in your kits, with both of the Gate resistors installed.



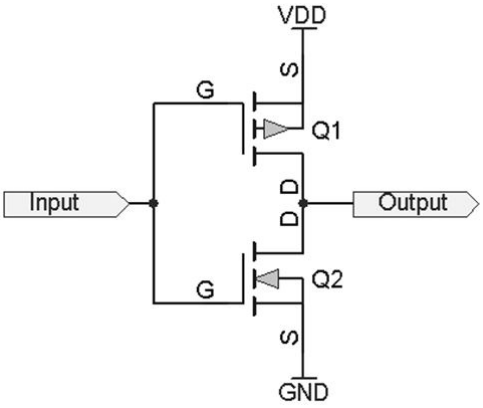


8. If the LED has a barrier potential of 1.7 V and requires at least 6 mA to glow visibly, will this circuit work with an input that switches between 0 and +5 V? _____
9. The available power supply is +9 VDC. Calculate the ideal resistance for R3. _____ kΩ, then pick the next lowest 10% resistance value _____ kΩ.
10. When should the LED glow? _____
11. If, by mistake, the series gate resistor had been placed ahead of the pull-down resistor, what voltage would appear at the Gate when the input is HIGH? _____ V Would this provide sufficient current to turn the LED on fully? _____

CMOS Switch

We've finally made it to the switching circuit that has revolutionized digital electronics, and has made the E-MOSFET the most common resistor by far -- probably over 99% of earth's transistors are found in CMOS switches, because that's what is used in all of our computers, portable phones, and so on.

Here's the basic CMOS switch, which is the E-MOSFET version of the Totem Pole configuration:



Two transistors, no resistors -- pretty simple! Note that the upper transistor is P-Channel and the lower transistor is N-Channel. These form a complementary pair of E-MOSFETs, hence the name: Complementary Metal Oxide Semiconductor.

There is no need for biasing resistors in this design, because, in either of its static states, one transistor is turned off, so no current flows, and no power is dissipated.

12. When the input is LOW, Q1 is _____ and Q2 is _____ In this state, the output is directly connected to _____ and the output is _____ . The current from VDD to GND is _____
13. When the input is HIGH, Q1 is _____ and Q2 is _____ In this state, the output is directly connected to _____ and the output is _____ . The current from VDD to GND is _____
14. Based upon what you have discovered, this device is a logical _____
15. How much power is dissipated when the input is LOW? _____ mW
16. How much power is dissipated when the input is HIGH? _____ mW

From what you've just done, you've shown that the CMOS switch can provide both logic HIGH and logic LOW without any current, and therefore with no power dissipated as heat, as P=IV. This is the reason CMOS can be used in extremely computationally powerful devices like computers and phones. However, these devices still produce some heat, and your computer probably has a fan and maybe even liquid cooling, if you're a serious gamer. Where does that heat dissipation come from?

When a CMOS switch makes the transition between one logic level and the other, there is a split-second of time when both transistors are turned on. During this time, since there are no current-limiting resistors in the circuit, the transistors are effectively trying to short the power supply to ground, and a great deal of current can flow. The accumulated effect of millions of these transitions per second can lead to a significant amount of heat being produced.

The solutions to the heating problem are typically

- Speed up the transition time so the current burst is as short as possible
- Lower the voltage of the power supply, because P=IV, so a lower voltage means less power
- Reduce the overlap between the threshold voltages of the two transistors so that the percentage of time they are both on is reduced

Of course, in our relentless pursuit of technological advancement, as soon as we reduce the power dissipation, we speed up our devices! So, power dissipation will always be an issue.

CMOS Issues

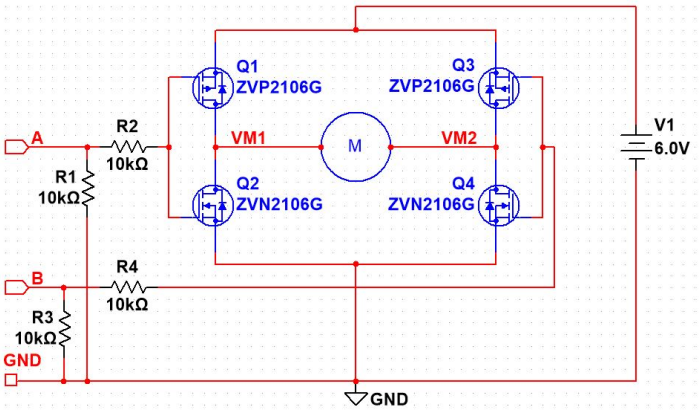
1. We've seen that the overlap of threshold voltages in CMOS switches results in heat dissipation.
2. Another problem caused by this overlap is that CMOS inputs must always be held at a defined logic level. If a CMOS input is allowed to float, it will -- any static electrical charge available will collect on the Gates, and will very likely result in an input voltage between LOW and HIGH, where both transistors will be turned on. With no current-limiting resistors, something is going to experience Thermal Destruction, and the device will be destroyed. The solution is to ensure that all CMOS ***inputs*** (don't mess with the outputs) must be pulled or tied HIGH or LOW. Many modern devices have weak internal pull-up or pull-down resistors to protect them, but these resistors add to the overall power dissipation of the device.

3. A third problem caused by the threshold voltage overlap is that each logic transition puts a voltage spike onto the power supplies, as the voltage is pulled down towards ground and then recovers. This can interfere with the operation of other ICs in the device, and can generate electromagnetic radiation (EMR) that could interfere with other sensitive devices such as radio-based equipment or heart pacemakers. The solution to this problem is the careful use of ***decoupling capacitors***. Each CMOS device power pin should have a capacitor to ground as close to the device as possible. Since the voltage across a capacitor cannot be changed instantaneously, the CMOS switching spike will not be able to pull the power supply to ground. In other words, the decoupling capacitor will provide the instantaneous charge demands of the CMOS switch as it changes logic levels.
4. Electrostatic Discharge damage -- the thin oxide layer at the Gate is quite easily damaged. A "spark" of 30 V or more is likely to cause irreparable damage. Dropping a piece of paper onto a CMOS chip is likely to generate more than 30 V, and a visible or tangible "shock" is likely to be in the hundreds or thousands of volts -- definitely enough to kill a CMOS device. Many devices have ESD protection built into them, but CMOS devices should only be handled when the handler is wearing an electrostatic dissipative (static) strap that is properly grounded or held at the potential of the device being worked upon.
5. A completely unrelated problem that arises with CMOS devices is called ***latch-up***. This is a problem that arises from having hundreds of CMOS switches made on the same layers of semiconductor material. in places other than where the desired circuitry has been built, there will be material that forms unexpected semiconductor devices that are outside of the control of the circuit. These vestigial devices can sometimes go into reverse breakdown, attempting to short power to ground, and there is no way to turn them off other than to shut off the power to the IC. Latch-up only happens if a CMOS input is pulled to a voltage either above the power supply voltage or below ground. Some devices have clamping circuits built into their inputs, but it is wise never to allow out-of-range input voltages to reach a CMOS device.

As long as these limitations and issues are properly addressed in the design of a piece of equipment, CMOS can provide long and trouble-free service with very low power consumption.

CMOS H-Bridge

It should probably have crossed your mind that the CMOS switch is essentially a FET Totem-Pole or Half-Bridge, so it's just a small step to creating a CMOS H-Bridge. The following is a worked example to help you firm up your understanding of the CMOS switch and also show you the operation of a CMOS DC motor controller.



First, a quick investigation. The inputs are coming from off-board, likely from a microcontroller. As always, there needs to be a common ground between off-board equipment and our circuit. Also, note that the two inputs have pull-down resistors, so the default condition is 00. From what we know of H-Bridges, this should be one of the two OFF conditions for the motor. Also, there are capacitive charge-limiting capacitors shared by the Gates of the MOSFETs. Unlike the BJT version, we don't need separate resistors for each transistor, since there's no operating current at the Gate of a FET. Only the voltage matters.

A quick check shows that the Sources of the P-Channel devices are connected to the positive power rail and the Sources of the N-Channel devices are connected to ground, which is as it should be.

All of the MOSFETs have internal protection diodes, so we don't need to install our own. Also notice that, with the transistors installed correctly, all the internal diodes are reverse biased, as they should be.

Another important thing to notice is that the motor-side of this circuit is powered by its own 6 VDC circuit. We can probably assume that the logic levels are 0.0 V and 5.0 V, so we'll have to make sure the input voltage goes high enough to shut off the P-Channel devices. Let's do that. The Data Sheet (https://www.diodes.com/assets/Datasheets/ZVP2106A.pdf) for the ZVP2106G indicates that the smallest value for V_{TH} is -1.5 V. So, with a 6 VDC power rail, we need to have the input logic rise above 6 V - 1.5 V =4.5 V, so as long as our input signal HIGH is 5.0 V, this circuit will work. *(If it hadn't, we'd have needed to provide Level Translators to bring the HIGH voltage up to 6 V.)*

Now for a quick analysis:

- When an input is LOW

- V_{GS} for the P-Channel device will be V_G - V_S = 0 V - 6 V = -6 V, which is much greater than the worst V_{TH} of -3.5 V, so the transistor will be ON, connecting the Drain and therefore the motor connection to +6 V.
- V_{GS} for the N-Channel device will be 0 V - 0 V = 0 V, so the transistor will be OFF, disconnecting the Drain and therefore the motor connection from ground.

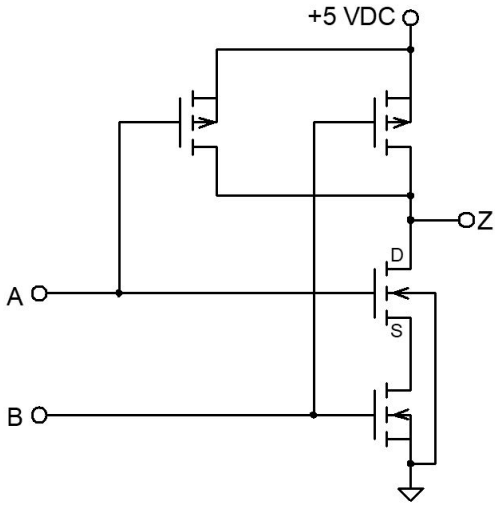
- When an input is HIGH (+5 V)
  - V_{GS} for the P-Channel device will be V_G - V_S = 5 V - 6 V = -1 V, which is less than the smallest expected V_{TH}, so the transistor will be OFF, disconnecting the motor connection from the positive rail.
  - V_{GS} for the N-Channel device will be V_G - V_S = 5 V - 0 V = +5 V, which is higher than the largest expected V_{TH} of 2.4 V, so the transistor will be ON, connecting the motor connection to ground.
- So, when both inputs are LOW (00), both motor connections will be at 6 V, no current will flow, and the motor will be OFF.
- When A is LOW and B is HIGH (01), Vout1 will be 6.0 V and Vout2 will be 0.0 V, so current will flow through the motor from left to right (assume "forward").
- When A is HIGH and B is LOW (10), Vout1 will be 0.0 V and Vout2 will be 6.0 V, so current will flow through the motor from right to left (assume "reverse").
- When both inputs are HIGH (11), both motor connections will be at 0.0 V, so current will flow, and the motor will be OFF.

The (11) input logic condition is the safest way to turn the motor off, because all the lines will be de-energized and accidental shorting won't damage anything.

CMOS Logic Gates

Various combinations of complementary E-MOSFET transistors are possible, giving rise to all of the logic gates you encounter in courses like your Digital Logic course. Here are two examples for you to analyze. For each transistor, determine V_{GS} to help you tell if the transistor is ON or OFF (V_{GS} = 0 means OFF for an E-MOSFET). From that, determine whether the output, Z, is connected to +5 VDC or Ground. Fill in the table and use it to determine which logic gate this is.

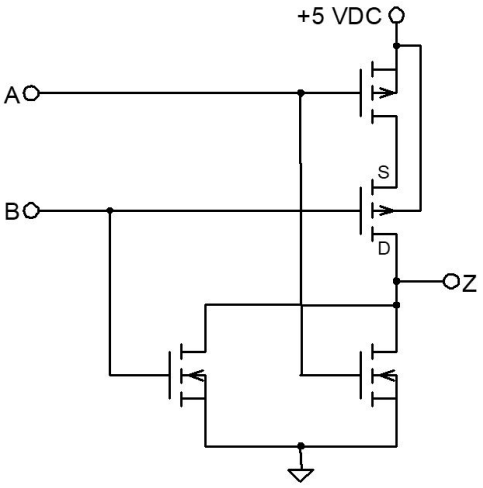
17. Circuit #1



A	B	Z
0 V	0 V	_____ V
0 V	+5 V	_____ V
+5 V	0 V	_____ V
+5 V	+5 V	_____ V

This logic gate is _____

18. Circuit #2



A	B	Z
0 V	0 V	_____ V
0 V	+5 V	_____ V
+5 V	0 V	_____ V
+5 V	+5 V	_____ V

This logic gate is _____

Online Homework System

Assignment Worksheet
5/31/21 - 9:55:56 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA09 FET Transistor Theory Quiz

Question 1: (1 point)

A field-effect transistor that must have the Gate voltage at or below the Source voltage is

(a) P-channel JFET

(b) P-channel D-MOSFET

(c) N-channel JFET

(d) N-channel E-MOSFET

(e) N-channel D-MOSFET

(f) P-channel E-MOSFET

Question 2: (1 point)

Which field effect transistor conducts maximum current when the Gate and Source voltages are the same?

(a) E-MOSFET

(b) JFET

(c) D-MOSFET

Question 3: (1 point)

Which field effect transistor conducts when the Gate and Source voltages are the same, and conducts a greater current when the Gate voltage is below the Source voltage?

(a) P-channel D-MOSFET

(b) N-channel D-MOSFET

(c) N-channel JFET

(d) P-channel E-MOSFET

(e) P-channel JFET

(f) N-channel E-MOSFET

Question 4: (1 point)

Which field effect transistor is normally off, but will conduct (i.e. have a Drain current) when the Gate voltage is considerably below the Source voltage?

(a) P-channel D-MOSFET

(b) N-channel E-MOSFET

(c) N-channel D-MOSFET

(d) N-channel JFET

(e) P-channel E-MOSFET

(f) P-channel JFET

Question 5: (1 point)

The output of a CMOS device is made up of

(a) An N-channel D_MOSFET and a P_channel D-MOSFET

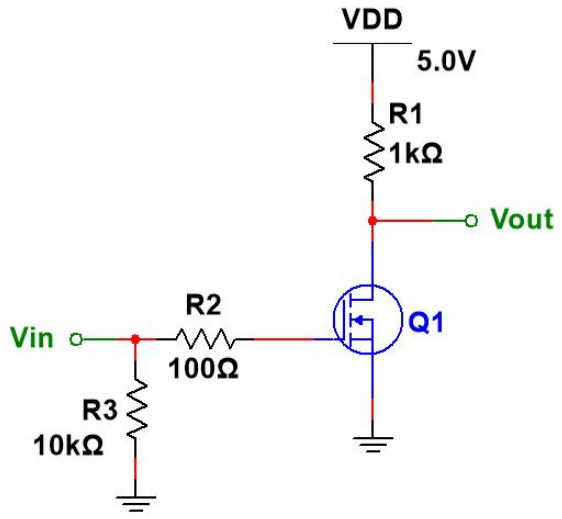
(b) An N-channel E-MOSFET and a P-channel E-MOSFET

(c) Two N-channel E-MOSFETs

(d) Two P-channel D-MOSFETs

Question 6: (8 points)

Use the schematic below to answer the following questions.



When V_{in} is 0 V, the voltage expected at V_{out} is _____ V.
When V_{in} is 0 V, the current expected through R_1 is _____ mA.
When V_{in} is 5 V, the voltage expected at V_{out} is _____ V.
When V_{in} is 5 V, the current expected through R_1 is_____ mA.
When V_{in} is 5 V, the current expected through R_2 is _____ mA.
When V_{in} is 5 V, the current expected through R_3 is _____ μA.

Which answer best describes the purpose of R_2?

(a) R_2 limits the Gate current in order to control the Drain current.

(b) R_2 provides a known input condition in the event that no input source is connected.

(c) R_2 limits the capacitive charge current at the Gate during a logic level transition.

(d) R_2 acts as a current-to-voltage converter to produce a logic level at the output.

Which answer best describes the purpose of R_3?

(a) R_3 provides a known input condition in the event that no input source is connected.

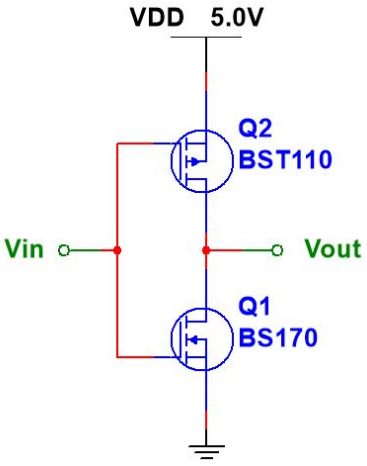
(b) R_3 limits the Gate current in order to control the Drain current.

(c) R_3 limits the capacitive charge current at the Gate during a logic level transition.

(d) R_3 acts as a current-to-voltage converter to produce a logic level at the output.

Question 7: (2 points)

Use the following schematic to answer the questions below.



When V_{in} is 0 v, the voltage expected at V_{out} is _____ V.

When V_{in} is 5 V, the current expected through Q_1 is _____ mA.

Online Homework System

Assignment Worksheet
10/18/22 - 1:52:27 PM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Lab05 FET Switching

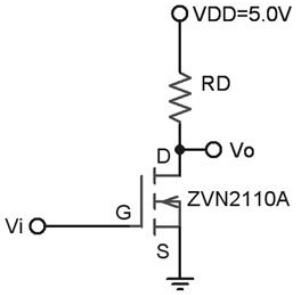
Question 1: (10 points)

Lab 05 Pre-Lab

Note: Do not move on to the "Next" page until you have completed your Pre-Lab. The next page is the Lab Activity, and once you move to that page, you will not be able to return to the Pre-Lab page!

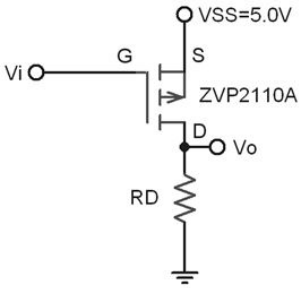
Single-Transistor E-MOSFET Switches

Use the schematic below to answer the questions that follow.



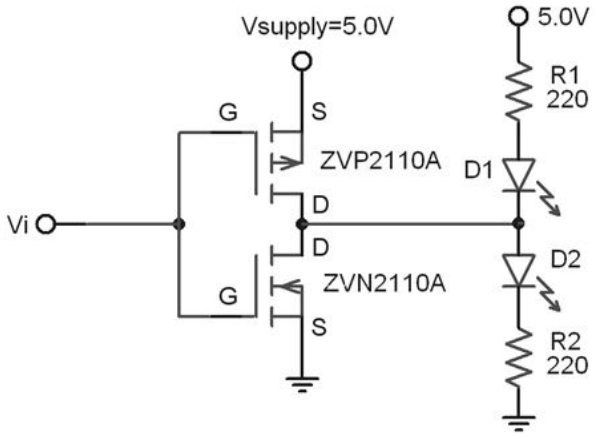
1. If I_D is to be about 760 μA, calculate the ideal value for R_D, assuming V_{DSon} is practically zero. _____ kΩ
2. Pick a standard 10% resistor value that is slightly less than double the ideal value, to ensure saturation. _____ kΩ
3. From the ZVN2110A Specification Sheet (https://www.diodes.com/assets/Datasheets/ZVN2110A.pdf), determine the range of possible threshold values for V_{GS}, for I_D = 1 mA: from _____ V to _____ V
4. If V_i = 0 V, V_{GS} = _____ V, and the transistor will be _____
5. If V_i = 4 V, V_{GS} = _____ V, and the transistor will be _____

Use the schematic below to answer the questions that follow.



6. From the ZVP2110A Specification Sheet (https://www.diodes.com/assets/Datasheets/ZVP2110A.pdf), determine the range of possible threshold values for V_{GS}, for I_D = -1 mA; from _____ V to _____ V
7. If V_i = 0 V, V_{GS} = _____ V and the transistor will be _____
8. If V_i = 4 V, V_{GS} = _____ V and the transistor will be _____

Use the schematic below to answer the questions that follow.



Note: It is recommended that you draw simplified models of this circuit for the two different input conditions, and trace the possible current paths from power to ground as you attempt to answer the following questions.

9. If V_i = 0 V, the Drains of the two transistors will be at _____ V; D1 will be _____ and D2 will be _____
10. If V_i = 4 V, the Drains of the two transistors will be at _____ V; D1 will be _____ and D2 will be _____

You have now completed the Pre-Lab. You may Save and Close or move on to the Lab Activity page, but do not "Submit" until you have completed the Lab Activity!

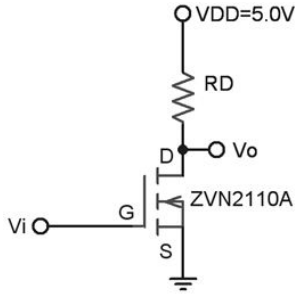
Question 2: (10 points)

Lab 05 Activity

Throughout this activity, the orientation of the transistors is critically important. Make sure you know what the Drain, Source, and Gate look like, and position them correctly!

N-Channel E-MOSFET Single Transistor Switch

On your breadboard, build the following circuit and test it as follows. R_D should be 12 kΩ.



- Use a +5 VDC power supply for V_{DD}.
- For V_i, use a signal generator set to produce a unipolar Pulse with an amplitude switching between 0 V and 4 V at 1 kHz, with a duty cycle of 25%.
- Display V_i and V_o appropriately on the two oscilloscope channels.
- Verify that the input signal really is switching between 0 V and +4 V, and that the output is switching essentially between +5 V and 0 V.

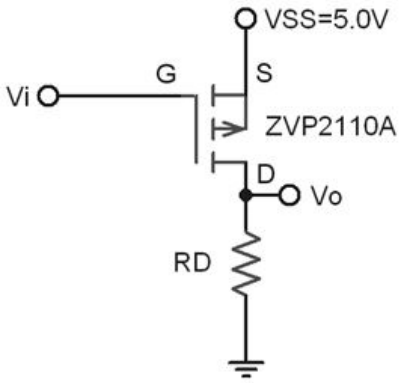
Once you are convinced your circuit is working properly, supply the following results:

1. When V_i = 0 V, V_o = _____ V

2. When V_i = 4 V, V_o = _____ V
3. Ask your instructor to give you a grade out of three marks for your circuit and the proper setup of your oscilloscope. _____

P-Channel Single Transistor Switch

Using your breadboard, build the following circuit and test it as follows. Make sure you know which pins are Source and Drain! R_D should be 12 kΩ.



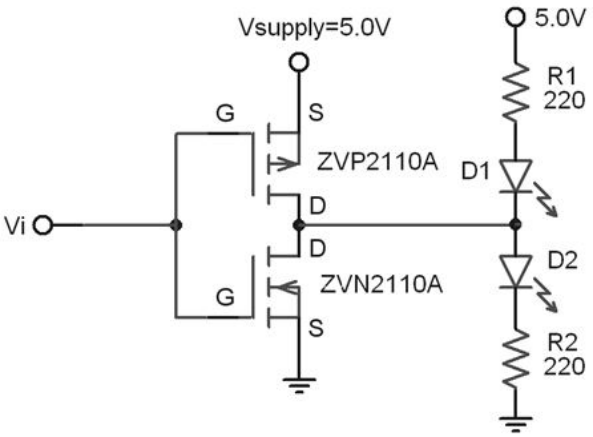
Use the same settings as in the previous section for the two waveform channels and the two oscilloscope channels. Follow the same check-list as before to ensure the equipment and circuit are working properly.

Once you are convinced your circuit is working properly, supply the following results:

4. When V_i = 0 V, V_o = _____ V
5. When V_i = 4 V, V_o = _____ V
6. Ask your instructor to check your work and oscilloscope settings for a grade out of three marks. _____

CMOS LED Driver Circuit

Using your breadboard, build the circuit below to answer the questions that follow. Use a RED LED for D1 and a GREEN LED for D2.



Since we want to see the action on the LEDs, change the frequency of the unipolar pulse to 0.5 Hz. All the rest of the settings can remain the same for you to use as V_i.

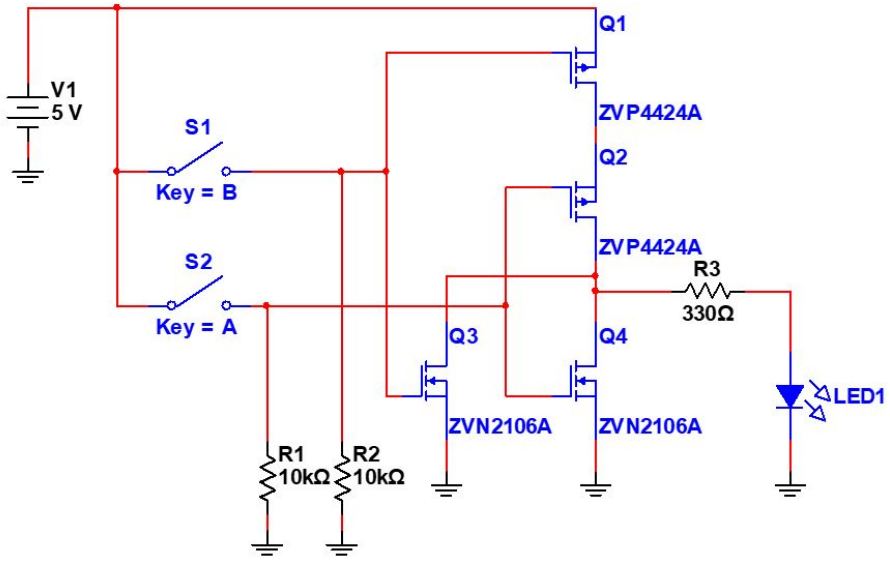
Use the oscilloscope channels to observe V_i and the voltage at the node with the two transistor Drains. You will need to change the horizontal time base of your oscilloscope to a much larger time/Div setting to see such a slow signal.

Once you are convinced that your circuit is working properly, record the following:

7. When V_i = 0 V, _____
8. When V_i = 4 V, _____
9. Ask your instructor to check your work and oscilloscope settings for a grade out of three marks. _____

Two-Input Logic Gate -- Simulation

Using Multisim, build the circuit below and answer the questions that follow.



Place voltage probes on the output sides of the two switches and at the node between Q2 and Q4. Assuming that 0 V represents Logic 0 and +5 V represents Logic 1, work your way through the following Truth Table, and determine which gate type it represents.

B	A	Output (0 or 1)
0	0	_____
0	1	_____
1	0	_____
1	1	_____

This circuit is a _____

You have now completed this Lab. Once you submit your results, you will not be able to return to this page!

Online Homework System

Assignment Worksheet
10/21/22 - 7:50:29 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA10 FET Relay Driver Activity

Question 1: (10 points)

FET Relay Driver

For this exercise, we will focus on the use of an E-MOSFET in controlling an inductive load such as a relay coil.

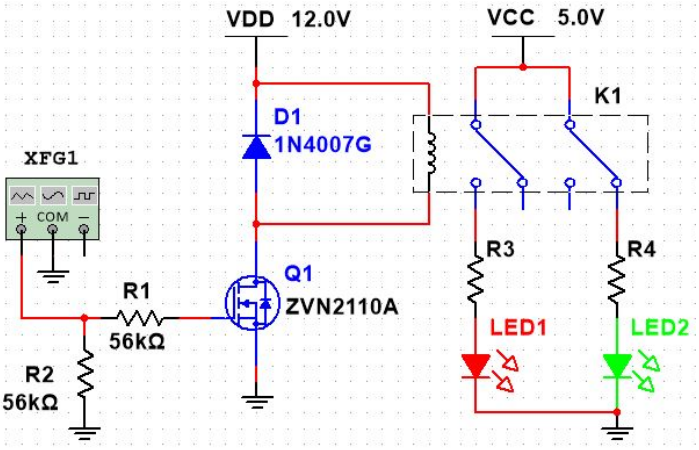
In your parts kit, you have two relatively small FETs: ZVN2110A and ZVP2110A. The first is an N-Channel device, the second is a P-Channel device. Make sure you know the difference!

The Manufacturer's Specification Sheet (https://www.diodes.com/assets/Datasheets/ZVN2110A.pdf) will provide you with the necessary information to answer the following questions.

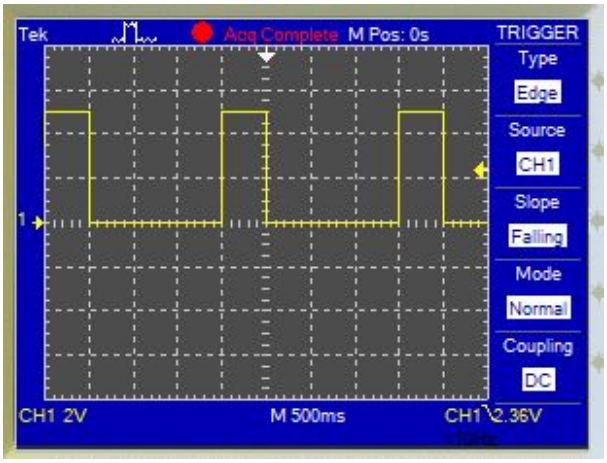
1. Our relay draws close to 50 mA when powered from +12 V. How much continuous current can the ZVN2110A handle? _____ mA
2. What is the maximum V_{DS}? _____ V
3. Based upon these specifications, the ZVN2110A is capable of operating our relay (True/False).

(a) True
(b) False

On your breadboard, build the circuit as shown in the schematic below. Instructions follow.



4. K1 is the relay from your CNT Year 1 Kit -- G2R-2-DC12; for this, you need to determine the pinout, and connect the coil, a normally-open contact of one switch to the RED LED circuit, and the normally-closed contact of the other switch to the GREEN LED circuit
5. Determine suitable values for R3 and R4 to limit the LED currents to 12 mA each
6. Use a +12 VDC power supply to generate VDD, and a +5 VDC supply for VCC.
7. Use a signal generator to produce a pulse that switches from 0 V to +5 V at a frequency of 500 mHz (i.e. a period of 2 s) with a duty cycle of 25%, as shown below. Use your oscilloscope to verify that the incoming signal is correct.



8. Since we're going to try and see the voltage spike generated by the relay coil when it doesn't have a protection diode, we need to use the x10 probe feature. Make sure both the scope probe and the scope settings are set to x10!
   What you have actually done is inserted a 9 MΩ resistor in series between the scope probe tip and the front end of the oscilloscope. This input has an impedance of 1 MΩ, so you've created a voltage divider where Vin = Vprobe(1MΩ/(1MΩ+9MΩ), or 1/10th of the original signal. Now your oscilloscope can measure signals ten times bigger than it could with a x1 probe!

   Once you have your input signal set up properly, ask your instructor for a grade out of four marks. _____

Make sure your circuit is responding to this input signal as you would expect it to.

9. When the input is HIGH, _____

Now, set your oscilloscope to respond to a FALLING edge of the input signal, in NORMAL mode so we can catch individual events. Set the trigger level to around 2.5 V. Use Channel 2 to observe the signal at the Drain of the transistor. Set the amplitude of Channel 2 to maximize the Drain Voltage signal, and set the Horizontal time base to 500 μs/div.

Temporarily remove the diode, and adjust your oscilloscope channels to display the whole inductive spike generated by the relay coil.

10. Ask your instructor to give you a grade out of two marks for the oscilloscope display. _____

Return the diode to its proper place in the circuit, and change the time-base so that you can see two or three cycles of the signal.

Use the Measurement Menu and the graticule lines on the oscilloscope to help you measure and record the following:

11. In the OFF condition, V_D settles to _____ V
12. However, right after the transistor turns OFF, the voltage rises to _____ for a short time. The component responsible for maintaining a small difference between the last two answers is _____
13. As before, temporarily disconnect D1 from your circuit. The maximum voltage is now in the range of _____ The component responsible for generating this voltage is _____
14. Reconnect D1. Now, temporarily disconnect the function generator (i.e. remove the connecting wire). The RED LED stays _____ The component responsible for this condition is _____
15. Disconnect R2 from ground and connect it instead between the input and the +5VDC source. The RED LED stays _____
16. Reconnect the signal generator, and verify that, with R2 connected to VCC, the circuit operates as it did before. In this arrangement, R2 acts as _____
17. R1 acts as _____

You have now completed this exercise. Save and Close it so your instructor can grade it.

Online Homework System

Assignment Worksheet
3/6/23 - 10:21:20 AM MST

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA11 FET Heater Circuit Activity

Question 1: (10 points)

Your instructor's check-off for this exercise is based largely on a schematic diagram you will draw as you proceed through this assignment. Make sure you include part types or values and wire the pins correctly.

In your kit, you have an IRF540 power MOSFET, capable of handling over 20 A of current. Given that the outlets in your house are set to trip the breaker if more than 15 A is drawn from them, this MOSFET can control a lot of power! We could use this to turn on a serious heater coil. Unfortunately, the resistors in your kit are only designed to handle 0.5 W, so we will have to make do with one of them as a simulated heater coil. However, we'll drive it hard to produce some heat.

1. Determine the size of resistor that would produce 750 mW of power from a 12 VDC supply (that's higher than the resistor's rating, but it will be able to handle it). Pick the next largest value available in your kit (10% list). _____ Ω
2. How much current will this resistor draw from the 12 V supply? _____ mA

Start drawing your schematic for your instructor, using Multisim. Show a +12 VDC power supply, the IRF540, your resistor inserted as R_D, and a DC_INTERACTIVE_VOLTAGE with its maximum value set to +5 V.

3. Recall that FETs should have either a pull-up resistor or a pull-down resistor to establish a known condition in the event that the input signal is not connected. To prevent accidental current from flowing through the load resistor, you should use a

   (a) Pull-up resistor

   (b) Pull-down resistor

Use 100 kΩ for this resistor, in the configuration you've chosen, and add it to your schematic.

Also, add a surge current limiting resistor of 47 kΩ at the Gate of the FET.

You will also want to know when the circuit is actually heating. An unsatisfactory solution to this would be to put an indicator on the input side of your circuit -- this would only tell you if the *control signal* was active, so you would only know when heating is being called for, not whether the FET has actually turned on the current to the load. A better solution would be to put an indicator on the load side. You've got two choices: either you could put an indicator in series with the load, or you could put it in parallel. If it's in series, it would need to handle the entire current; if it's in parallel, you will really only know if the FET is turning on.

4. Given that we want to use an LED, and a real heater could draw up to 30 A (even your half-watt resistor is drawing more current than the 10 mA required for the LED), determine which of these options is most practical.

   (a) Series indicator

   (b) Parallel indicator

5. Your LED indicator needs a current limiter between it and +12 V. Determine a suitable resistance value to limit the LED current to 10 mA, assuming an LED forward voltage of 1.8 V, and pick a suitable value from the parts in your kit (10%). _____ kΩ

Add the indicator circuit to your schematic. At this point, you may want to check your circuit with your instructor.

Build the circuit on your breadboard using the +/- 12 V PowerBRICK as the source, and set up your Waveform generator to produce a +5 VDC signal for the input. (You can turn this on and off when you want to, using Waveforms.)

Verify that it works properly -- you should be able to detect some warmth from the load resistor when the input is set to +5 VDC.

Take a screen-shot of your schematic, and upload it here for your instructor to grade out of five marks. Don't use any spaces or special characters in your filename, but personalize it for easy identification as belonging to you. Document Upload (Direct)

Online Homework System

Assignment Worksheet
10/18/22 - 1:39:42 PM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Project 3: Transistor Circuits

Question 1: (50 points)

Project 3 Preparation and Simulation

This Project must be submitted for grading at the time specified by your instructor. You will be given some class time to work on it, and will be expected to do other work on your own time.

As this is a more formal assessment than the lab activities, your instructor's involvement will be limited to clarification of the requirements and simple feedback on your work. This assessment is intended to show that you have a good grasp on the associated course outcomes, so please limit your interactions with others to points of clarification or improvement of your understanding of the material rather than working together to arrive at solutions.

The first part of this assessment will involve preparatory work and predictions regarding a circuit similar to what you will build later, culminating in a simulation to demonstrate its operation. The second part will involve building and testing a real circuit, and will be graded primarily upon your technical skills of cuircuit building and use of test equipment.

Grading breakdown:

30% -- Preparatory Work and Predictions

20% -- Simulation

50% -- Circuit Building and Testing

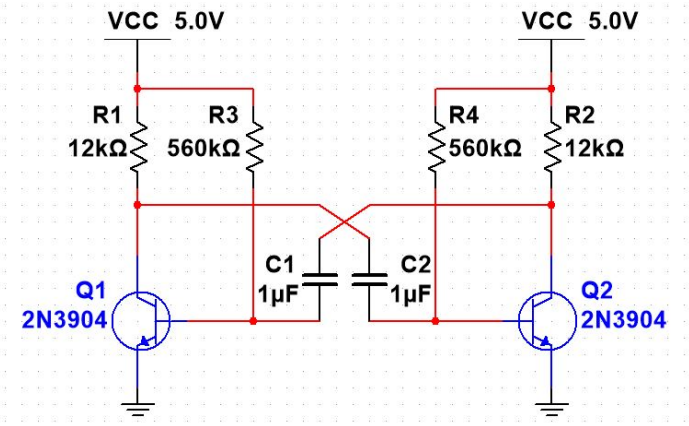
Note: Once you submit this first page and move on to the next, you will not be able to return to it! Instead of moving on to the next question, you can "Save and Close" if you intend to return later.

The "Printable Version" is also available for you to work through before submitting your answers.

You are allowed one "How Did I Do?" to check your answers to this part of the project.

Oscillator with Cross-Coupled Bases

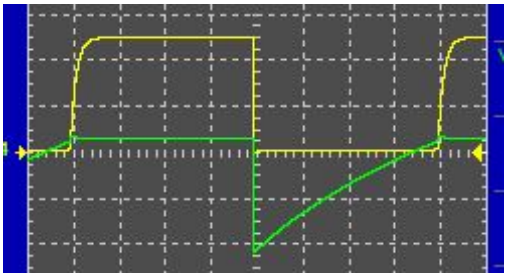
The circuit shown below is designed to run continuously as a square-wave oscillator. Its mode of operation will be explained below, with some input from you.



Notes:

- Assume the VBEon voltage for the transistors is 0.7 V
- Assume that β = 100, in other words the minimum value for a 2N3904 transistor
- Assume an ideal VCEsat of 0.0 V

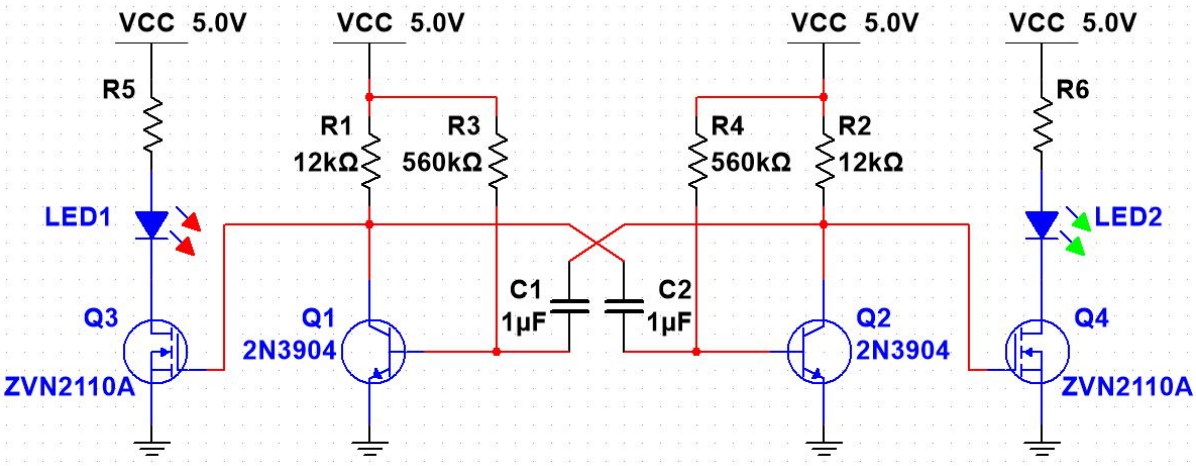
The oscillator takes a couple of cycles to reach its steady state. We'll jump in at a point after steady state oscillation has been achieved. At this point, the voltages at the two ends of one of the capacitors appear as follows on an oscilloscope:



1. C2, after being quickly charged to a net potential difference of 4.3 V through R1 (yellow trace), suddenly has its positive end grounded as Q1 turns on. This means that the negative end of C2 is plunged to -4.3 V (green trace). The capacitor is then more slowly discharged through the 560 kΩ resistor, and partially charged in the opposite direction until its voltage is high enough to activate Q2. According to our transistor model, the required voltage to activate the Base of Q2 is _____ V. To simplify the calculation of the time required, assume that the charging current is a constant 12.5 μA and the full discharge and partial charge of the capacitor results in an overall potential difference of 5.0 V. Using $V_C = \frac{I \cdot t}{C}$, determine the time required to change the capacitor voltage by 5.0 V, and record this in milliseconds: _____ ms
2. In the meantime, C1 has been fully charged through the 12 kΩ resistor, and is sitting with 4.3 V across it. When Q2 is activated, the negative end of C1 is plunged to -4.3 V and starts to ramp up until it activates Q1, which starts the cycle again. Therefore, a complete cycle involves first the discharge and partial charging of C2 then the discharge and partial charging of C1. Assuming that the time for discharging and partially charging one capacitor is 450 ms, the overall period of one cycle would be _____ ms and the frequency of the oscillator would be _____ Hz.
3. Let's check to make sure the transistor circuits are actually designed to switch properly. When all the Base current is supplied through the 560 kΩ resistor, what is the predicted Base current, in microamps? _____ μA. What Collector current is predicted using the Active transistor model? _____ μA. What is the maximum possible Collector current, based upon the resistors in the circuit? _____ μA. The transistor must therefore be _____

Oscillator with LED Drivers

Consider the following circuit:



Notes:

- Assume a V_{TH} of 2.0 V for the FETs
- Assume an ON voltage for the FETs of practically zero
- Assume a forward diode drop of 1.8 V for the LEDs

4. The Field-Effect transistors were most likely chosen because, with a net Gate current of _____ μA, they will have minimal effect on the operation of the oscillator.
5. When Q1 is saturated, or turned ON, Q3 will be _____
6. When Q3 is ON, we want to limit the current to just under 10 mA so the LED will glow reasonably brightly. What standard 10% resistor should be chosen for R5 (and R6)? _____ Ω
7. In this circuit, R1 functions as both a Collector resistor for Q1 and as a _____ for Q3.

Simulation

Using Multisim, build the circuit above, using the resistor value you chose (which you can doublecheck here) for R5 and R6.

Notes:

- You don't have to do the angled lines for the cross-coupled Bases -- just make them electrically correct.
- Multisim doesn't have a ZVN2110A in its libraries, so use a ZVN2106A instead.
- Place a current probe to measure the current through the LED when it lights.
- Use a Tektronix four-channel oscilloscope to look at the Collectors and Bases of the two BJTs.

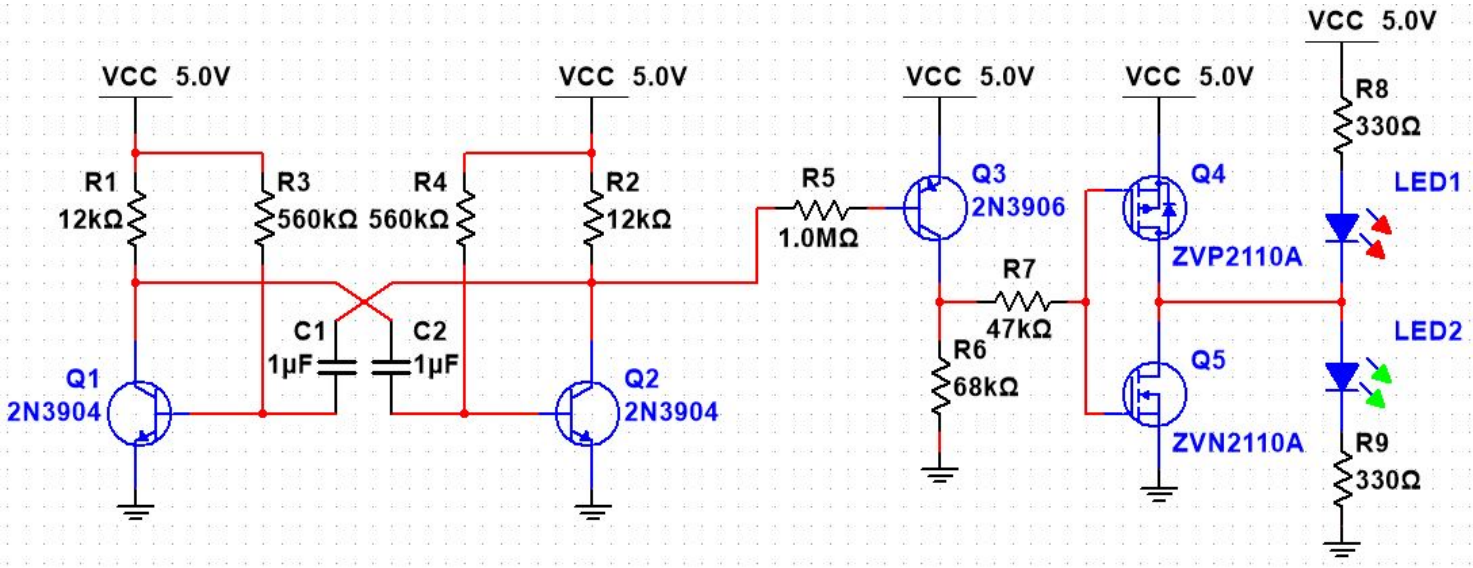
8. Take a screenshot of your schematic and upload it here for a grade out of three marks. Document Upload (Direct)
9. When an LED is ON, it draws _____ mA
10. Adjust the oscilloscope so that all traces are set up identically. Display two to five cycles on the screen, and take a screenshot for your instructor to grade for proper operation of the circuit and proper setup of the oscilloscope, out of four marks. Document Upload (Direct)

You have now completed the Preparation and Simulation components of this project. Save your work, then move on to the next question (Build and Test). Once you move on, you will not be able to access this part of the project again!

Question 2: (50 points)

Project 3 Build and Test

The following circuit uses the same Cross-Coupled Base Oscillator design, but uses a totem pole configuration to activate the LEDs.



Build this circuit. You may want to build it in stages to verify the operation of each part of the circuit.

1. Check the oscillator: Use your two oscilloscope probes to observe the signals at the Collectors of Q1 and Q2. You should see two square waves, 180^{o} out of phase to each other. What is the frequency of the circuit's oscillation? _____ Hz
2. The Q3 circuit squares up the oscillator's signal, removing the R-C charge curve at the beginning of each pulse. Set up your oscilloscope to compare the signal at the Collector of Q2 to the signal at the collector of Q3, and ask your instructor to grade your display out of four marks. _____

3. Note the size of Q3's Base resistor and the circuit configuration. In addition to squaring up the oscillator's signal Q3 performs which of the following functions? Select all that apply.

(a) LED driver

(b) Current amplifier

(c) Logic Inverter

(d) Level shifter

4. What function is performed by R7?

(a) Surge current limiter

(b) Pull up resistor

(c) Limit the transistor-controlling Gate current

(d) Pull down resistor

5. Use your oscilloscope to compare the signal at the Collector of Q3 to the signal at the Drains of Q4 and Q5. When the signal at Q3 is HIGH, the signal at the Drains is _____ .

6. When the signal at the Drains of Q4 and Q5 is HIGH:

(a) neither LED glows

(b) LED1 glows

(c) LED 2 glows

(d) Both LEDs glow

7. Ask your instructor to grade your circuit out of ten marks. You will be deducted marks for each time your instructor needed to help you with troubleshooting or circuit layout. _____

You have now completed this project. Once you submit your work, you will not be able to return to any of these questions!

Online Homework System

Assignment Worksheet
5/20/22 - 9:30:06 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Introduction to Amplification

Question 1: (1 point)

Basics of Amplification

Transistors, by nature, are current amplifiers -- in response to a small input (for the BJT a current signal at the Base, for the FET a voltage signal at the Gate), transistors control large current signals through the main path (Collector and Emitter for the BJT, Drain and Source for the FET). Notice the careful wording -- they don't "make a small input signal into a large current": they use a small input signal to control a large current, which requires a good DC power source to drive that large current.

The letter ***A*** is used as a variable to represent amplification, or ***Gain***. For the BJT transistor, the current gain was given the symbol β. However, for an amplifier circuit, it would be called the current gain. So, for a current amplifier,

$$A_i = \frac{I_{out}}{I_{in}}$$

Voltage gain compares output voltage to input voltage for a voltage amplifier:

$$A_v = \frac{V_{out}}{V_{in}}$$

Power gain compares output power to input power for a power amplifier:

$$A_p = \frac{P_{out}}{P_{in}}$$

In this course, we will concentrate on voltage gain.

Voltage Amplifier Model

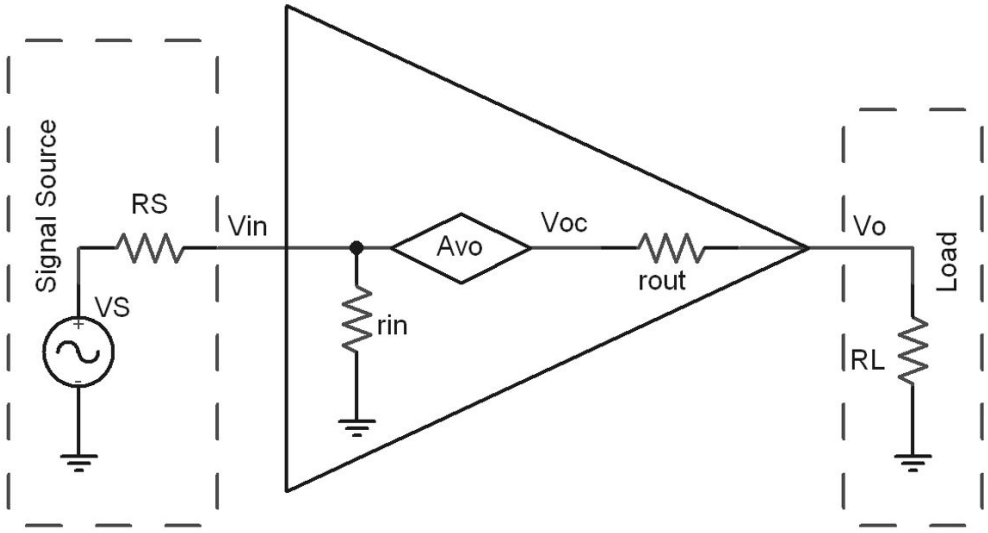
An ideal amplifier would simply take an input signal and multiply it by a gain factor to produce the output signal: $V_{out} = A_v V_{in}$. Unfortunately, not many transistor amplifiers are ideal. Operational amplifiers (op amps) can be very nearly ideal. However, they were designed in response to years of working with the non-ideal characteristics of simple transistor amplifiers.

An ideal amplifier, in order to be ideal, would have:

1. an infinite input impedance so that no current would be drawn from the source, thereby having no effect on the source itself
2. zero output impedance so that being connected to a resistive load would not result in any loss of signal

Unfortunately, most amplifiers have measurable input and output impedances, which need to be taken into account when analyzing the performance of the amplifier.

Here's a model of a non-ideal amplifier, as connected to a non-ideal signal source and a load:



The "A_{vo}" component in the middle would be the ideal amplification component of this model -- the V_{in} signal presented to the A_{vo} diamond is multiplied by the "open circuit gain" to produce the "open circuit output voltage", V_{oc}. More on that terminology in a moment.

$$A_{vo} = \frac{V_{oc}}{V_{in}}$$

The problem is that, when connected to a non-ideal source, V_{in} ends up being less than the driving signal from the inside of the source, V_S, because of a voltage divider created by the signal source's output impedance, R_S, and the input impedance of the amplifier, r_{in}. So,

$$V_{in} = V_s \left(\frac{r_{in}}{R_s + r_{in}} \right)$$

At the output, the full-sized V_{oc} also encounters a voltage divider, so that the real (often called "loaded") output voltage, V_o, is reduced in amplitude as well:

$$V_o = V_{oc} \left(\frac{R_L}{r_{out} + R_L} \right)$$

The overall gain for the amplifier (which doesn't include the loss at the input) is

$$A_v = \frac{V_o}{V_{in}}$$

If you substitute in the formula for V_o, this ends up as

$$A_v = A_{vo} \left(\frac{R_L}{r_{out} + R_L} \right)$$

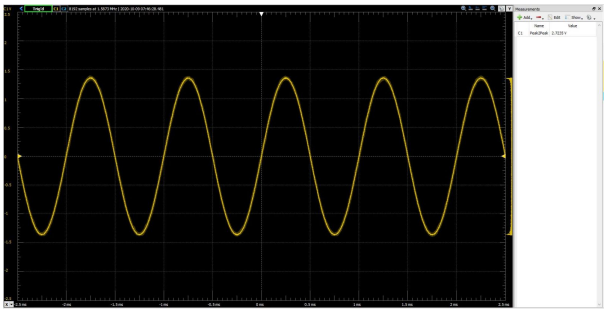
Empirical Amplifier Analysis

An amplifier may be considered as a "black box" -- something that we can get information out of, but we can't see what's inside. However, by taking appropriate measurements, we can determine what's inside the box.

One very useful tool to finding out what's "in the box" of an amplifier, or for that matter any non-ideal voltage source, is to measure the output when there's no load attached. That's where the "vo" in A_{vo} comes from, and the"oc" in v_{oc}. This is the "open circuit" measurement of the source. Since, with no load, there's no current and therefore no voltage drop across the output impedance, we can "see" the internal voltage of the device.

This is true of a signal source such as a function generator as well as for an amplifier -- if we measure the output of a function generator with a high-impedance tool like an oscilloscope or DMM, we get to see the "internal" or open circuit voltage. However, if we attach a load to the function generator, the voltage drops. From this, we can actually determine what the output impedance of the function generator is. Here's a real-life example. The first screenshot is of the output from a function generator directly measured by an oscilloscope. The second one is the same setup, but with a 100 Ω load resistor connected to ground.

3.87 V_{p-p}



2.72 V_{p-p}

Clearly, connecting the load resistor had a big effect, which would not have been the case if the function generator had zero output impedance.

Since the loss is due simply to the voltage divider between the source impedance and the load impedance, we can say

$$V_L = V_S \left(\frac{R_L}{R_S + R_L} \right)$$

...which rearranges to

$$R_S = R_L \left(\frac{V_S - V_L}{V_L} \right)$$

Using this rearranged voltage divider, the internal impedance of the function generator must be _____ Ω

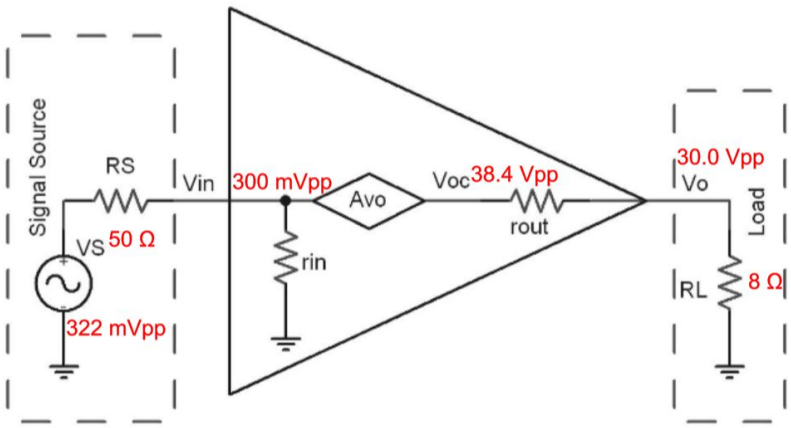
Applying the same logic to our "black box" amplifier model, we can determine the input and output impedances of the amplifier by driving it using a source with a known output impedance, R_S, and by connecting it to a known load. Using the variables from the model,

$$r_{in} = R_S \left(\frac{V_{in}}{V_S - V_{in}} \right)$$

$$r_{out} = R_L \left(\frac{V_{oc} - V_o}{V_o} \right)$$

Question: Working late in your lab one night, your eyes beheld the strangest sight: an amplifier with no specification label. You grab your 50 Ω function generator and an 8 Ω speaker and set to work. With everything connected together, the voltage at the input is 300 mV_{p-p} and the voltage at the output is 30.0 V_{p-p}. You disconnect the speaker and measure 38.4 V_{p-p}. With the amplifier disconnected, the function generator's signal measures 322 mV_{p-p}.

1. Start by sketching the black box model of this system, and applying the values supplied to the various nodes and resistances. You should end up with the following:



2. The amplifier's open circuit gain, A_{vo}, must be _____
3. The amplifier's loaded gain, A_v, is _____
4. The amplifier's input impedance appears to be _____ Ω
5. The amplifier's output impedance appears to be _____ Ω

There! Without knowing anything about the components inside the box, we've determined ***empirically*** all of the characteristics of this amplifier.

We will be analyzing specific amplifier circuits, and for these we will be able to predict their input and output impedances and their open circuit gains based upon components used in the design. However, we will always come back to this emperical analysis procedure when we want to determine the actual values of these characteristics.

Online Homework System

Assignment Worksheet
5/20/22 - 9:30:35 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Introduction to Operational Amplifiers

Question 1: (1 point)

Introduction to Operational Amplifiers (Op Amp)

In this revision of the Semiconductors course, we have not built any discrete transistor amplifiers. These amplifiers are hard to design, finicky, usually have poor input and output impedances, can't handle DC signals or very high frequency signals, and usually give you the choice between stability and high gain -- one or the other, but not both. Consequently, these amplifiers are almost never used anymore.

For years, the goal of analog electronics was to come up with the "perfect" amplifier-in-a-box, a device that could be used for practically any application without needing to know "what's in the box". This was referred to as an "operational amplifier" -- a pre-packaged device for which you just needed to know how to make it work, not why it worked the way it did. Here were some of the design goals:

- infinite input impedance
- zero output impedance
- really high, or infinite, gain
- differential inputs (and maybe even differential outputs)
- bandwidth from zero (DC) to infinity

With ***infinite input impedance***, the amplifier could be connected to any source, ideal or non-ideal, without any loss of signal due to loading. In other words, the amplifier would draw no current from the source, and would be completely undetectable. V_{in} would always equal V_S in the "black box model" of an ideal amplifier.

With ***zero output impedance***, the output signal would be unaffected by any load that could be attached, except for a dead short to ground. V_o would always equal V_{oc}.

With ***infinite gain*** the actual gain could be brought down to anything you wanted using negative feedback.

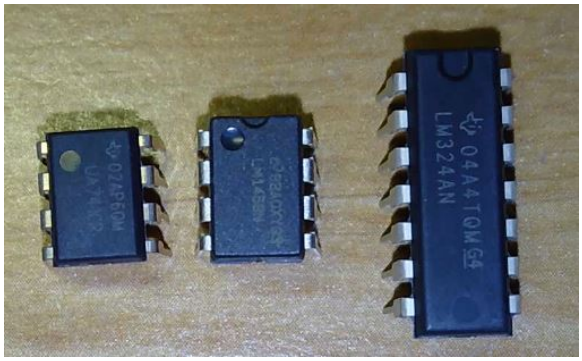
With ***differential inputs*** the amplifier would amplify the ***difference*** between the signals on its two inputs. This would allow for the amplifier to be inverting or non-inverting, or to use a differential two-wire signal referenced to itself rather than to ground. Also, any signal that appeared equally on both inputs would be automatically eliminated by superposition.

And of course, if the amplifier came with ***DC to infinity bandwidth***, you could add your own filters to pass only the frequencies you wanted, and you'd be able to manipulate super-slow signals (practically DC, often called "pseudo DC") like those generated by temperature sensors and other real-world sensors.

The first attempts at building operational amplifiers were promising in terms of approaching the design specifications, but they were completely impractical in terms of size, complexity, and cost. An early design involved dozens of vacuum tubes and high voltages; another design involved dozens of transistors. Then, in 1958, Jack Kilby came up with a way of building multiple transistors on a single piece of silicon, which he patented as "integrated circuit" technology, and suddenly there was a practical way to build an operational amplifier.

The operational amplifiers (OK, let's start calling them op amps) in your parts kit cost only pennies and can be tiny -- the ones in your kit have been cast in plastic to make them big enough to handle and work with, and so you can mount them on your breadboards. Surface mount versions of these can be really tiny.

Here are the three op amp ICs in your kit.



The one on the left is a single op amp -- the 741. The one in the middle has two op amps in it (dual op amp) -- the 1458. The one on the right has four op amps in it (quad op amp) -- the 324. You'll notice other characters before and after the numbers -- the ones in front indicate the manufacturer or designer, and the ones after specify things like grade of design and packaging. Often if you see an 'N' or a 'P' at the end it means it's dual inline pin (DIP) and can be used on a breadboard; 'D' usually means surface mount in an SOIC-style package -- not a good choice for breadboarding (keep that in mind when you get to courses where you order the components you'll be using!).

The 741 Op Amp

An old standby design, the 741 is an inexpensive and not very fancy IC; however, it's good enough for most of what we will need it to do. The 1458 and 324 op amps have pretty similar characteristics to the 741, just with multiples per IC. If you want better characteristics, and you'll soon be learning about some of the things you might need to improve upon, you'll end up paying more and having more difficulty sourcing the components.

Let's see how the 741 stacks up against the design standards discussed above. Look up the 741 Specification Sheet (https://www.ti.com/lit/ds/symlink/lm741.pdf?ts=1603937430839&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FLM741%253Futm_source%253Dgoogle%2526utm_medium%253Dcpc%2526utm_campaign%253Dasc-null-null-GPN_EN-cpc-pf-google-wwe%2526utm_content%253DLM741%2526ds_k%253DLM741%2526DCM%253Dyes%2526gclsrc%253Daw.ds%2526%2526gclid%253DEAIaIQobChMIju-ovNzY7AIVIgnnCh1bjwrKEAAYASAAEgJjPfD_BwE) and answer the following questions, based on the first set of specs labelled "LM741".

1. What is the stated typical input impedance? _____ _____ . A fairly typical single-transistor amplifier has an input impedance in the 5 kΩ to 10 kΩ range, so that's a significant improvement! We'll soon discover that, in an actual circuit with negative feedback, the input impedance is much, much higher than the specified open-circuit input impedance.
2. The output impedance isn't stated on the specification sheet, but from an Internet search, it appears to be 75 Ω for the open-circuit device. That same fairly typical single-transistor amplifier has an output impedance in the 1 kΩ to 5 kΩ range, so this is again a big improvement. As with the input impedance, when we add negative feedback to the op amp, its output impedance improves dramatically.
3. Look up the average Large signal voltage gain. _____ _____ . Convert that into a simple ratio: _____ . The single transistor amplifier we've been comparing to has a gain of about 20, so the op amp's gain is huge!
4. Take a look at the two input pins on the schematic symbol for the op amp. This tells us that the amplifier has _____

5. Last, and unfortunately the biggest issue: In the 741 chart they don't even mention bandwidth, so look in the 741A chart to find the typical bandwidth _____ MHz. Since this is a real sticking point for the op amp, let's also look at its minimum value, converted to kilohertz: _____ kHz. Given that FM radio stations are from 88 MHz to 108 MHz, clearly this amplifier can't even touch signals like that. And, unfortunately, things get worse when we try to do any kind of actual signal amplification with the op amp -- the listed bandwidth is for when its gain is just 1, or no amplification at all, and it decreases with gain.

So the operational amplifier provides us with some interesting and close to ideal characteristics that make it easy to work with, but it has some limitations that must be considered when using it for certain applications, particularly those where speed and bandwidth are concerned.

Online Homework System

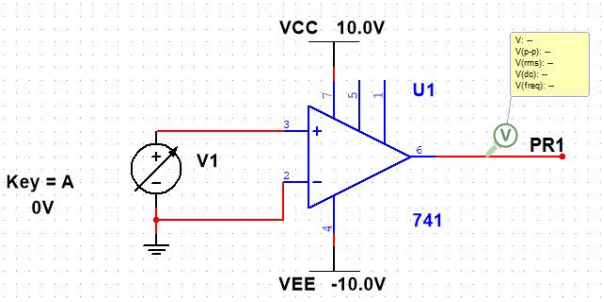
Assignment Worksheet
5/20/22 - 9:31:00 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Op Amp Model

Question 1: (1 point)

Op Amp Model

The huge gain of the op amp presents some interesting characteristics. Consider this: if the op amp had infinite gain, any non-zero input would produce an infinite output, because infinity times anything other than zero is infinity. Try this in Multisim:



The input signal is a DC_INTERACTIVE_VOLTAGE. Set it to a Maximum value of 0.1 V and a Minimum value of -0.1 V, and set the increment to 0.5%. Run the simulator, and see if you can get anything other than some maximum value (around 9 V) and a similar minimum value (around -9V).

Apparently, it's basically impossible to get anything out of this circuit other than its saturation values -- completely maxed out in either the positive or negative direction. A quick calculation will help you see why.

1. The gain of the 741 op amp is typically 200,000. If the input voltage to the circuit above is +0.05 V, what is the calculated output? _____ V. However, the amplifier is only powered by a +10 V source, so it can't produce a voltage that high. In fact, since this is not a "rail to rail" op amp, it can't even get to +10 V out. So try as it might to produce 10,000 V, it's stuck at around 9 V.
2. If the input voltage to the circuit above is -0.005 V, what is the calculated output? _____ V. Again, due to its limitations, it's stuck at around -9 V.
3. If the maximum output voltage is +8 V, what is the biggest input signal that can be amplified by this op amp? _____ μV. Using your digital multimeter (DMM), can you accurately measure just a few microvolts? _____ If you saw a measurement as small as 50 μV, you would probably record it as _____ V.

The pessimists in the group are probably saying "What's the use of an amplifier that can't be used to amplify any signal bigger than zero volts?" and the optimists are saying "I dunno -- there must be some way to make lemon juice out of this."

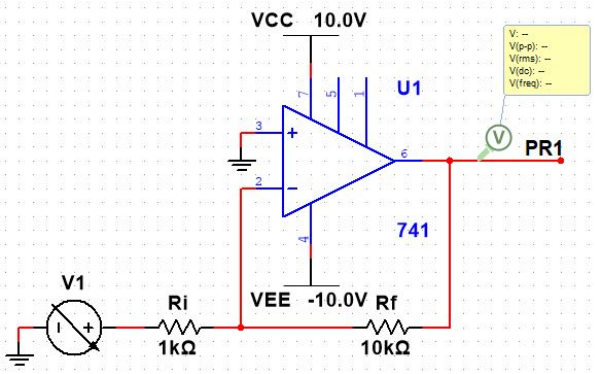
It turns out that this feature of the op amp helps us develop a really simple model to help us analyze any amplifier circuit. Based upon this interesting feature of the op amp and what we know about its input impedance, here are the *just two* parts of the op amp model:

Op Amp Model

- ***No current flows into or out of the inputs*** of an op amp, because we consider the input impedances to be infinite.
- ***Virtual Short between inputs***: The voltage difference between the input pins will be so small when the op amp is acting as an amplifier that it can be considered as zero. (It's not a true short, because no current flows into or out of the inputs.)

That's it! That's all you need to know to analyze any operational amplifier circuit!

When we build op amp circuits, we add other components, like resistors, to the circuit, typically to introduce Negative Feedback. Any component that goes ***from the output to the inverting input*** introduces negative feedback, which reduces the overall gain of the amplifier. Here's a circuit with two resistors, one as feedback (R_f) and one at the input (R_i). This second resistor is sometimes the input impedance for the op amp, but sometimes it isn't, so we don't call it r_{in}. It's just a part of what's called the ***feedback network***. Again, you may want to build this circuit in Multisim to verify that it does what we expect it to do, based on our newly-acquired model.



4. Using the model, what voltage is the inverting input, pin 2, at? _____ V
5. If V_1 = +0.5 V, use Ohm's law to predict how much current, in milliamps, flows through R_i. _____ mA
6. Using the model, how much of this current flows into the inverting input? _____ mA
7. The current flowing through R_f must be flowing toward a negative voltage. According to Ohm's law, what must that voltage be? _____ V (Consider the op amp as a "black box" that does whatever it takes to keep the voltage difference between its inputs at zero.)
8. Given that the answer to the previous question is V_{out} for this circuit, what is the gain of this amplifier? _____

We can now relate what we know back to the values of the resistors.

$$A_v = \frac{V_{out}}{V_{in}} = \frac{-IR_f}{IR_i} = -\frac{R_f}{R_i}$$

In this case, $A_v = -\frac{R_f}{R_i} = -\frac{10\ k\Omega}{1\ k\Omega} = -10$

9. Based upon this, what output would be expected if the input signal was -250 mV? _____ V (Try it and see!)
10. What would be the expected output if the input was +0.2 V? _____ V (Again try it!)
11. If the output was +7.4 V, what must the input have been? _____ V (Do it! Do it!)
12. If the input was -3.0 V, what will the output be? _____ (It still can't jump over a tall building or stop a speeding train.)
13. If the input was a sine wave with an amplitude of 300 $mV_{p\text{-}p}$ at a frequency of 1 kHz, describe the expected output:

- Expected amplitude: _____ $V_{p\text{-}p}$
- Expected phase relationship: _____
- Expected frequency: _____ kHz (You can replace the DC supply with a function generator, and view the input and output using an oscilloscope to verify these answers.)

In the next lesson, we'll revisit this amplifier and develop the standard characteristics expected for some other standard op amp circuit configurations.

Online Homework System

Assignment Worksheet
5/20/22 - 9:31:29 AM MDT

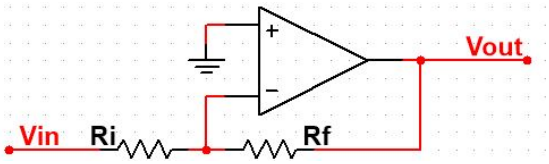
Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Op Amp Configurations

Question 1: (1 point)

Op Amp Configurations

We've already investigated one of the most commonly used configurations of op amp circuits. so we'll formalize that discussion here before going on to others.

Inverting Op Amp Circuit



We've determined the gain previously, so it will be included in the key points below.

Notice that this simplified diagram doesn't include power connections. No op amp, or any other semiconductor circuit, can operate without power -- this is just an over-simplification that is frequently used to emphasize the importance of the feedback network. In reality, you would source a physical op amp, determine what its pin numbers are, and power it using DC power supplies -- typically two supplies, one positive and one negative, although there are some "single rail' op amps available. (These cannot produce negative voltages at the output, so they introduce a whole host of issues with trying to add a DC offset to any AC signals that are to be amplified. We won't concern ourselves with this issue in this course.)

As with all op amp circuits, the output impedance of the inverting amplifier is so small as to be negligible, so we typically consider it to be zero.

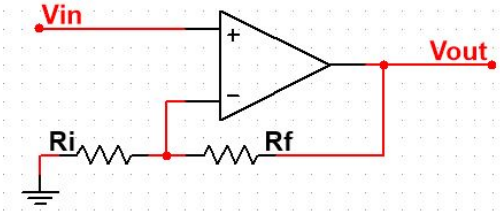
Unfortunately, even though the inverting input of the op amp has a practically infinite impedance, current flows from the signal source through R_i to a virtual ground point. Any time current is drawn from the signal source, the input impedance is not infinite. In this case, the input impedance is, in fact, R_i.

$$A_v = -\frac{R_f}{R_i}$$

$$r_{in} = R_i$$

$$r_{out} = 0$$

Non-Inverting Op Amp



Notice the similarities and differences between this circuit and the previous one. The two resistors are still in a network with the inverting pin -- to reduce the gain, negative feedback is required. However, the Ground and V_{in} have been swapped. Let's do a quick analysis of this configuration, using our two-piece model, then summarize the results below.

1. If, as before, the input signal was +0.5 V, what is the voltage expected at the inverting input, using our model? _____ V
2. If, again as before, R_i = 1 kΩ, how much current, in milliamps, will flow through it from the voltage present at the inverting input? _____ mA
3. Using our model, how much current comes out of the inverting input? _____ mA

4. Given that the current has to come from somewhere, what voltage must exist across R_f in order to supply this current, if R_f = 10 k Ω? _____ V
5. Now, add the voltage across R_f to the voltage at the inverting pin to determine what V_{out} must be, referenced to ground. _____ V
6. Determine the gain of this amplifier, based upon V_{out} and V_{in}. _____

Using Ohm's law, we can once again determine how the gain of this amplifier relates to the resistors in the feedback network:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{IR_f + IR_i}{IR_i} = \frac{R_f + R_i}{R_i} = \frac{R_f}{R_i} + 1$$

7. Notice that the input signal goes directly to the non-inverting input, with no other resistors either in series or to ground. From our model, this means that the input impedance is _____

Again, the output impedance is practically zero.

So, in summary, for the non-inverting op amp circuit:

$$A_v = \frac{R_f}{R_i} + 1$$

$$r_{in} = \infty$$

$$r_{out} = 0$$

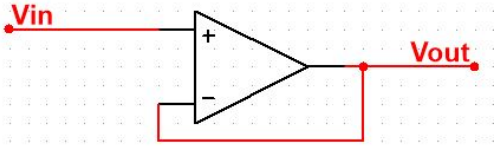
In other words, this is almost the ideal amplifier, if it weren't for the "+1" in the gain expression. In fact, this limits the non-inverting amplifier significantly, because it cannot be used as an "attenuator" -- a circuit that decreases the amplitude of the input signal.

However, for the optimists in our midst, this offers the opportunity for one more useful op amp configuration -- the Unity Gain Buffer. We've discussed current buffers previously in terms of switches that drive LEDs, relays, or motors, but now we can do the same with an amplifier. Let's develop it from the non-inverting amplifier.

8. If we wanted to reduce the gain of the non-inverting amplifier to +1, the "R_f/R_i" would need to be reduced to _____
9. In order to reduce the "R_f/R_i" part to zero, R_f could be _____ . In a circuit, this would be a(n) _____ . In other words, we could replace the resistor with a wire jumper.
10. In order to reduce the "R_f/R_i" part to zero, R_i could be_____ . In a circuit, this would be a(n) _____ . In other words, we could simply not put a resistor to ground, and eliminate any reference to ground.

The resulting circuit would look like the one below.

Unity Gain Buffer



Notice that, according to our model, V_{out} has to be equal to V_{in}, because the inverting terminal, which is directly connected to V_{out}, has to be identical to V_{in} (virtual short). Also notice that V_{in} has no current path, since it is connected to a high-impedance input, so the input impedance is practically infinite.

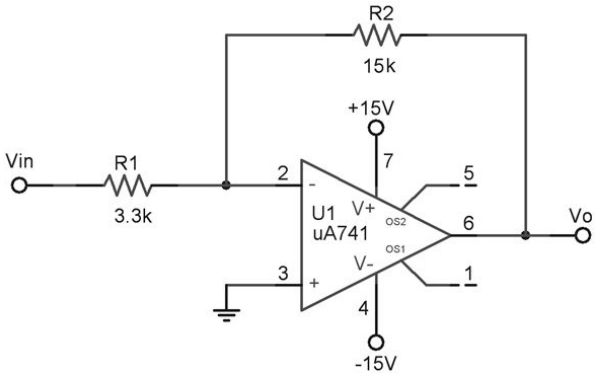
$$A_v = +1$$

$$r_{in} = \infty$$

$$r_{out} = 0$$

Exercises and Applications

Use the schematic diagram below to answer the questions that follow. (Note that sometimes the amplifiers are drawn with the inverting terminal on top, sometimes with the non-inverting terminal on top. Nothing changes in their functionality.)

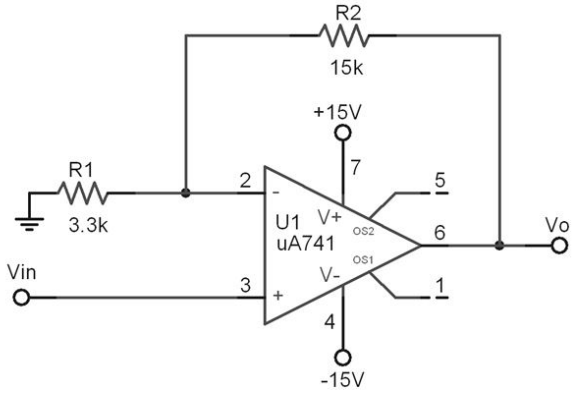


11. This amplifier is _____
12. What is the voltage gain? _____
13. What is the input impedance of this amplifier? _____
14. What is the output impedance of this amplifier? _____
15. Fill in the missing values in the following table, You may want to draw the "black box" amplifier model to help you with your results.

V_S, mV	R_S, Ω	V_{in}, mV	V_{oc}, mV	R_L, Ω	V_o, mV
+118	600	_____	_____	270	_____
_____	1000	_____	_____	1000	+1300

16. If this amplifier were to be driven by a function generator with an output impedance of 600 Ω set to a 50 mV_p sine wave at a frequency of 500 Hz, what would the output voltage be? _____ mV_p at _____ Hz, _____
17. If a Unity Gain Buffer were to be placed between the function generator and this amplifier circuit, what would the output voltage be? _____ mV_p at _____ Hz, _____

Use the schematic diagram below to answer the questions that follow.



18. This amplifier is _____
19. What is the voltage gain? _____
20. What is the input impedance of this amplifier? _____
21. What is the output impedance of this amplifier? _____
22. Fill in the missing values in the following table, You may want to draw the "black box" amplifier model to help you with your results.

V_S, mV	R_S, Ω	V_{in}, mV	V_{oc}, mV	R_L, Ω	V_o, mV
+118	600	_____	_____	270	_____
_____	1000	_____	_____	1000	+1300

23. If this amplifier were to be driven by a function generator with an output impedance of 600 Ω set to a 50 mV_p sine wave at a frequency of 500 Hz, what would the output voltage be? _____ mV_p at _____ Hz, _____

24. Would there be any difference expected if a unity gain buffer were to be installed between the signal source and the input to this amplifier? _____

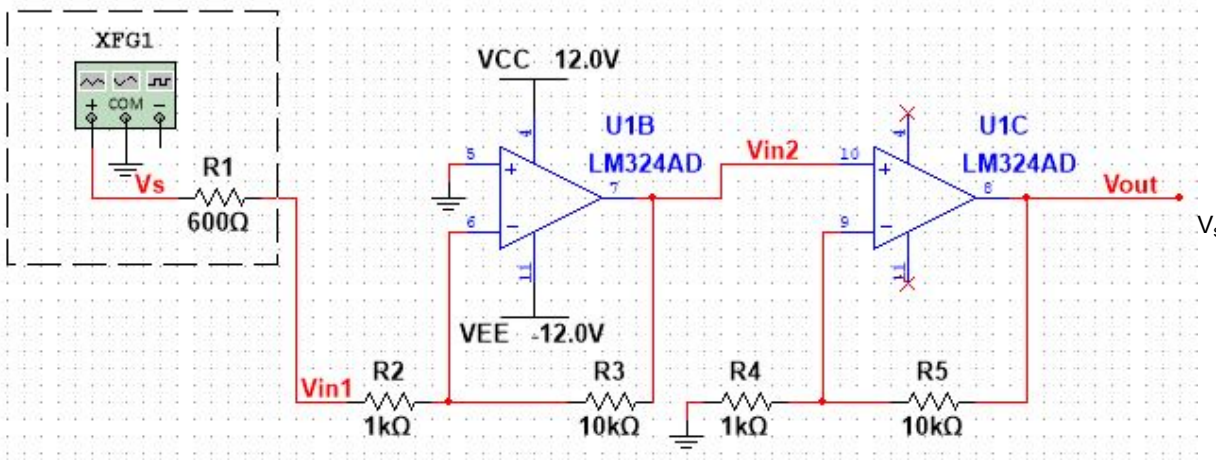
Cascaded Amplifiers

As was hinted at above, it is possible to connect amplifiers together, something called "Cascading". There are really only about five things you need to know about cascading amplifiers:

- The overall gain of the amplifier is the ***product*** (i.e. multiply together) of the gains of the individual stages
- The input impedance of the cascaded amplifiers is the input impedance of the first stage
- The output impedance of the cascaded amplifiers is the output impedance of the last stage
- If the amplifier stages do not have ideal input impedances (i.e. infinite) or ideal output impedances (i.e. essentially zero), the losses between stages need to be determined using the "black box" model. This won't be an issue for op amps, because their output impedances are ideal.
- Good design puts the amplifier with the best (highest) input impedance first and the best (lowest) output impedance last

25. Two op amp circuits, both using R_i = 3.3 kΩ and R_f = 15 kΩ are to be cascaded together. One is inverting, the other is non-inverting. (You've just finished analyzing these two amplifiers in the preceding questions.) What is the overall gain of the cascaded amplifier? _____
26. How should they be connected together? _____
27. If the non-inverting amplifier was put first and the amplifier was to be driven by a 50 mV_p sine wave from a function generator with an output impedance of 600 Ω, what would V_{in} be? _____ mV_p, and what would V_{out} be? _____ V_p, _____
28. If the inverting amplifier was put first with the same signal from the same function generator, what would V_{in} be? _____ mV_p, and what would V_{out} be? _____ V_p, _____

Carefully follow through the analysis of the worked example below.



V_s = 100 mV_p @ 1 kHz

U1B, the first stage, has the signal presented to its inverting terminal, with the non-inverting terminal grounded. This makes it a classic inverting amplifier.

Its gain, then, will be

$$A_{v1} = -\frac{R_f}{R_i} = -\frac{10\ k\Omega}{1\ k\Omega} = -10$$

U1C, the second stage, has a signal presented to its non-inverting terminal, with a grounded negative feedback network connected to its inverting terminal. This makes it a classic non-inverting amplifier.

Its gain, then, will be

$$A_{v2} = \frac{R_f}{R_i} + 1 \ = \ \frac{10\ k\Omega}{1\ k\Omega} + 1 = 11$$

The overall gain of the amplifier, then, will be

$$A_{vT} = A_{v1} \cdot A_{v2} = -10 \cdot 11 = -110$$

Since the first stage is an inverting amplifier, its input impedance is R_i = 1 kΩ

This means there is a voltage divider created by the internal impedance of the signal generator and the amplifier's input impedance.

$$V_{in1} = V_s \left(\frac{r_{in1}}{R_S + r_{in1}} \right) = 100\ mV_p \cdot \left(\frac{1\ k\Omega}{0.6\ k\Omega + 1\ k\Omega} \right) = 62.5\ mV_p$$

We can determine Vout two ways.

First, we can follow through the stages, determining the voltages as we go.

$$V_{out1} = V_{in1} \cdot A_{v1} = 62.5\ mV_p \cdot -10\ = \ 625\ mV_p,\ inverted$$

Since the output impedance of the first stage is practically zero, $V_{in2} = V_{out1} = 625\ mV_p$, inverted.

$$V_{out} = V_{in2} \cdot A_{V2} = 625\ mV_p \cdot 11\ = \ 6.875\ V_p,\ inverted$$

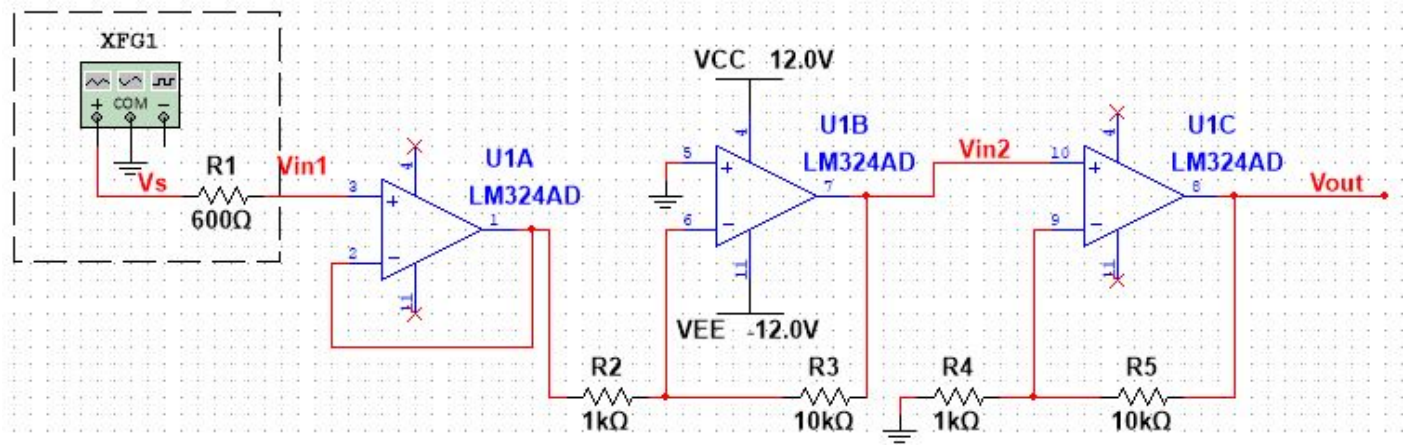
Since the output impedance of the second stage is practically zero, it wouldn't matter if we attached a load resistor (within reason) -- the loaded output would be the same as the open circuit output, at 6.875 V_p, inverted.

The simpler solution would be to take the input signal and multiply it by the overall gain:

$$V_{out} = V_{in1} \cdot A_{VT} = 62.5\ mV_p \cdot -110 = \ 6.875\ V_p,\ inverted$$

It's unfortunate that the input signal is less than the source signal, due to the imperfect input impedance of the first stage. We could fix this problem by reversing the two amplifiers -- put the non-inverting stage first, followed by the inverting amplifier. In this configuration, $V_{in1} = V_s$ so $V_{out} = V_{in1} \cdot A_{VT} = 100\ mV_p \cdot -110 = 11.0\ V_p,\ inverted$

Another solution, since we've got a quad op amp in the circuit, would be to place a unity gain buffer in front of the inverting amplifier, as shown here.



In this case, the input impedance of the unity gain buffer is practically infinite, so $V_{in1} = V_s$. The gain of the first stage is +1, so the overall gain is still -110. Thus,

$$V_{out} = V_{in1} \cdot A_{VT} = 100\ mV_p \cdot -110 = 11.0\ V_p,\ inverted$$

Non-Ideal Amplifier Characteristics

This topic isn't directly related to Op Amp Configurations, but it will help you understand why we assume the input and output impedances of the op amp are practically ideal.

We've made reference to the Feedback Network of the op amp, and discovered that it establishes the gain of the op amp, assuming that the gain is so big that we can consider the voltage between the two input pins to be essentially zero (i.e. Virtual Short). Without going into too much detail, there's a mathematical reason for that, which comes down to an analysis of these two resistors appearing as a voltage divider between the output of the amplifier and ground, with the inverting input in the middle. To help with associated analyses, the resistor ratio in the voltage divider has been called β, which is unfortunate because it has nothing to do with the β we used for the BJT Transistor.

$$\beta = \frac{R_i}{R_f + R_i}$$

As you can see, this β can't be bigger than one.

This β is combined with the open circuit gain of the amplifier to create a new term, $1 + A_{vol}\beta$, that can be applied to the actual gain, the input impedance, and the output impedance of a non-ideal op amp (i.e.) one that doesn't have a huge gain. Here are the related expressions for the non-inverting configuration of the op amp, where the "ol" values are the open loop numbers from the manufacturer's specification sheet.

Non-Inverting Amplifier, Non-Ideal Calculations

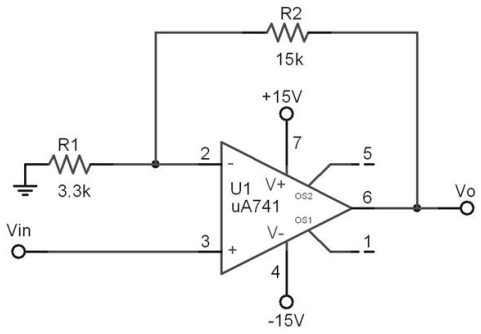
$$A_v = \frac{A_{vol}}{1+A_{vol}\beta}$$

$$r_{in} = (1 + A_{vol}\beta) r_{in_{ol}}$$

$$r_{out} = \frac{r_{out_{ol}}}{1+A_{vol}\beta}$$

Interestingly, we'd have to have a really bad op amp for these formulas to show the non-ideal characteristics of the amplifier, so we'll start by assuming we've got an amplifier with similar characteristics to the 741, except the gain. For historical reasons, we'll give you that gain in dB, which will have to be converted to a V/V ratio before you can use it.

29. Our non-ideal amplifier has an open loop voltage gain of 34 dB. What is that as a V/V ratio? _____ Round this value to the nearest whole number to simplify the rest of the calculations.
30. We'll use this amplifier in a non-inverting amplifier with the same resistors as our previous example:



31. What would the gain of this amplifier be, using the non-ideal non-inverting amplifier formulas above? _____ , which is a bit lower than the +5.55 we got for our previous ideal calculation.
32. Given that the specification sheet gave us r_{inol} = 300 kΩ, determine the non-ideal r_{in} for this amplifier. _____ _____
33. Assuming the op amp has an r_{outol} = 75 Ω, what is the output impedance for our non-ideal amplifier? _____ _____

Those input and output impedances look pretty good. But let's see what they look like if we use the real gain of the 741 op amp, 200,000 V/V.

34. What would the gain of this amplifier be, using the non-ideal non-inverting amplifier formulas above? _____ , pretty much what we predicted with our ideal model.
35. Given that the specification sheet gave us r_{inol} = 300 kΩ, determine the non-ideal r_{in} for this amplifier. _____ _____ That's practically infinity!
36. Assuming the op amp has an r_{outol} = 75 Ω, what is the output impedance for our non-ideal amplifier? _____ _____ And that's practically zero!

So, using our calculations for the non-ideal operational amplifier, we've finally proved that our model is actually valid: the input impedances of the inputs are practically infinite, the output impedance is practically zero, and we can predict the gains using just the feedback resistors.

Oddly, none of the textbooks on op amps include formulas for the non-ideal inverting amplifier. Here they are, just for you!

Inverting Amplifier, Non-Ideal Calculations

$$A_v = 1 - \frac{A_{vol}}{1+A_{vol}\beta}$$

$$r_{in} = R_i || \Big((1 + A_{vol}\beta) r_{in_{ol}} \Big)$$

$$r_{out} = \frac{r_{out_{ol}}}{1 + A_{vol}\beta}$$

From what you remember about parallel components, it should be fairly obvious that, for r_{in}, putting a resistor like 3.3 kΩ in parallel with a resistance in the gigaohms will result in $r_{in} \approx R_i$.

Now that you've seen these non-ideal formulas at work, you won't need them again (except for in an online quiz) -- they've just proved to us that our model is adequate for predicting the behaviour of op amps in circuit.

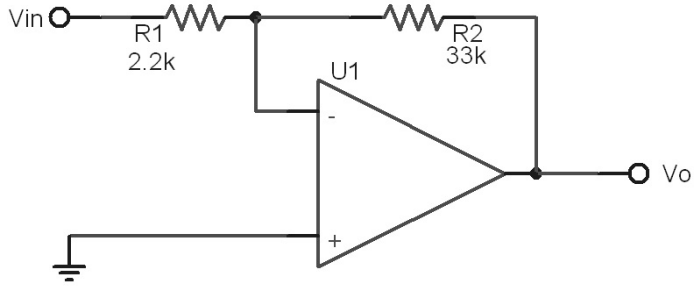
Online Homework System

Assignment Worksheet
5/31/21 - 1:54:21 PM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA12 Op Amp Theory Quiz

Question 1: (5 points)

Use the schematic diagram below to answer the questions that follow.



What is the gain of this amplifier? Include the correct sign to indicate if it is inverting or non-inverting. _____

If the input signal is -160 mV_{DC}, what will the output signal be? (Select correct polarity.) _____ _____ V_{DC}.

What is the input impedance for this amplifier?

(a) 33 kΩ

(b) Practically infinite

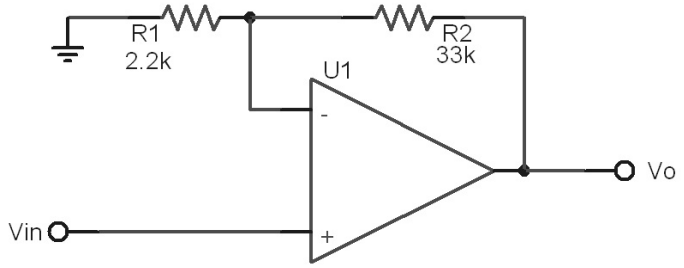
(c) 2.06 kΩ

(d) 2.2 kΩ

If the signal source generates an internal voltage of 1.4 V_p and it has an output impedance of 600 Ω, what would the input signal voltage to this amplifier be? _____ V_p.

Question 2: (4 points)

Use the schematic diagram below to answer the questions that follow.



What is the gain of this amplifier? Include a sign, if necessary, to indicate whether it is inverting or non-inverting. _____

What is the input impedance for this amplifier?

(a) Practically infinite

(b) 2.2 kΩ

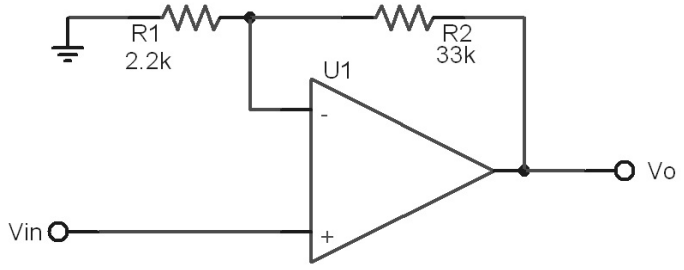
(c) 33 kΩ

(d) 2.06 kΩ

If a DC source with an output impedance of 600 Ω producing -1.00 V_{DC} is connected to the input, what output voltage is expected? _____ _____ V_{DC}.

Question 3: (4 points)

Use the schematic below to answer the following questions. Treat the op amp as non-ideal with an open-loop gain of 18 dB.



What is the open-loop gain in volts per volt? _____

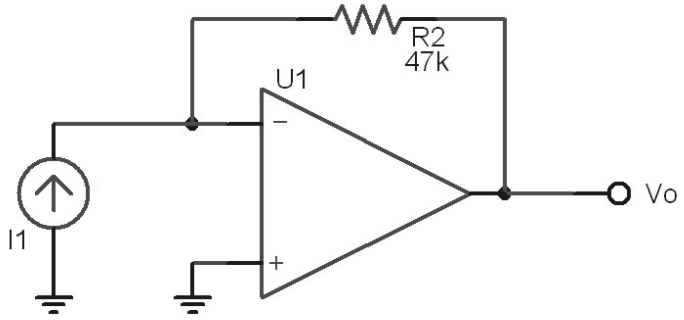
What is the non-ideal gain of this amplifier, based on the open-loop gain of 18 dB? _____

If the input impedance for the op amp from the data sheet is 50 kΩ, what is the non-ideal input impedance for this amplifier? _____ kΩ

If the output impedance for the op amp from the data sheet is 10 Ω, what is the non-ideal output impedance for this amplifier? _____ Ω

Question 4: (4 points)

Use the schematic below to answer the questions that follow.

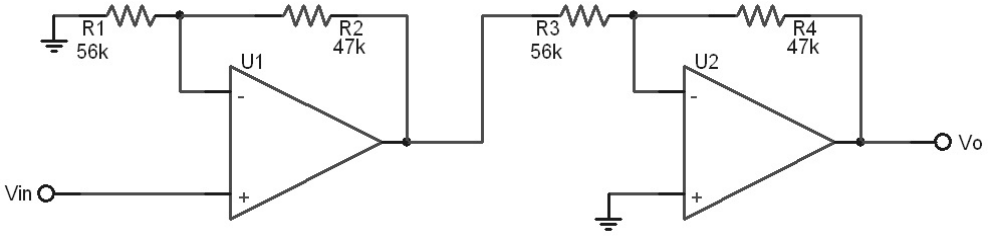


If the input current is 33 μA, what is the expected output voltage? _____ _____ VDC.

What current would be required to produce an output voltage of +1.0 V_{DC}? _____ _____ μA.

Question 5: (7 points)

Use the schematic below to answer the questions that follow.



What is the gain of the first stage? _____ _____

What is the gain of the second stage? _____

What is the overall gain of this amplifier? _____

The input impedance for this amplifier is

(a) 47 kΩ

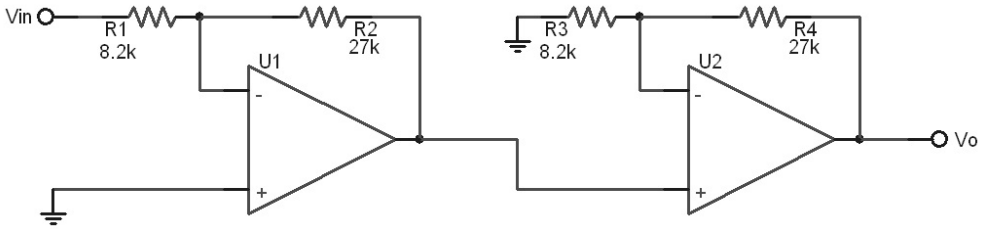
(b) 25.6 kΩ

(c) Practically infinite

(d) 56 kΩ

Question 6: (6 points)

Use the schematic below to answer the questions that follow.



What is the overall gain for this amplifier? _____ _____

What is the input impedance for this amplifier?

(a) 8.2 kΩ

(b) 27 kΩ

(c) Practically infinite

(d) 6.29 kΩ

If a function generator with a 600 Ω impedance introduces a 2.00 V_p sine wave to this circuit, what is the expected value of V_{in}? _____

What is the expected output signal for this amplifier with the input signal as described in the previous question? _____ V_p,_____ .

Online Homework System

Assignment Worksheet
10/18/22 - 1:49:26 PM MDT

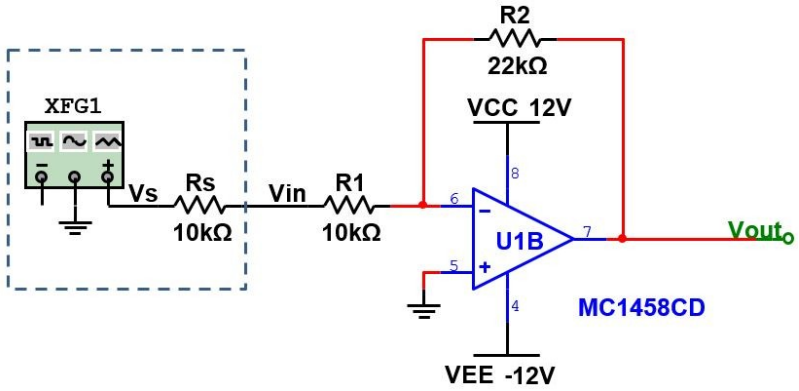
Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Lab06 Op Amp Configurations

Question 1: (10 points)

Lab 06 Pre-Lab: Op Amp Configurations

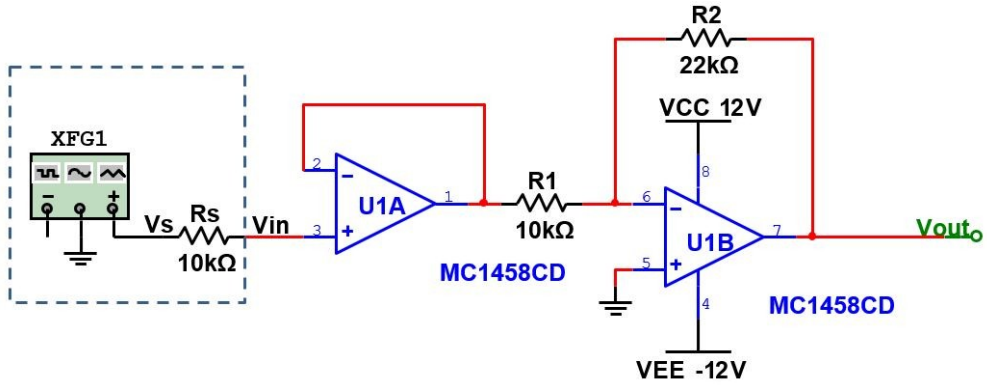
Note: Do not move on to the "Next" page until you have completed your Pre-Lab. The next page is the Lab Activity, and once you move to that page, you will not be able to return to the Pre-Lab page!

Use the schematic diagram below to answer the questions that follow.



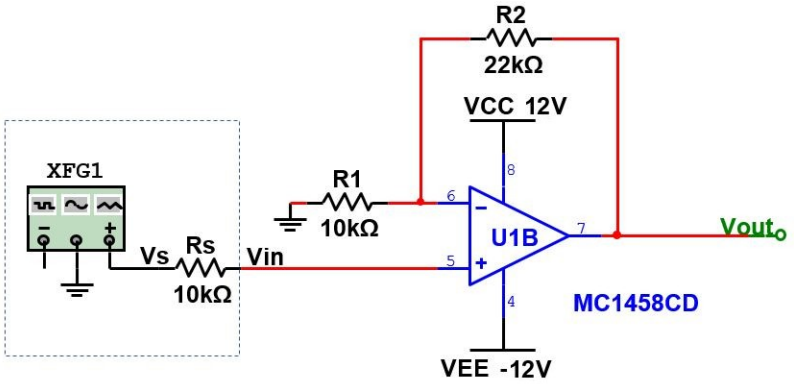
1. Determine the gain of this amplifier. _____ _____
2. What is the input impedance of this amplifier? _____ kΩ
3. If V_S = 1.0 V_p at 1.0 kHz, what will V_{in} be? _____ V_p at 1.0 kHz.
4. If V_{in} = 0.5 V_p at 1.0 kHz, what will V_{out} be? _____ V_p, _____

Use the schematic diagram below to answer the questions that follow.



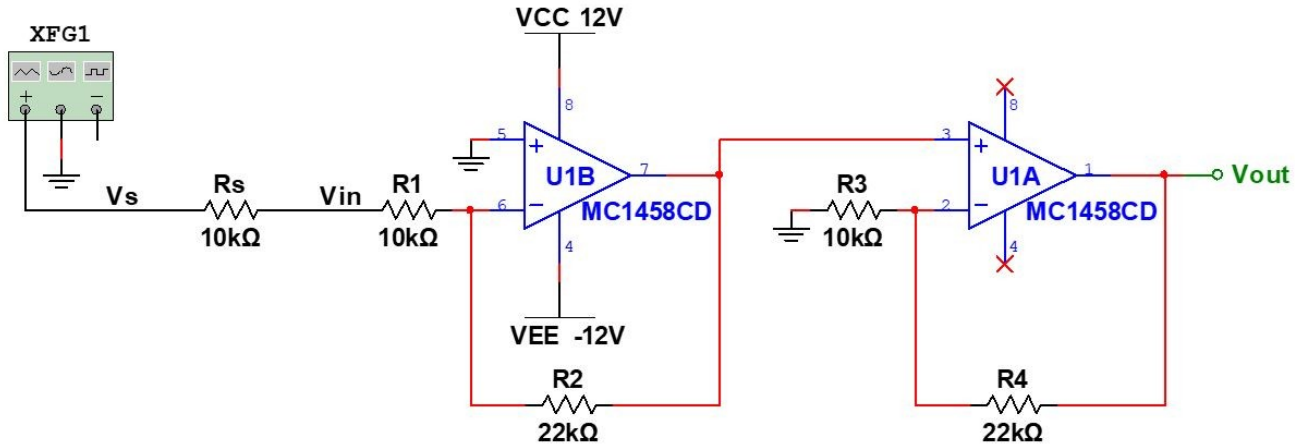
5. If V_S = 1.0 V_p, what is the expected value for V_{in}? _____ V_p
6. If V_S = 1.0 V_p, what is the expected signal for V_{out}? _____ V_p, _____

Use the schematic diagram below to answer the questions that follow.



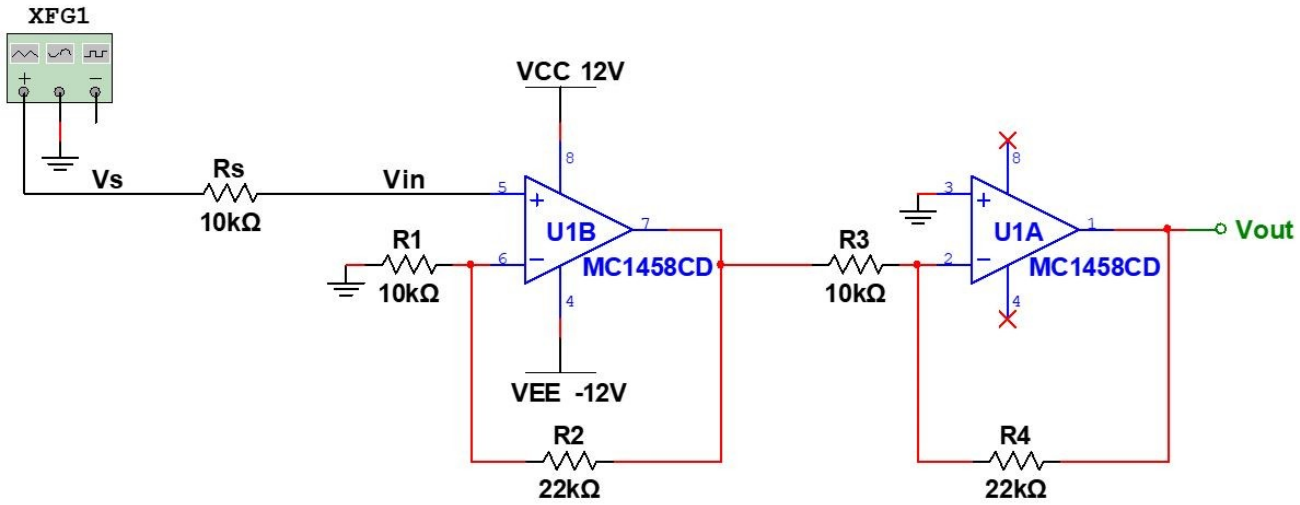
7. What is the gain of this amplifier? _____
8. What is its input impedance? _____
9. If V_S = 1.0 V_p at 1.0 kHz, V_{in} is expected to be _____ V_p at 1.0 kHz.
10. If V_S = 1.0 V_p, what is the expected signal at V_{out}? _____ V_p, _____

Use the schematic diagram below to answer the questions that follow.



11. What is the overall gain of this amplifier? (Don't forget to include inversion, if it is required.) _____
12. If V_S = 1.0 V_p, what will be the expected amplitude of V_{in}? _____ V_p
13. If V_S = 1.0 V_p, what will be the expected signal at V_{out}? _____ V_p, _____

Use the schematic diagram below to answer the questions that follow:



14. What is the overall gain of this amplifier? (Don't forget to include inversion, if it is required.) _____
15. If V_S = 1.0 V_p, what will be the expected amplitude of V_{in}? _____ V_p
16. If V_S = 1.0 V_p, what will be the expected signal at V_{out}? _____ V_p, _____

17. Select all correct statements regarding the last two circuits from the following list:

(a) The second circuit is, in essence, an ideal amplifier

(b) The phase of the output signals is different.

(c) The improvement in output amplitude is due to the input impedance.

(d) The second circuit has an improved output impedance.

(e) The gains of the two circuits are the same.

(f) The order of the amplifiers affects the overall gain.

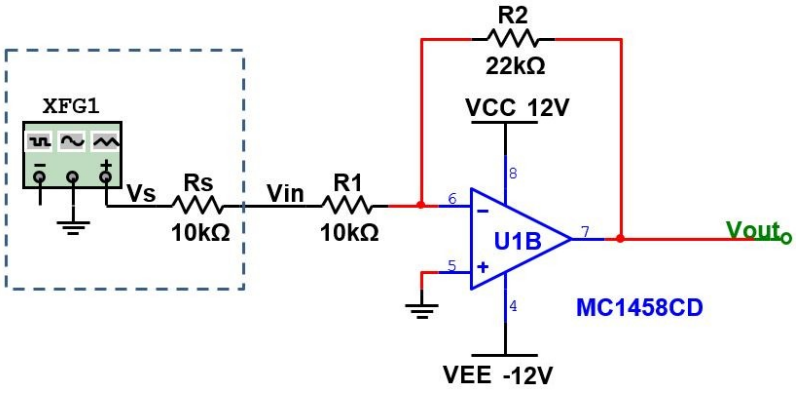
You have now completed the Pre-Lab. You may Save and Close or move on to the Lab Activity page, but do not "Submit" until you have completed the Lab Activity!

Question 2: (10 points)

Lab 06 Activity

Using your breadboard, construct and test the circuit below.

- Note that the op amp is labelled "U1B". This means it is the second of two parts in a dual op amp Integrated Circuit. You will be adding the other op amp in this IC to your design later.
- Use a signal generator with the following settings:
  - 1.0 kHz
  - Sine Wave
  - amplitude 1.0 V_p (Note that this is "peak"; some equipment doesn't offer that option, so double the value and use "peak to peak".)
  - Make sure, oscilloscope Channel 1, that your signal meets the specifications above before you move on.
- Use a dual power supply to produce both +12 V and -12 V. Your instructor may provide instructions as to how to configure the equipment.
- The "R_S" resistor is one you will place in your circuit to become the non-ideal output impedance of the function generator.
- Use oscilloscope Channel 1 to display and record the value for V_S, then move the probe so that Channel 1 displays the signal seen at V_{in} and Channel 2 displays the signal seen at V_{out}.



Record the following values. It is recommended that, for accuracy, you measure the peak-to-peak (AMPLITUDE) voltage and divide by two to get an accurate value for the peak voltage of a sine wave, since there may be a small DC offset that would affect the MAX or HIGH value (ground referenced) but not the peak-to-peak value (self-referenced).

1. V_S = _____ V_p
2. V_{in} = _____ V_p

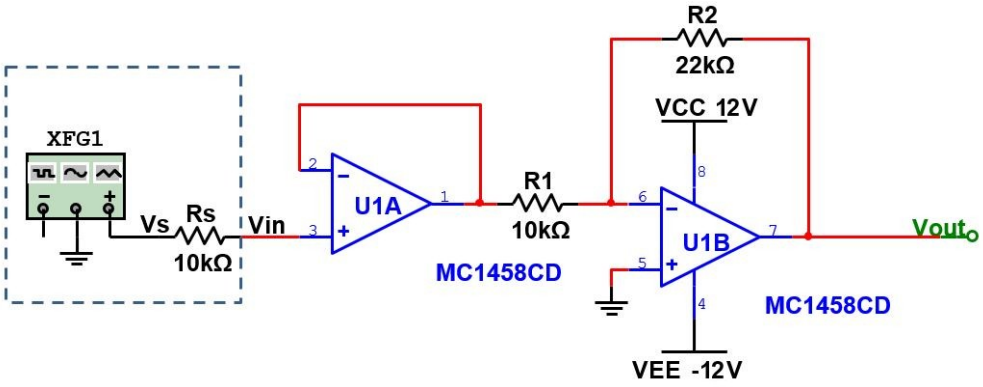
3. V_{out} = _____ V_p, _____ (this is V_{oc}, the open circuit output voltage)
4. Add a 330 Ω load resistor betwen the output and ground, and measure just the amplitude of V_{out} again: _____ V_p (this is V_o, the loaded circuit voltage)

From these measured values, determine the actual (empirical) values for the following (i.e. this question is not looking for the theoretical values from the Pre-Lab -- use the "black box" model).

5. A_{vo} = _____ (That's open, i.e. without the load resistor)
6. A_v = _____ (That's loaded)
7. r_{in} = _____ kΩ (This is ***not*** just the value of R_1,which is a theoretical prediction -- do the empirical calculation)
8. r_{out} = _____ Ω
9. With your circuit and oscilloscope visible, and with your oscilloscope set up to display V_{in} and V_{out} each maximized for proper measurements (i.e. the channels should ***not*** be set the same this time!), and with the measurements displayed on the oscilloscope, ask your instructor to grade your circuit and oscilloscope settings out of five marks. _____

Modify your existing circuit to match the changes in the following schematic diagram. Note that the new op amp is designated "U1A", which means it's the first of two parts in the IC you've already placed. You should end up with only one IC on your breadboard.

The setup for your signal generator should remain the same. Remove the load resistor.



Leave your oscilloscope Channel 1 probe on V_S, and use Channel 2 to display and measure the following signals: V_{in}, the voltage at the output of U1A, and V_{out}.

10. How does the voltage at the output from the Unity Gain Buffer (U1A) compare to V_{in}? _____
11. Measure V_{in}: _____ V_p
12. Measure V_{out}, unloaded: _____ , _____
13. Calculate the gain for this circuit: _____
14. Add a 330 Ω load resistor. Did the output signal amplitude decrease appreciably? _____
15. Select all the correct statements about this amplifier:

(a) The output signal is bigger due to the high input impedance.

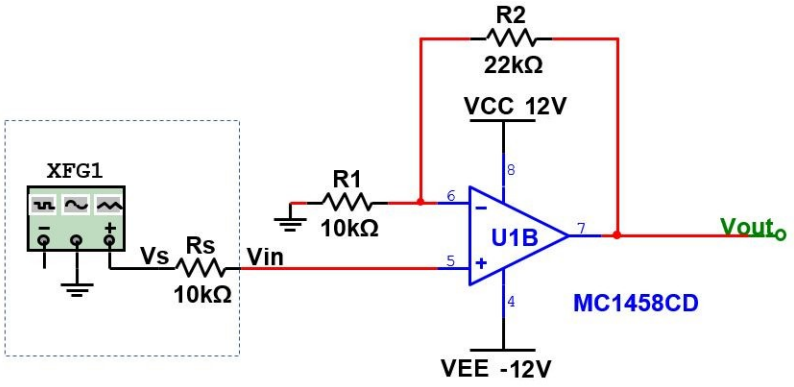
(b) The input impedance is practically zero.

(c) The output impedance is practically infinite.

(d) The gain is the same as the previous one.

Using your breadboard, build the circuit in the schematic diagram below, and answer the questions that follow.

The setup for your signal generator should remain the same.



Leave your oscilloscope Channel 1 probe on V_S, and use Ch2 to display and measure V_{in} and V_{out}. Record the following:

16. V_S = _____ V_p
17. V_{in} = _____ V_p
18. V_{out} = _____ V_p, _____

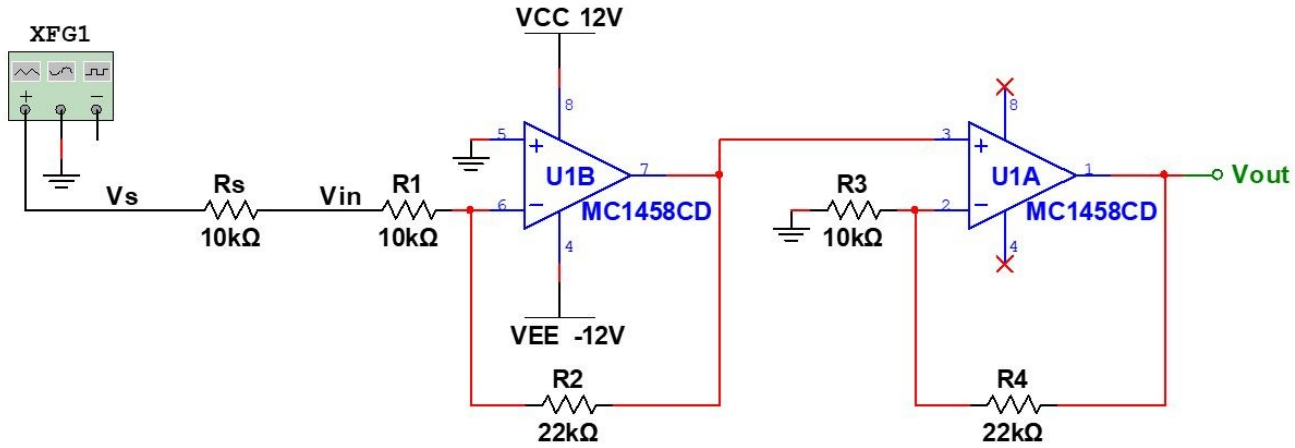
From these measured values, determine the actual (empirical) values for the following (i.e. this question is not looking for the theoretical values from the Pre-Lab -- use the "black box" model). If you want, you can check to see that adding the 330 Ω load makes no appreciable difference to your output signal, but we won't investigate that again formally.

19. A_v = _____
20. From your values, attempt to calculate r_{in}. If you get a negative number or a number in the megaohms, treat it as infinite. The input to this amplifier is essentially infinite:

(a) True
(b) False

Simulation

Use Multisim to create the circuit below, and answer the questions that follow. You will need to ensure one of the op amps is "U1A" and the other is "U1B". (Note the red 'X' symbols on the power pins of the second op amp in the IC -- this means the circuit is wired correctly, and power is being supplied to the power pins of the other half of the IC. If you don't get red 'X' symbols, you've done something wrong -- probably placed an op amp from a differently-numbered IC.) Use the Function Generator settings from the previous exercises, and verify that the input signal matches the specifications before proceeding.



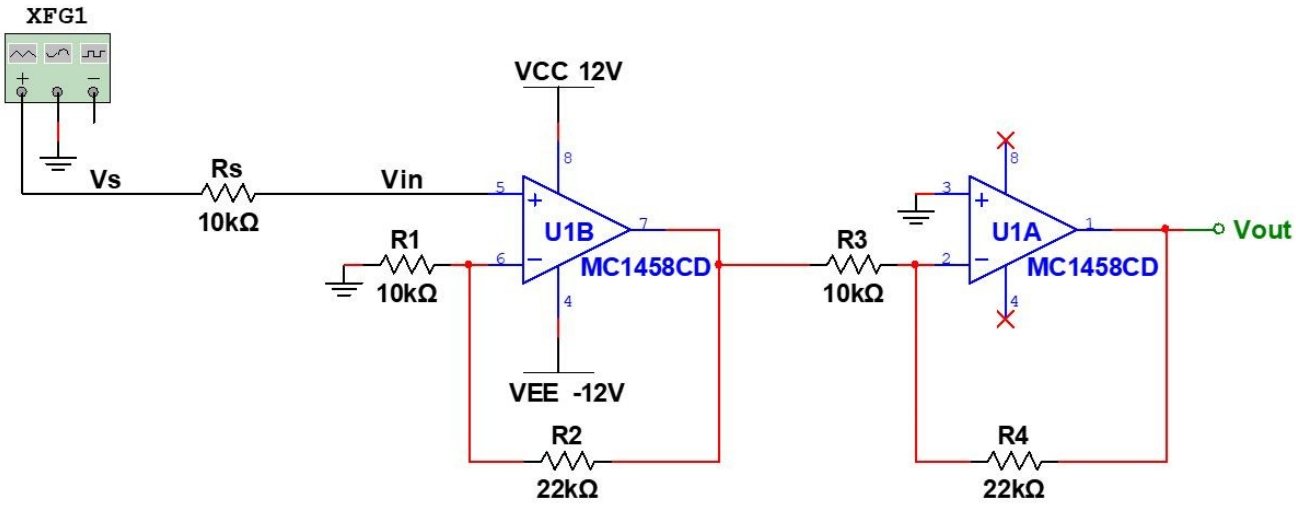
Use three channels of the Tektronix oscilloscope to display and measure V_S, V_{in}, and V_{out}. Record the following:

22. V_S = _____ V_p
23. V_{in} = _____ V_p
24. V_{out} = _____ V_p, _____

From these measured values, determine the actual (empirical) values for the following (i.e. this question is not looking for the theoretical values from the Pre-Lab -- use the "black box" model). If you want, you can check to see that adding the 330 Ω load makes no appreciable difference to your output signal, but we won't investigate that again formally.

25. A_v = _____
26. r_{in} = _____ kΩ

Now, reverse the two stages to create the following circuit, with the same input signal as before. Measure and record the items below.



27. V_S = _____ V_p
28. V_{in} = _____ V_p
29. V_{out} = _____ V_p, _____
30. Calculate the amplifier's gain: _____
31. Select all of the true statements from the following for the two cascaded amplifiers:

    (a) It makes no difference which stage comes first.

    (b) The input impedances are practically the same.

    (c) The gains of the two circuits are the same.

    (d) The output signal of the second is much bigger than the first.

32. With the function generator, circuit, and oscilloscope all visible, and with the signals displayed appropriately for good measurements on the oscilloscope along with the three measurements above on display, take a screen-shot and upload it here for a grade out of six marks. Document Upload (Direct)

You have now completed this Lab. Once you submit your results, you will not be able to return to this page!

Online Homework System

Assignment Worksheet
5/20/22 - 9:31:56 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Differential Amplification

Question 1: (1 point)

Differential Amplification

One of the desired characteristics of the operational amplifier was having differential inputs -- two inputs, one inverting and the other non-inverting. So far, we've seen that this allows us to create both inverting and non-inverting amplifiers. But that's only scratching the surface of what can be done with differential inputs on an amplifier.

If equal but opposite signals are applied to the two inputs of a differential amplifier, the output signal is amplified twice as much as it would have been for a single-input amplifier. The gain of a differential amplifier is

$$A_{v(diff)} = \frac{V_{out}}{(V_{in+} - V_{in-})}$$

Rearranged in terms of the output voltage,

$$V_{out} = A_{v(diff)} (V_{in+} - V_{in-})$$

To explain the difference in output signal size for a single-input amplifier *vs*. a differential input amplifier, consider the following example:

If the input signal to an amplifier with a gain of 10 was +1.0 V:

- applying the signal to the non-inverting input while the inverting input was at ground would result in V_{out} = 10*(1.0 - 0) = _____ V
- applying the signal to the inverting input with the non-inverting input at ground would result in V_{out} = 10*(0 - 1.0) = _____ V
- applying the signal to the non-inverting input and the inverse of the signal, -1.0 V, to the inverting input would result in V_{out} = 10*(1.0 - -1.0) = _____ V

We often refer to the difference of the two inputs as the differential input voltage, V_{diff}.

$$V_{diff} = V_{in+} - V_{in-}$$

Common Mode Rejection

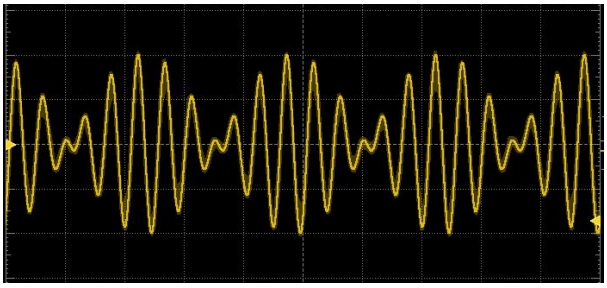
Just as significant as Differential Amplification is something called Common Mode Rejection. This refers to what happens to an identical signal that is applied to both inputs of a differential amplifier. Again, consider our previous example with a gain of 10 and an input signal of 1 V. If the same signal is applied to both inputs, the result is V_{out} = 10*(1.0 - 1.0) = _____ V. In other words, any signal that is "common" to both inputs will be removed from the output! Thus, ***common mode signals*** will be rejected by the differential amplifier. This may seem like a waste, but in reality it is one of the amazing features of the operational amplifier, when used as a differential amplifier. Consider the following two examples:

- In a concert facility, microphone and instrument signal cables are routed from the stage to a soundboard at the back of the room, crossing over AC power cords and under flourescent lights, all of which are operating at 60 Hz, and injecting noise into the signal cables. If the cables are single-ended (signal referenced to ground), the noise on the signal-carrying line will be amplified along with the desired signal, resulting in an annoying hum; however, if the cable is differential, the desired signal will be doubled while the unwanted common mode signal will be eliminated!
- Certain industrial sensors, such as Thermistors and Resistance Temperature Detectors (RTDs) must typically be wired so that the resulting signal has a large DC component and a small useful signal. If an equal DC signal is connected to the other terminal of a differential amplifier, the DC component will be eliminated, leaving only the desired small signal.

The common mode part of a combined signal can be determined as follows:

$V_{in(CM)} = \frac{V_{in+} + V_{in-}}{2}$ in other words, the average of the two inputs.

It seems a little silly to state these two formulas to describe differential and common mode signals. However, when it comes to the kinds of signals that are presented to an amplifier, they are rarely simple voltages or simple true AC signals -- they will be combinations of frequencies and DC components, all of which must be treated separately. For example, a 1.0 V_p 100 Hz signal and a 1.0 V_p 120 Hz signal can't be combined and called a 2.0 V_p signal at either of the frequencies or any combination of the frequencies. Here's what the result looks like:



In places, the amplitude is 2.0 V_p, and in places the amplitude is 0.0 V_p. The frequency is neither 100 Hz not 120 Hz, and there's a repetitive pattern called a "beat frequency" that happens every 50 ms for a "buzzing" sensation at 20 Hz. The main point of this is that we have to deal with each of the components separately in our analysis of a complex signal. Let's do an example.

On a particular differential pair of wires, the following components have been identified. Notice, in this case, that we're allowed to use a negative V_p because it indicates a 180° phase difference between two related signals.

V_+ = 1.2 V_p @ 250 Hz + 0.8 V_p @ 60 Hz + 0.50 V_{DC}

V_- = -1.2 V_p @ 250 Hz + 0.8 V_p @ 60 Hz - 0.20 V_{DC}

1. V_{diff} = _____ V_p @ 250 Hz + _____ V_p @ 60 Hz + _____ V_{DC}
2. V_{CM}= _____ V_p @ 250 Hz + _____ V_p @ 60 Hz + _____ V_{DC}

Notice that equal amplitude components are easy to deal with, but unequal components don't disappear in either the differential term or the common mode term. This leads somewhat indirectly to the next topic.

Common Mode Rejection and Common Mode Rejection Ratio

No amplifier is perfect, and no pair of signal wires will be truly identical; so some portion of the undesirable common mode signal is likely to be transmitted through the amplifier. The common mode gain, therefore, will be

$$A_{v(CM)} = \frac{V_{o(CM)}}{V_{in(CM)}}$$

Hopefully, the common mode gain will be really small. In other words, the common mode component should be significantly attenuated. If the differential gain is really big, then the result will be a pretty clean signal. We quantify this using the ***Common Mode Rejection Ratio***.

$$CMRR = \frac{A_{v(diff)}}{A_{v(CM)}}$$

Since the differential gain should be so much bigger than the common mode gain, we usually state this in decibels as ***Common Mode Rejection***.

$$CMR = 20\ logCMRR$$

3. For a particular differential amplifier, the following values were measured:

- V_+ = 22.5 mV_p @ 3.0 kHz + 3.0 V_{DC}
- V_- = -22.5 mV_p @ 3.0 kHz + 3.0 V_{DC}
- V_{out} = 6.0 V_p @ 3.0 kHz + 20 mV_{DC}

What is the Differential Gain? _____

What is the Common Mode Gain? _____

What is the Common Mode Rejection Ratio? _____

What is the Common Mode Rejection? _____ dB

Notice, in this example, how a tiny differential signal and a large common mode signal, once passed through this amplifier, produce a large version of the differential signal and an almost non-existent common mode component. That's what differential amplification and common mode rejection are all about.

Online Homework System

Assignment Worksheet
5/31/21 - 1:55:56 PM MDT

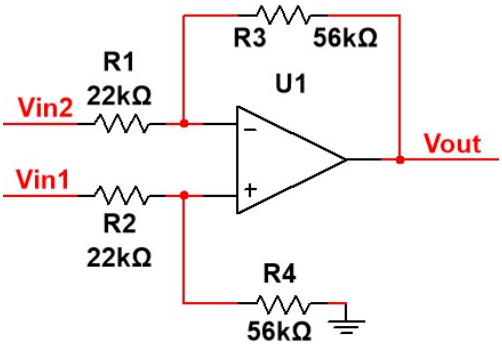
Name: _____ **Class:**

Class #: _____ **Section #:** _____

Instructor: Ross Taylor **Assignment:** SA13 Differential Amplification Activity

Question 1: (10 points)

Use the partially-completed schematic below to answer the questions that follow.



With V_{in1} disabled (i.e. grounded), what would be the gain for signal connected to V_{in2}? (Indicate the correct phase as positive or negative.) _____

With V_{in2} disabled (i.e. grounded), multiply the gain for the V_{in1} signal by the voltage divider at V_{in1} to determine the overall gain for the signal connected at V_{in1}.

_____

If V_{in1} and V_{in2} are both 1 kHz sine waves with amplitudes of 1.00 V_p, what amplitude would you expect to see at the output if the signals were 180º out of phase (differential mode)?

_____ V_p

If V_{in1} and V_{in2} are both 1 kHz sine waves with amplitudes of 1.00 V_p, what amplitude would you expect to see at the output if the signals were in phase (common mode)?

_____ V_p

Schematic

Using Multisim, complete the design circuit for proper wiring using a 741 op amp, as follows:

- Use the actual 741 component
- Power the 741 using +12.0 V and -12.0 V
- Use two Generic Function Generators for the two input signals
- You can "double-click" to terminate the "Vout" wire without connecting it to anything
- Click on any wire to call up its "Properties", provide a "Net Name", and click the box to "Show" the net name so you can label the wires

Circuit

Build the circuit using your schematic diagram. Use your +/-12 V PowerBRICK as the DC power supply.

You will be using the two output waveform channels of your Analog Discovery 2 to generate first a differential signal, then a common mode signal.

Set up your output channels as follows:

- Both channels: 1.0 kHz sine wave, no DC offset, amplitude 1.00 V_p
- Select "Synchronized" to lock the phase of the two channels
- Set Channel 1 Phase to 0º and Channel 2 Phase to 180º. This makes the signals differential.

Connect the two signals from the function generator to V_{in1} and V_{in2}.

Use the two channels of your oscilloscope to verify that these two signals are equal but opposite to each other.

Move oscilloscope channel 2 to the output of your amplifier, and determine the Differential Gain, using the formula provided in class.

_____

Now set both function generator output phases to 0º (common mode). Use the two channels of your scope to verify that these signals are identical, and in the same phase.

Use oscilloscope channel 2 to observe the output of your amplifier. Adjust the vertical attenuation for the output channel to make the signal as big as possible on screen.

Measure the output signal voltage, and determine the Common Mode Gain. It should be considerably less than 1, but will vary from amplifier to amplifier. If your circuit and signals are correct, your answer should fall within the fairly generous range allowed for this question.

_____

Determine the common mode rejection, in dB.

_____ dB

Provide the following for grading:

- a screenshot of your completed schematic for a grade out of four Document Upload (Direct)
- a picture of your working circuit for a grade out of two Document Upload (Direct)
- a screenshot of your oscilloscope showing one of the inputs and the output when the input signals are ***180° out of phase*** for a grade out of two Document Upload (Direct)

Online Homework System

Assignment Worksheet
6/7/22 - 1:28:49 PM MDT

Name: _____ **Class:**

Class #: _____ **Section #:** _____

Instructor: Ross Taylor **Assignment:** SA14 Op Amp Controlled Power Amplifier Activity

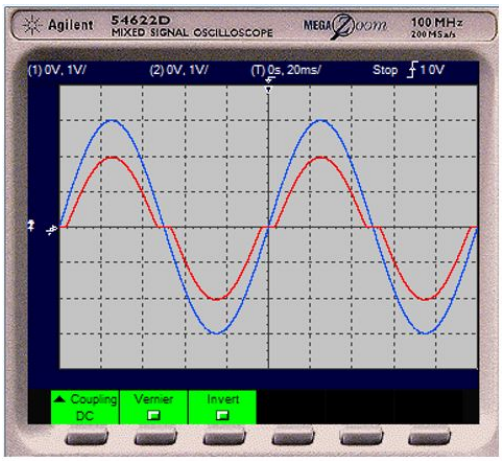
Question 1: (25 points)

This exercise is completely auto-graded. screenshots have been included to help you determine if your circuit and equipment setup are correct. Please ensure you are seeing the correct results before you proceed.

Problem: Amplifying Power

One of the issues with op amps is that they aren't capable of driving a lot of current, and therefore cannot be used as power amplifiers.

In the past, the solution has been to use one of two push-pull BJT power amplifier configurations, both of which have their issues. The true "Class B" amplifier is simple, powerful, and has nearly ideal amplifier characteristics -- high input impedance and low output impedance. However, it suffers from "crossover distortion", which looks like this:



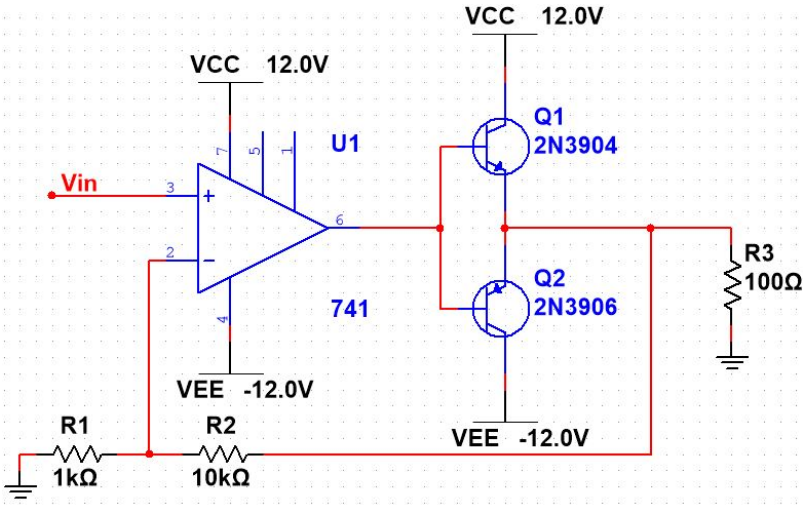
The alternative circuit, "Class AB", adds biasing diodes to the power transistors to overcome crossover distortion, but it has its own issues: its input impedance isn't as high as the Class B amplifier's, and unless the amplifier is designed very carefully, it has a tendency towards thermal runaway, a condition that will destroy the amplifier and could potentially be a fire hazard.

In addition, neither the Class B nor Class AB amplifiers have any voltage gain -- the amplitude of the signal remains the same, but the current is dramatically increased, resulting in power gain, since $P = IV$. Consequently, both of these amplifiers must be preceded by "small signal" amplifiers that can increase the voltage but not the current.

An interesting hybrid that crosses an op amp with a Class B amplifier returns us to nearly ideal conditions. The input impedance can be very high, the output impedance is very low, and classical crossover distortion isn't an issue. In addition, this hybrid amplifier can amplify both the voltage and the current, resulting in a very large power gain. However, there is a new form of distortion that's related to crossover distortion. Fortunately, this form of distortion can be minimized through the use of high-frequency op amps.

Op Amp/Transistor Voltage and Current Amplifier

The amplifier in the schematic diagram below is just one of a number of possible hybrid solutions. We'll analyze this amplifier using the questions that follow.



1. Considering the arrangement of the input and the feedback network, this amplifier is _____
2. Considering where V_{in} is connected, the input impedance of this amplifier would be _____
3. Given that there are no current-limiting resistors between the transistors and the load resistor (R_3), we can probably assume that the output impedance of this amplifier is _____
4. Considering that the op amp will attempt to maintain zero volts (virtual short) between its differential inputs, using the feedback resistors we can predict a voltage gain for this amplifier of _____ _____
5. If V_{out} = 8.25 V_p, what is that in RMS for power calculations? _____ V_{RMS}
6. Given that the load resistor is 100 Ω, how much power will it dissipate if V_{out} is 8.25 V_p? _____ mW
7. What is the RMS current through the load? _____ mA_{RMS}
8. Consider the specification sheet (https://www.ti.com/lit/ds/symlink/lm741.pdf) for the 741 op amp. Is it capable of producing the required current for the situation above? _____
9. Consider the specification sheet (https://www.mouser.com/datasheet/2/149/2N3904-82270.pdf) for the 2N3904 transistor, which has fairly similar characteristics to its complement, the 2N3906. Is this transistor capable of handling half of the required current? _____
10. When the output signal is positive, how much higher must the output voltage of the op amp be, to activate the 2N3904? _____ V
11. When the output signal is negative, how much lower must the output voltage of the op amp be, to activate the 2N3906? _____ V
12. When the output signal crosses zero, how much does the output of the op amp suddenly need to change? _____ V
13. If the op amp's Slew Rate (maximum rate of change of voltage) is 0.5 V/μs, how long will it take to make the required change when the output signal crosses zero volts? _____ μs

The problem we've just investigated is that, as the op amp attempts to change from positive to negative and *vice versa*, the output signal will experience a slight glitch, which will distort the output signal. Since the transition time is constant, it will have a much bigger effect on high frequency signals than it does on low frequency signals.

14. What percentage of a 100 Hz signal's period is 3 μs? _____ %
15. What percentage of a 20 kHz signal's period is 3 μs? _____ %

Build the Circuit

Using your breadboard, a +/-12 V power supply, a signal generator, and an oscilloscope, build and test this circuit.

- Be very careful with the orientation of the two transistors -- the two Emitters are connected together
- Be very careful with your choice of resistors -- 100 Ω has a brown multiplier band
- Set up signal generator Ch1 as follows:
  - Sine Wave
  - 750 mV_p
  - No offset
  - 100 Hz
- Use oscilloscope Ch1 to observe V_{in}
- Use oscilloscope Ch2 to observe V_L, the voltage across the load resistor

Analyze the Circuit

At this point, you should be seeing something like this on your oscilloscope. Notice the different vertical scales for the two channels.

Make the following measurements, using the oscilloscope measurement menu.

- For the amplitudes, use Amplitude, which is a smoothed version of peak to peak, and divide by two to get V_p
- For V_s, record the voltage you set the signal generator to produce
- For V_{oc}, disconnect the load resistor and measure the output voltage ***Caution: this resistor could be hot enough to burn you -- this is a power amplifier!***
- For V_o, measure the output with the load resistor connected

V_s, mV_p	V_{in}, mV_p	V_{oc}, V_p	V_o, V_p
_____	_____	_____	_____

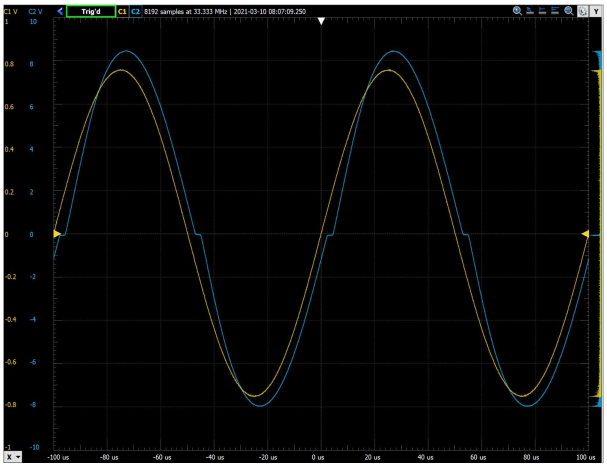
Using "black box" empirical calculations, determine the following:

r_{in}	A_{vo}	A_v	r_{out}
_____	_____	_____	_____

Temporarily, move oscilloscope Channel 2 to the Bases of the two transistors to see the transition made by the op amp. You should see something like the following:

Move Channel 2 back to the output.

Set the frequency to 10 kHz, with the other settings unchanged. Notice the glitch as the output signal crosses the zero line, caused by the time it takes for the op amp to switch from -0.7 V to +0.7 V. You should see something like the following:



Note that, unlike the crossover distortion generated by the Class B amplifier (see first image in this exercise), the overall amplitude of the signal is not decreased by 1.4 V -- there's just a glitch at the zero crossing point. This is, therefore, a much less significant form of distortion.

How could this glitch be minimized? _____

Online Homework System

Assignment Worksheet
5/20/22 - 9:32:23 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Differential Offset Compensation

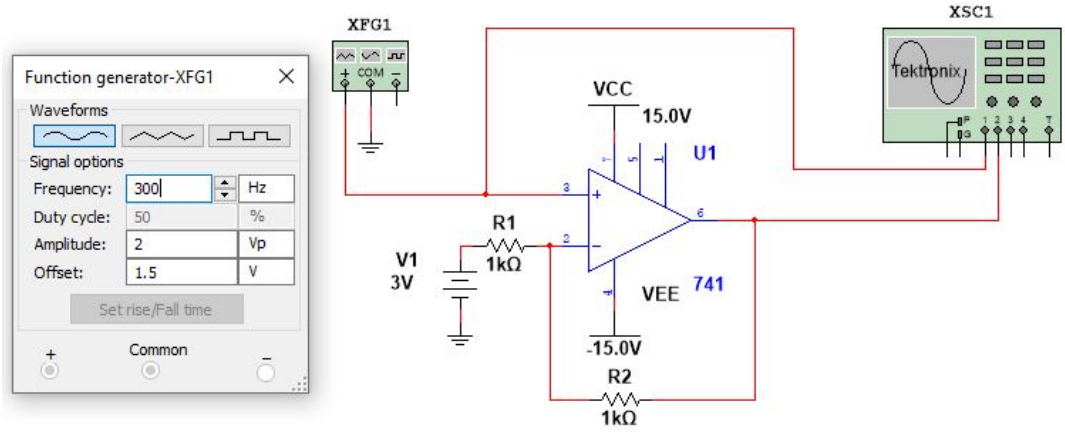
Question 1: (1 point)

Differential Offset Compensation

So far, we've seen that having differential inputs on an op amp allow us to create either inverting or non-inverting single-input amplifiers, and to build differential amplifiers that can remove common mode signals while amplifying desired differential signals.

Somewhat related to that last topic is the addition or removal of a DC component in a complex signal, as we will investigate in this lesson. We'll start with a circuit that demonstrates the process, then we'll evaluate it to see how it works.

Build the following circuit in Multisim, and answer the questions that follow. Pay close attention to the settings of the function generator, the power supplies, and the DC offset voltage (V_1). Set up the Tektronix oscilloscope to display the input and output signals adequately.



1. What is the amplitude of the output signal? _____ V_{p-p} or _____ V_p
2. What is the DC component of the output signal? _____ V_{DC}

If all went well, you should have discovered that, even though the input signal has a large DC offset, the output signal does not. Let's analyze the circuit to understand why.

3. Before you do, though, prove to yourself that the DC removal is deliberate by changing the function generator offset to 2.5 V. What is the DC offset in the output signal now? _____ V_{DC}

We'll use superposition. To do this, we first determine the theoretical outputs generated by the two inputs independently, then we add the results together.

4. First, let's disable the function generator by shorting it to ground. What gain does the DC voltage, V_1, see? We'll call this A_{v1}._____
5. Use this gain and the value of V_1 to determine the DC component at the output generated from V_1. _____ V_{DC}
6. Second, let's disable V_1 by shorting it to ground. Being careful to determine the op amp configuration seen by the function generator signal, determine the associated gain. We'll call this A_{v2}._____
7. Multiply the DC offset from the function generator by the gain to determine the DC component at the output from this signal. _____ V_{DC}
8. Add the two DC components together, to show why the DC in the output signal has been effectively removed. _____ V_{DC}
9. Multiply the AC component by the gain seen by the function generator to determine the resulting amplitude of the signal. _____ V_p

We can write what is called a Transfer Function for this circuit by combining the parts we analyzed using superposition, then simplifying.

$V_{out} = A_{v2}*V_{in} + A_{v1}*V_1$

$V_{out} = 2V_{in} - 3$

This fits into the equation of a line, y=mx + b

where

$y = V_{out}$

m = Av

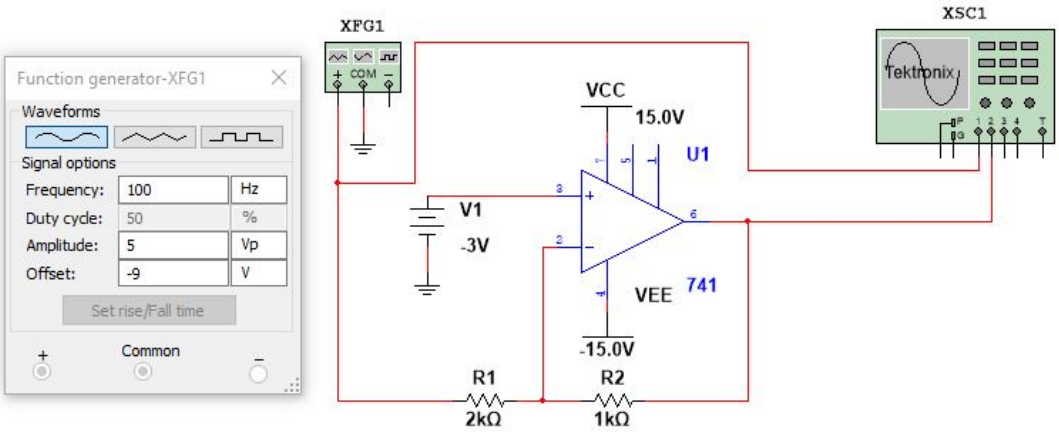
$x = V_{in}$

$b = V_{offset}$

Question 2: (1 point)

In the last example, a DC offset was added at the inverting terminal. The same can be done with the non-inverting terminal, as seen in the following example.

Using Multisim, build the following circuit and analyze it as follows.



The input signal from the function generator is all negative, so you may have to adjust the scope settings to see it. Try to leave the ground marker (little yellow arrow) in the middle of the screen.

1. What is the amplitude of the output signal? _____ V_{p-p} or _____ V_p
2. What is the DC component of the output signal? _____ V_{DC}

Again, you should have discovered that the huge DC offset in the original signal has been effectively eliminated by this circuit.

Use superposition to determine the following characteristics of this circuit:

3. Gain seen by the DC input, V_1: _____
4. DC offset in the output from V_1: _____
5. Gain seen by the function generator input: _____
6. Transfer function: V_{out} = _____ x V_{in} - _____
7. By entering the DC component of V_{in} into your transfer function, you should be able to prove that the output offset is what you observed in Multisim: _____ V_{DC}

Online Homework System

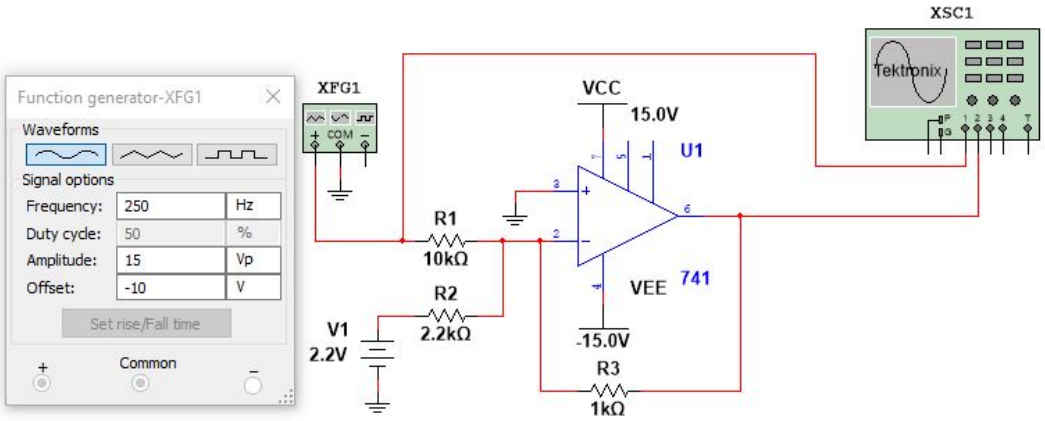
Assignment Worksheet
5/20/22 - 9:33:53 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Summing Amplifier

Question 1: (1 point)

A very common circuit for combining signals is the Summing Amplifier, in which the various signals are combined at a single point, which must be a Virtual Ground in order to work properly. Since we've been investigating ways to remove DC from an incoming signal, we'll begin there, but there's much more that can be done with summing amplifiers.

Build the following circuit in Multisim, and analyze it as follows.



What is the amplitude of the output signal? _____ V_{p-p} or _____ V_p

What is the DC offset of the output signal? _____ V_{DC}

Prove that the DC removal was intentional by changing V1 to 3.0 V. What is the DC offset in the output now? _____ mV_{DC}

Now, let's analyze the circuit to see why the DC was effectively eliminated.

By disabling V_1, determine the gain seen by the function generator circuit. _____

By disabling the function generator, determine the offset in the output generated by V_1. _____ V_{DC}

Insert these values into the following transfer function:

V_{out} =_____ x V_{in} - _____

Now, by entering the two components of the input signal, determine the following:

V_{out} = _____ V_p +_____ V_{DC}

Also note that the output signal is inverted with respect to the input signal.

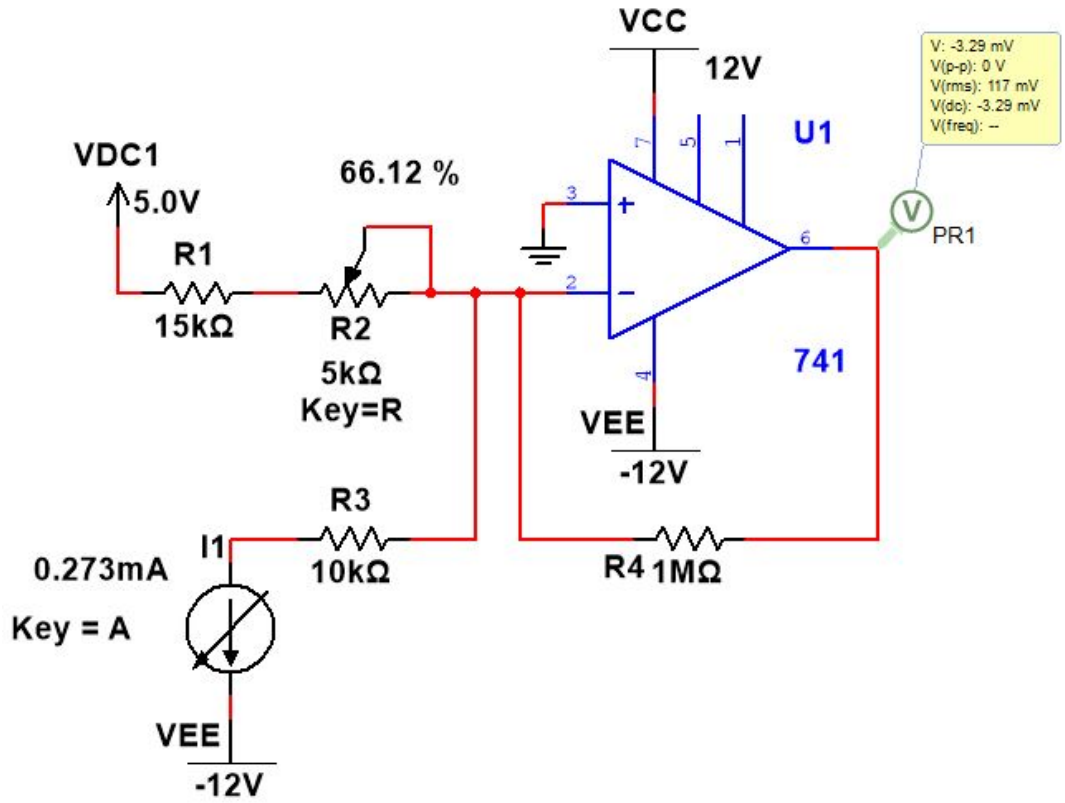
Question 2: (1 point)

Some devices operate as current sources, rather than as voltage sources. One such is the AD590 or AD592 temperature sensor, which produces a signal of 1 μA per Kelvin degree, K. The Kelvin scale has the same step size as the Celsius scale, but it starts at 0 K for absolute zero, which is approximately -273ºC. Using Multisim, build the circuit below.

V_{DC1} is "V_REF1" from "Sources" -> "SIGNAL_VOLTAGE_SOURCES" and I_1 is "DC_INTERACTIVE_CURRENT" from "Sources" -> "SIGNAL_CURRENT_SOURCES", and will simulate the temperature sensor.

Edit the potentiometer to have an "Increment" of 0.01%.

Edit I_1 to have a "Maximum value" of 500uA and an "Increment" of 0.2%.



Set the current source to 273 μA, then adjust the potentiometer until the output is a close as possible to 0 V.

Now, vary the current to the values indicated below, and record, to the nearest whole number, the output voltage observed.

Input Current, μA	Output Voltage, V
268	_____
269	_____
270	_____
271	_____
272	_____
273	_____
274	_____
275	_____
276	_____
277	_____
278	_____

What do these numbers best represent, in the real world?

(a) Temperature in Kelvin degrees

(b) Temperature in Celsius degrees

(c) Volts DC

Now, to analyze this circuit. First, disable V_{DC1} by shorting it to ground. From this half of the circuit, determine the relationship between V_{out} and I_1, which we will call I_{in}: V_{out} = _____ x I_{in}

Using this relationship, what would the output voltage be at a temperature of 0ºC? _____ V

Clearly, this is much too large a voltage to be produced by a 741 op amp, which can only be powered from -30 V to +30 V, and the output voltage is limited to one or two volts less than the power supply voltage.

Assuming that the combined resistance of R_1 and R_2 is 18.306 kΩ, determine the current supplied from V_{DC1}. _____ μA

Use this current to determine the DC offset for the output that is provided by V_{DC1} when I_1 is disabled. _____ V

Clearly, this is also much too large a voltage for the 741 op amp to produce. However, combined with the other part of the output signal, the result is within range.

Combine your results into a transfer function:

V_{out} = _____ x I_{in} - _____

Verify that this transfer function produces the results you recorded in the table above. By injecting a current to compensate for the sensor current at 0ºC, we have converted the sensor's current to voltages that directly represent the temperature in Celsius degrees.

If we were using this circuit as a thermometer, we would display the voltage at the output as temperature in Celsius degrees. This is referred to as an "Inverse Transfer Function", where the output of our circuit is mathematically manipulated to display the measured quantity in its native unit of measure. Although ITFs are usually more complex, ours looks like this:

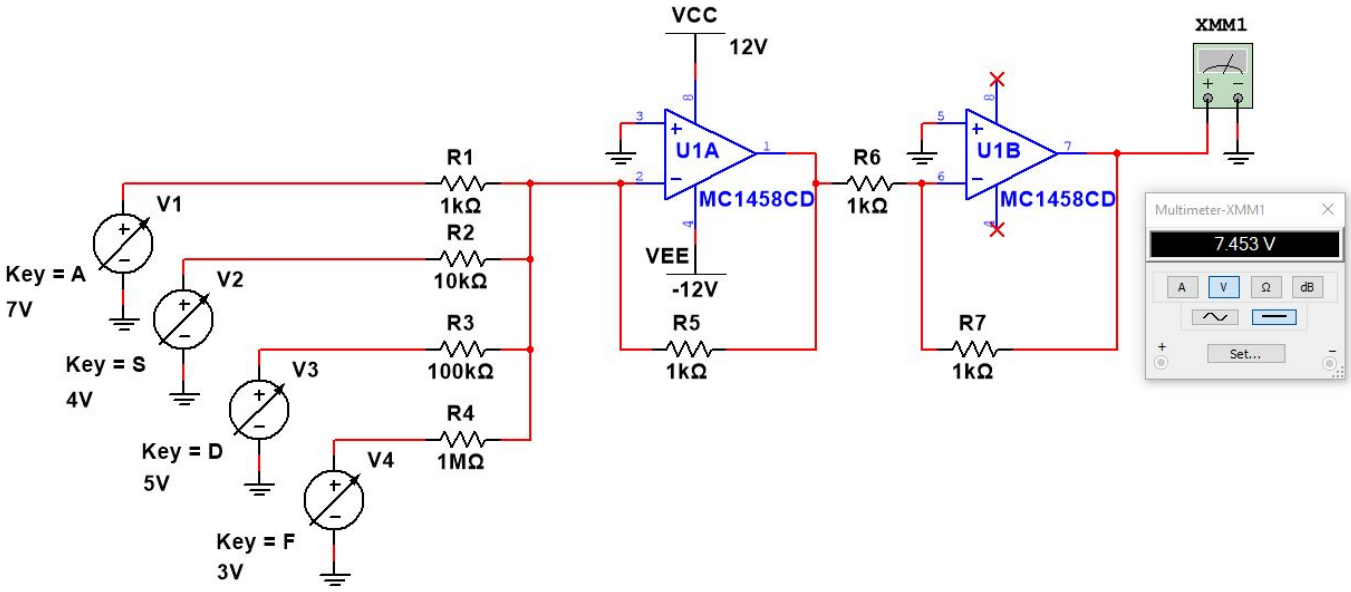
T = V_{out}, ºC

Question 3: (1 point)

The previous example demonstrated that the output from a summing amplifier is based upon the sum of the currents into the summing point. This next example will help to formalize the theory behind the summing amplifier a bit further.

Using Multisim, build the following circuit.

V_1, V_2, V_3, and V_4 are all "Sources" -> "SIGNAL_VOLTAGE_SOURCES" -> "DC_INTERACTIVE_VOLTAGE". Set these to a Maximum of 10 V and and Increment of 10%. This makes the step size suitable; however, you won't want to go over 9 V on any of the inputs.



Set the input voltages to the values in the following table, and record the associated output voltages to the nearest millivolt.

V_1, V	V_2, V	V_3, V	V_4, V	V_{out}, V
7	4	5	3	_____
1	9	2	0	_____
9	9	9	9	_____
2	5	7	6	_____

0	0	0	0	_____

By comparing the input voltage combinations to the output voltages, it should be clear to you that the outputs represent the decimal-weighted inputs in millivolts. Since we already know about Inverse Transfer Functions, let's write one for this circuit that gives us the whole number represented by the output voltage:

N = _____ x V_{out}

Now for the circuit analysis:

What is the gain of the second amplifier, U1B? _____

This amplifier is used to:

(a) increase the magnitude of the signal

(b) decrease the magnitude of the signal

(c) invert the signal presented to it

For the first example, as shown in the schematic, determine the current supplied by each of the input voltage sources in microamps.

From V_1, I_1 = _____ μA

From V_2, I_2 = _____ μA

From V_3, I_3 = _____ μA

From V_4, I_4 = _____ μA

What is the total incoming current? _____ μA

Since none of this current can enter the high-impedance input of the op amp, all of it must go through the feedback resistor. From this, determine the voltage seen at the output of the first amplifier, U1A. _____ V

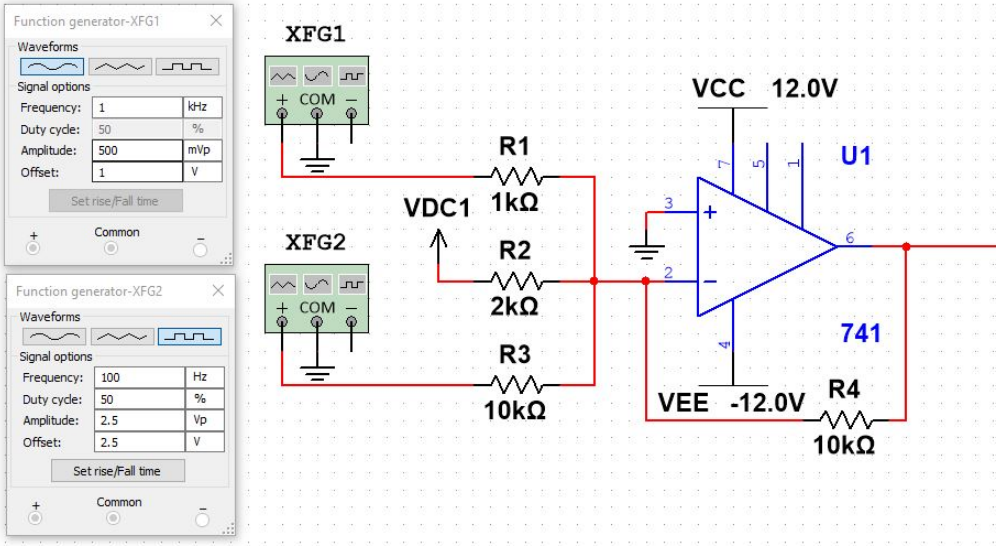
Here's the theory behind this amplifier configuration.

1. Since the inverting input is a Virtual Ground (0 V), current from each of the sources flows through each input resistor to "ground", and therefore does not affect the reference of any of the other input sources. In essence, the Virtual Ground Summing Point isolates all the input sources from each other.
2. There is only one available path for current entering the summing point: Through the feedback resistor. Therefore, the sum of the incoming currents must flow through this one path.
3. The output voltage is therefore the inverted product of the feedback resistor value and the sum of the currents.

In the form of an equation, this can be shown, as the general formula for all summing amplifiers, as

$$V_{out} = -R_f \cdot \left(\frac{V_{in1}}{R_{i1}} + \frac{V_{in2}}{R_{i2}} + \frac{V_{in3}}{R_{i3}} + \ldots \right)$$

Here's a worked example in which the DC offsets generated by two inputs needs to be cancelled using a third input.



In this case, both of the function generators contain DC offsets, which will add together in the output signal.

The DC component in the output from XFG1 will be

$$1.0\ VDC \cdot \left(-\frac{10\ k\Omega}{1\ k\Omega}\right) = -10\ VDC$$

The DC component in the output from XFG2 will be

$$2.5\ VDC \cdot \left(-\frac{10\ k\Omega}{10\ k\Omega}\right) = -2.5\ VDC$$

The combined DC voltage at the outputs from these two supplies will be -12.5 VDC.

If the DC in the output component is to be cancelled by VDC1, the DC component at the output from this supply would have to be +12.5 VDC. Consequently, the input voltage would be calculated as follows:

$$VDC1 = \frac{12.5\ VDC}{\left(-\frac{10\ k\Omega}{2\ k\Omega}\right)} = -2.5\ VDC$$

As a quick check, we could determine the combined DC output voltage using the general formula:

$$VDC_{out} = -10\ k\Omega \cdot \left(\frac{1\ VDC}{1\ k\Omega} + \frac{-2.5\ VDC}{2\ k\Omega} + \frac{2.5\ VDC}{10\ k\Omega}\right) = 0\ VDC$$

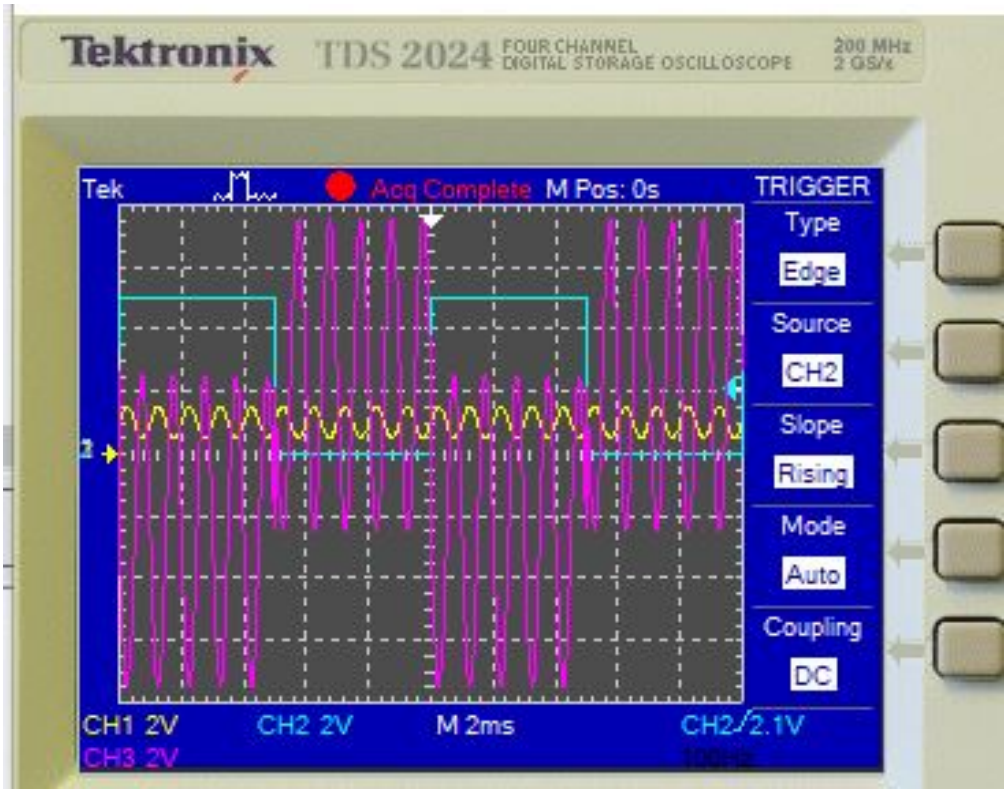
While we're at it, we could determine that the amplitude of the sine wave from XFG1 would be

$$v_{out1} = 500\ mVp \cdot \left(-\frac{10\ k\Omega}{1\ k\Omega}\right) = 5\ Vp,\ inverted$$

The amplitude of the square wave from XFG2 would be

$$v_{out2} = 2.5\ Vp \cdot \left(-\frac{10\ k\Omega}{10\ k\Omega}\right) = 2.5\ Vp,\ inverted$$

The oscilloscope display below, with all channels set to 2 V/div, shows the expected results:



The input signal from XFG1 shows a DC offset of +1 VDC and an amplitude of 1.0 $V_{p\text{-}p}$, or the expected 500 mV_p

At the output, this signal covers five divisions, or 10 $V_{p\text{-}p}$ (i.e. 5.0 V_p), matching the expected gain of 10; also note that when the input signal is at a maximum, the output signal is negative, matching the prediction that the gain for the XFG1 signal is inverted; so the gain is actually -10.

The input signal from XFG2 shows an average voltage of +2.5 VDC and a "peak to peak" amplitude of 5.0 $V_{p\text{-}p}$.

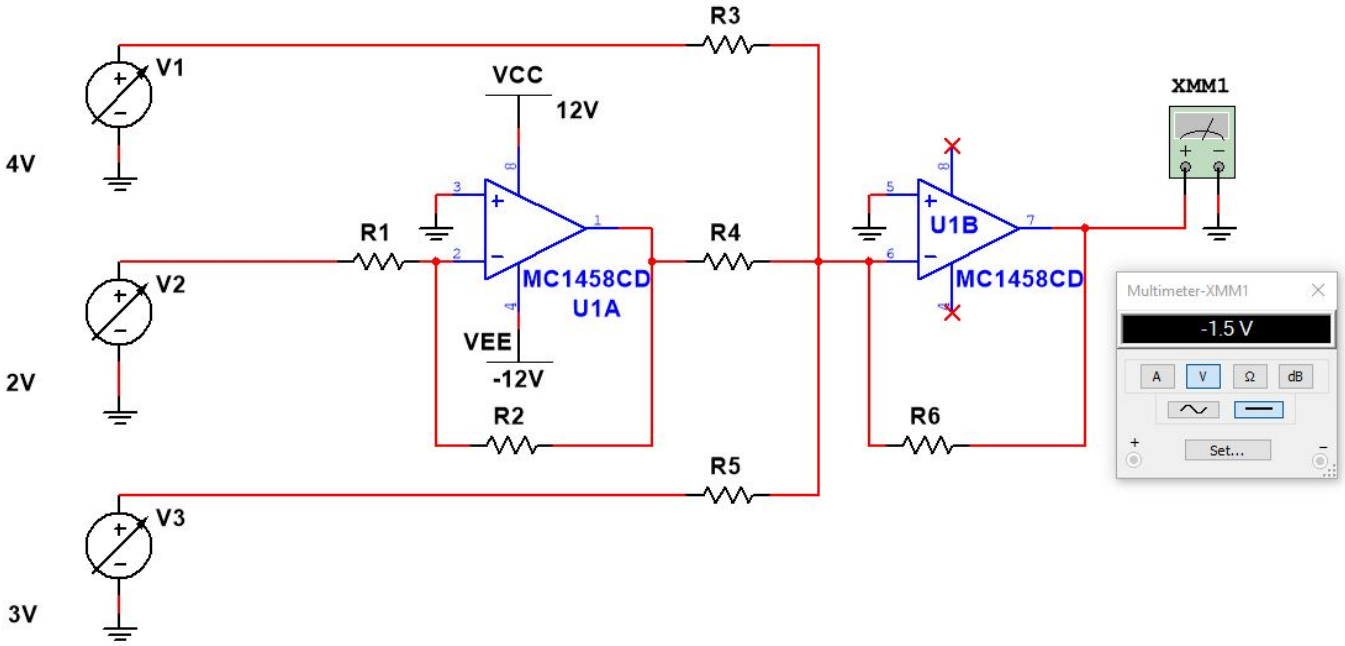
Its contribution to the output signal can be determined from the averages of the upper and lower "bursts" of the sine wave. The upper part of the signal is centered around +2.5 V, and the lower part is centered around -2.5 V; so its amplitude is 5.0 $V_{p\text{-}p}$ or 2.5 V_p, indicating a gain of 1.0 as predicted from the resistors. Also, note that when the input is at a maximum, the lower burst of sine wave appears, and when the input is at a minimum the upper burst of sine wave appears, so this component is also inverted. Hence, the gain for the XFG2 signal is -1.0.

Question 4: (1 point)

Here's a chance for you to do part of a summing amplifier design. This example is one of many "analog computer" circuits which has been designed to do a specific calculation based upon the inputs. Your task is to determine resistor values to generate the expected output. The mathematical expression is intended to be

$w = -x + 2\ y - \frac{z}{2}$

You can only use 10 kΩ and 20 kΩ resistors.



From the given input voltages and the resulting output, determine which voltage supply matches the variables in the expression:

_____

Now determine the values of each resistor:

R1 =

(a) 10 kΩ

(b) 20 kΩ

R2 =

(a) 10 kΩ

(b) 20 kΩ

R3 =

(a) 10 kΩ

(b) 20 kΩ

R4 =

(a) 10 kΩ

(b) 20 kΩ

R5 =

(a) 10 kΩ

(b) 20 kΩ

R6 =

(a) 10 kΩ

(b) 20 kΩ

Build the circuit with your chosen resistor values. Set up the three "DC_INTERACTIVE_VOLTAGE" sources with a Maximum of 5 V, a Minimum of -5 V, an Increment of 10%, and a Key matching the input variable (x, y, or z).

Verify that the circuit is working properly by filling in the following table. Round the output voltages to the nearest 0.1 V. The "Calculated" value is what you expect to get, determined using a calculator.

X, V	Y, V	Z, V	Vout, V	Calculated
4	2	3	_____	_____
-1	3	2	_____	_____
2	-2	-1	_____	_____

Online Homework System

Assignment Worksheet
3/20/23 - 12:31:21 PM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Project 4 Summing Amplifier

Question 1: (50 points)

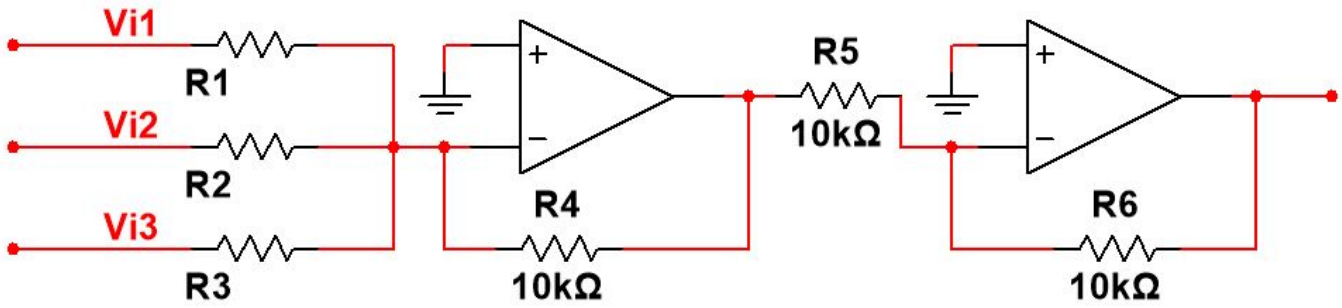
Project 4 Preparation and Simulation: Summing Amplifier

This Project must be submitted for grading at the time specified by your instructor. You will be given some class time to work on it, and will be expected to do other work on your own time.
As this is a more formal assessment than the lab activities, your instructor's involvement will be limited to clarification of the requirements and simple feedback on your work. This assessment is intended to show that you have a good grasp on the associated course outcomes, so please limit your interactions with others to points of clarification or improvement of your understanding of the material rather than working together to arrive at solutions.
The first part of this assessment will involve preparatory work and predictions regarding a circuit similar to what you will build later, culminating in a simulation to demonstrate its operation. The second part will involve building and testing a real circuit, and will be graded primarily upon your technical skills of cuircuit building and use of test equipment.

Grading breakdown:
30% -- Preparatory Work and Predictions
20% -- Simulation
50% -- Circuit Building and Testing

Note: Once you submit this first page and move on to the next, you will not be able to return to it! Instead of moving on to the next question, you can "Save and Close" if you intend to return later.
The "Printable Version" is also available for you to work through before submitting your answers.
You are allowed one "How Did I Do?" to check your answers to this part of the project.

The following is a partial schematic of the circuit you will be building.



Our goal is to build a circuit with the following Transfer Function:

$$Vo = 0.213\ V_{i1} + V_{i2} + 3.03\ V_{i3}$$

Since the circuit above is incomplete, you will need to prepare a complete schematic before you can properly build the real circuit. In Multisim, start by using a single MC1458 IC for the op amps. Use +12 V and -12 V for power. Add the rest of the components shown, and determine the resistor values as you answer the following questions.

V_{i1} will be -12 VDC, connected directly to the -12 V supply. Show this on your schematic, and pick a 10% resistor value to provide the appropriate gain for this part of the transfer function. R_1=_____ kΩ

V_{i2} will be a 1.00 kHz "unipolar" pulse with a LOW value of 0 and a HIGH value of 2.6 V. Pick a resistor that will provide the appropriate gain for this part of the transfer function. R_2=_____ kΩ

What is the expected peak to peak output of the part of the signal generated by V_{i2}? (Be careful! Maybe sketch the input signal to help you with this one.) _____ V_{p-p}

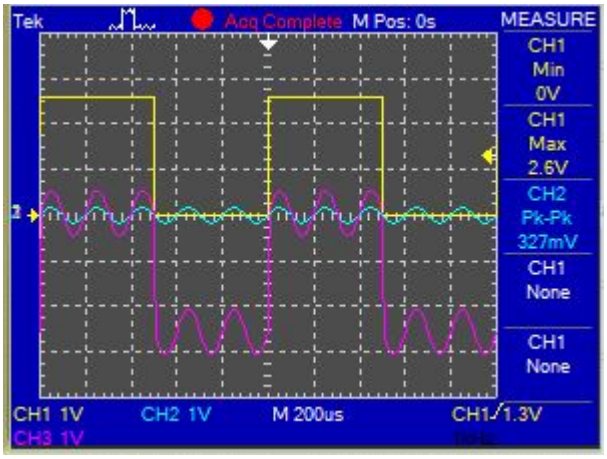
Since the pulse is not centred around zero volts, it will have a DC, or average, component. Determine the DC offset in this unipolar pulse. (Again, you may want to sketch the expected output signal to help you.) _____ V_{DC}

V_{i3} will be a 5001 Hz true AC sinewave (i.e. no DC). We want the output amplitude to be 1.0 V_{p-p}. Given the gain required, what should the function generator amplitude be, this time in volts peak? V_{i3}=_____ V_p

Determine the resistor required to achieve the appropriate gain for this part of the transfer function. R_3 = _____ kΩ

Add this resistor and a second function generator, set to the values indicated above, to your schematic in Multisim.

Using a Tektronix four-channel oscilloscope, check to see if your circuit works in the Multisim simulator. You should see something like the violet trace in the following image, if you set the amplitude of V_{i3} to the value you calculated above. (The other traces shown are V_{i2} and V_{i3}, which you will likely also want to display to help you verify that everything is correct. The sine wave component should scoll slowly along the square wave component because the two signals are deliberately not synchronized.)



For four marks, submit a screenshot (.jpg or .png) of your Multisim schematic here, with an oscilloscope display visible, for your instructor to grade. Do not use any spaces or special characters in the filename, but personalize it for easy identification. Document Upload (Direct)

You have now finished the Preparation and Simulation components of this project. Save your work, then move on to the next question (Build and Test). Once you move on, you will not be able to access this part of the project again! yet!

Question 2: (50 points)

Project 4 Build and Test

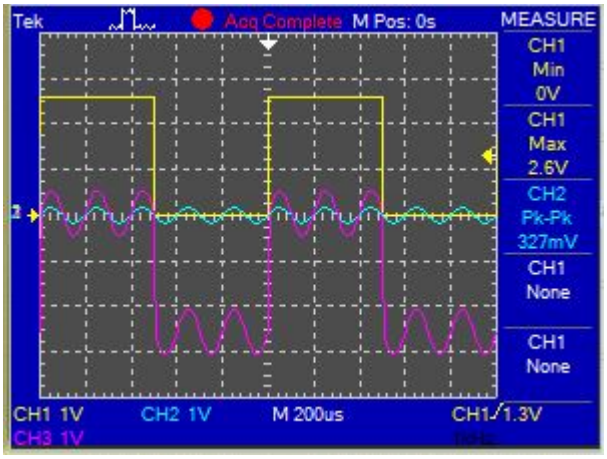
Build the circuit from your completed schematic diagram from the Preparation and Simulation component of this project.

Connect the three input voltages as specified in the Pre-Lab:

- V_{i1} is to be connected to the -12 VDC supply
- V_{i2} is to be a 1.00 kHz unipolar pulse switching from 0.0 V to +2.6 V.
- V_{i3} is to be a 5001 Hz sine wave small enough to generate an output signal of 1.0 V_{p-p}. You can initially set the amplitude to what you calculated in the Pre-Lab, but should adjust it if this particular output component isn't quite 1.0 V_{p-p}.

View V_{i2} on Channel 1 and the output signal on Channel 2 of your oscilloscope.

If all is well, you should have a display similar to what's shown below, if the two channels are set to 1V/div. (In this picture, V_{i3} is also displayed, but with your two channel oscilloscope, you won't be able to do that. If you want, you can observe V_{i3} temporarily to see if it matches what's shown in this picture.)



For three marks, ask your instructor to grade your circuit and the oscilloscope setup. _____

Measure the DC offset (mean) of the output signal. V_{ave} = _____ V_{DC}

Temporarily disconnect V_{i2} and V_{i3}. How much of the DC in the output is from Vi1? _____ V_{DC}

Temporarily disconnect V_{i1} and V_{i3}, but reconnect V_{i2}. How much of the DC in the output is from V_{i2}? _____ V_{DC}

Temporarily disconnect V_{i1} and V_{i2}, but reconnect V_{i3}. What is the amplitude of the output generated by this signal, in peak to peak volts? _____ V_{p-p}

Reconnect all the inputs. Temporarily change Channel 2 to AC Coupling. What is the average voltage of the output now? _____ V_{DC}

Add a horizontal cursor, and assign it to Channel 2. Now, add another horizontal cursor and assign it to Channel 2, as well. If the oscilloscope doesn't automatically display the difference ("delta") between the cursors, either adjust the settings or manually record the measurements you are about to make. With oscilloscope Channel 2 AC Coupled, put Cursor 1 at the very top of the output signal. Record the voltage here. _____ V

Now DC-Couple Channel 2, and put the second Cursor at the top of the output signal in this configuration. Don't move the first cursor. What is the difference ("delta") between these two signals? (To get the polarity correct, consider which way the signal moved when you DC-Coupled the channel.) _____ V

Hopefully, in these last two steps, you have shown that AC Coupling of the oscilloscope simply blocks the DC component of a compound signal, allowing only the AC components to be viewed.

You have now completed this project. Once you submit your work, you will not be able to return to any of these questions!

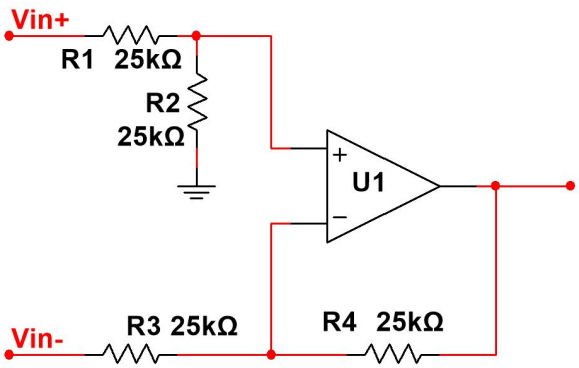
Online Homework System

Assignment Worksheet
5/20/22 - 9:34:32 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Instrumentation Amplifiers

Question 1: (1 point)

In a previous self-assessment, you used a differential amplifier to investigate differential amplification and common mode rejection. Here it is again, drawn in a slightly different orientation, and with the same resistor value used throughout rather than the two different resistor values in the self-assessment. This configuration is the heart of a special amplifier configuration used frequently as an interface between "real world" parameters like temperature, pressure, force, brightness, etc. and electronic circuits in measurement instruments -- hence the name Instrumentation Amplifier.



Using superposition to disable V_{in+}, determine the gain for V_{in-}. _____

Using superposition to disable V_{in-}, determine the gain for the non-inverting input. _____

Notice that there's a voltage divider between V_{in+} and the non-inverting input. How much of V_{in+} appears at the non-inverting input? _____

Multiply the output from the voltage divider by the gain at the non-inverting input to determine the overall gain for V_{in+}. _____

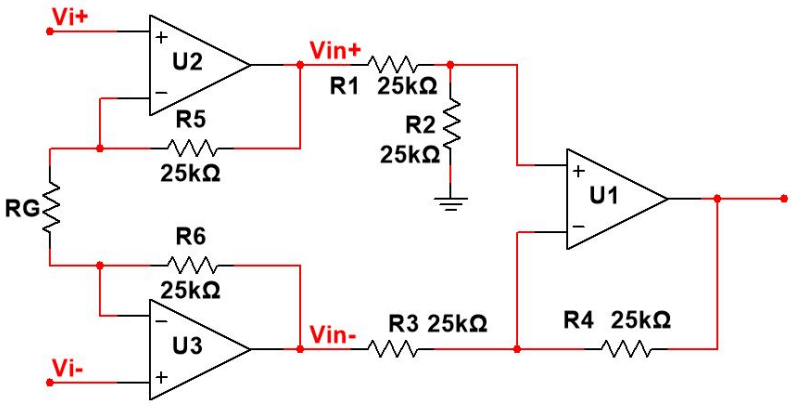
You should have determined that the magnitude of the gains for Vin- and Vin+ are the same, and only the polarity is different. Consequently, a Common Mode signal would be cancelled but a differential signal would be amplified, as shown in the self-assessment.

This amplifier, as shown, has limitations: first, it has no overall gain. But, more significantly, its input impedances are not ideal, and are not the same for the two inputs.

What is the input impedance seen by V_{in-}? _____ kΩ

What is the input impedance seen by V_{in+} (i.e. what resistance exists between Vin+ and ground)? _____ kΩ

The solution to the two issues -- fixed unity gain and poor, unmatched input impedances -- was brilliant. Here it is.



Notice, first of all, that the input impedance problem has been addressed -- both signals are connected directly to high-impedance inputs, so there will be no signal loss at either input.

But what about the gain issue? Let's investigate R_G, the gain setting resistor. Using the concept of the virtual short, the voltage at the top of this resistor is V_{i+} and the voltage at the bottom of the resistor is V_{i-}. Therefore, we can say that the current through R_G is

$$I_{R_G} = \frac{(V_{i+} - V_{i-})}{R_G}$$

Since all of the current through RG must flow between the nodes labelled Vin+ amd Vin-, we can say that

$$V_{in+} - V_{in-} = I_{R_G}\,(2\ R + R_G)$$

Substituting the expression for IRG into this expression, we get

$$V_{in+} - V_{in-} = \frac{(V_{i+} - V_{i-})}{R_G}\,(2\ R + R_G)$$

Now, since the gains for the two differential amplifier inputs are both unity,

$$V_{out} = V_{in+} - V_{in-}$$

So, with a bit of rearranging (check this for yourself), we get

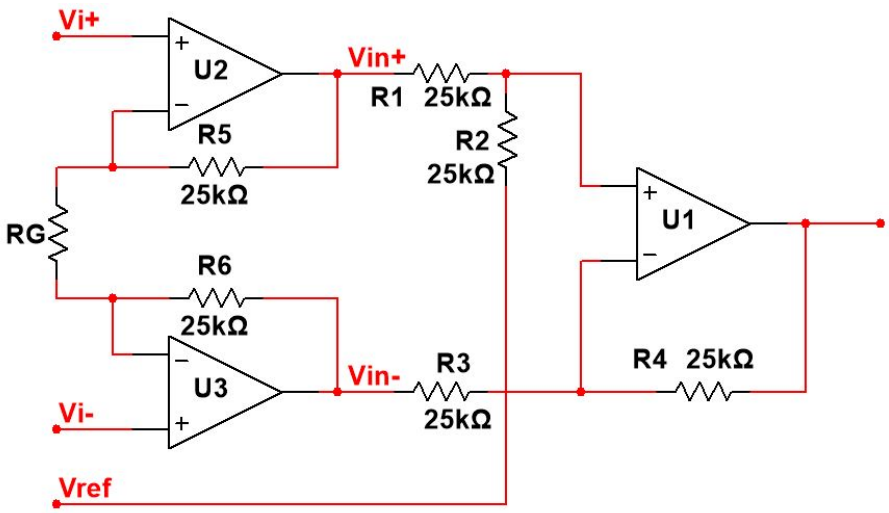
$$V_{out} = \Delta V_{in}\left(\frac{2\ R}{R_G} + 1\right)$$

Since the gain, Av, is V_{out}/V_{in},

$$A_v = \frac{2\ R}{R_G} + 1$$

For a given instrumentation amplifier, R is fixed. In the Burr Brown INA114, the internal impedance is laser-trimmed to 25 kΩ as in the schematics I've provided. Therefore, to set the gain, the designer need only pick an appropriate value for R_G!

The final touch for this extremely versatile circuit is introducing a means of introducing a DC offset. This was done by providing access to the bottom of the voltage divider, allowing the user to reference the circuit to any DC voltage, not just ground, as shown below.



It would have been nice if the designers of the instrumentation amplifier had put a unity gain buffer on the V_{ref} input, but the didn't. Consequently, we suffer from a poor input impedance on this one input, which affects our designs. Typically, to overcome this, we drive the V_{ref} input with an external op amp.

The transfer function for the completed intrumentation amplifier, written basically in the form y = mx + b, looks like this:

$$v_{out} = (v_{in+} - v_{in-})\left(\frac{2\ R}{R_G} + 1\right) + V_{off}$$

where

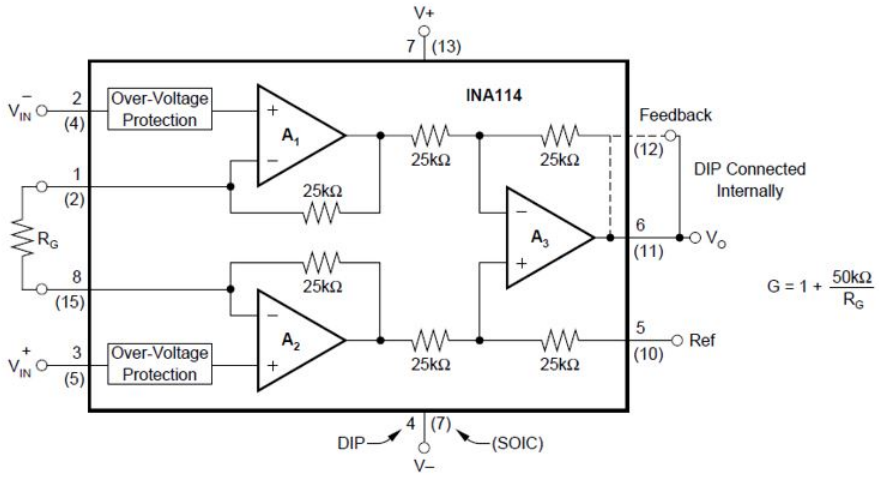
y=v_{out}

m=(2R/R_G + 1)

x=(v_{in+}-v_{in-})

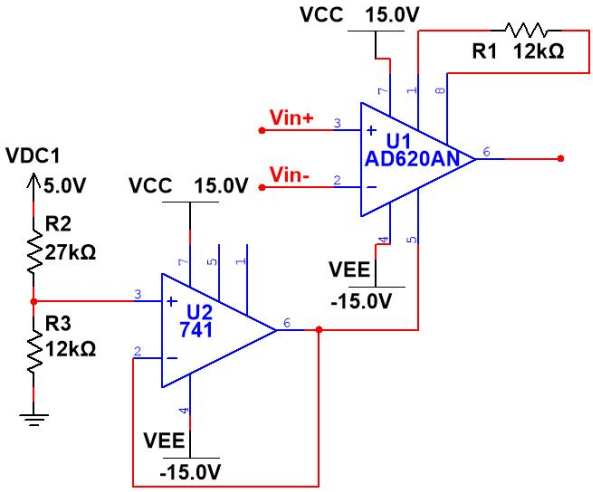
b=v_{off}

Here's a snippet of the Burr Brown INA114 data sheet. We use the 8-pin DIP version of this IC, the pins of which are shown without brackets. For some reason, the designers of this chip chose to use the same pins as those on the 8-pin version of the 741, even though the two ICs are definitely not interchangeable. At least it makes memorizing the pin numbers easy!



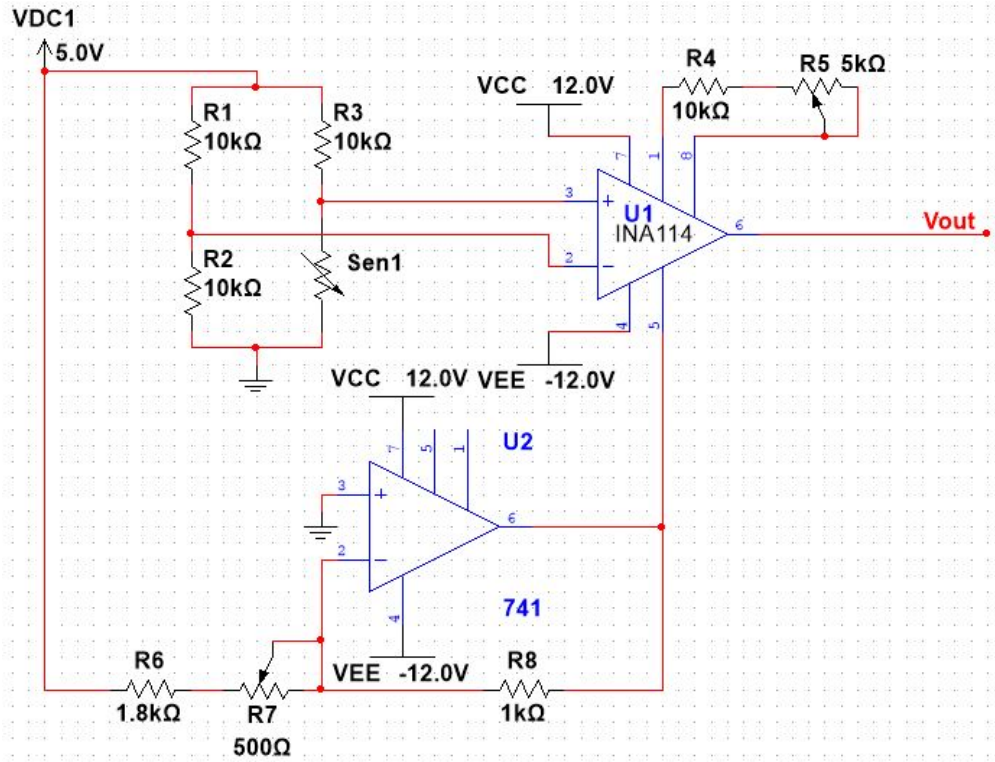
Question 2: (1 point)

Analyze the following circuit to determine its transfer function.



1. The internal resistors for the AD620 are 24.7 kΩ, probably just so they can say they're not copying Burr Brown. Determine the gain for the instrumentation amplifier. This amplifier has the same pinout and functionality as the Burr Brown INA114, discussed previously. _____
2. Determine the DC offset presented to pin #5. _____ V_{DC}
3. Fill in the following Transfer Function expression for this amplifier:
4. v_{out} = _____ x(v_{in+} - v_{in-}) + _____
5. If v_{in+} = +1.34 V and v_{in-} = -0.52 V, what should v_{out} be? _____ V_{DC}

Analyze the following circuit to determine its transfer function.

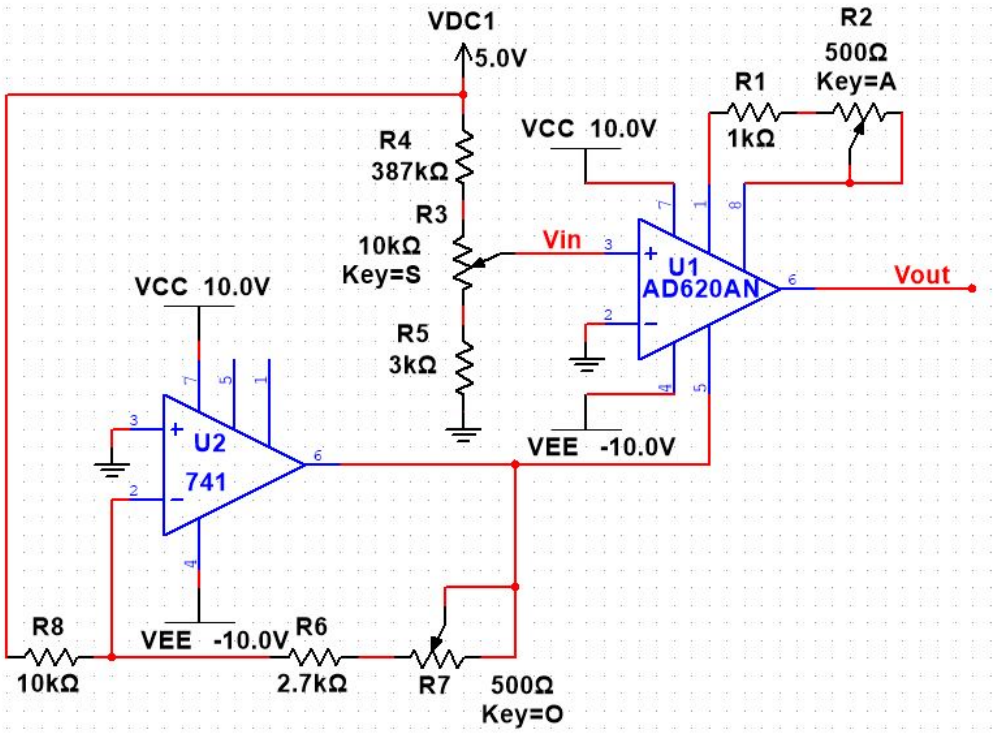


6. The sensor, Sen_1, varies from 6.667 kΩ to 40.0 kΩ. This translates to V_+ ranging from _____ V to _____ V.
7. The differential input signal would range from _____ V to _____ V
8. The output signal for this circuit is intended for an A to D converter than handles signals from -5.0 V to +5.0 V. Plot the endpoints of the transfer function graph below, using the differential input signal and the A to D output range.

null

9. What gain is required? _____
10. When the amplifier is properly calibrated, what do you expect the R_5 resistance to be? _____ kΩ
11. What offset voltage is required? (rearrange y=mx+b and use one of the endpoints for (x,y) to solve for b). _____ V
12. What gain is required for the 741 op amp to produce this offset voltage? _____
13. When the amplifier is properly calibrated, what do you expect the R_7 resistance to be? _____ Ω
14. Fill in the transfer function for this amplifier: V_{out} =_____ $\cdot (v_+ - v_-)$ − _____ ,V

Here's a worked example from an old exam in this course.



The intended transfer function for this circuit is

$$V_{out} = 41 \cdot V_{in} - 1.6,\ V$$

The gain of this amplifier, therefore, is intended to be 41. From the formula for the gain rearranged, we can determine what the combination of R_1 and R_2 (i.e. R_G) should be:

$$R_G = \frac{2\ R}{A_v - 1} = \frac{2 \cdot 24.7\ k\Omega}{41 - 1} = 1.235\ k\Omega$$

This is within the range of available resistances, which is from 1.0 kΩ to 1.5 kΩ.

The offset voltage for this circuit, from the transfer function, is expected to be -1.6 V_{DC}. Since the offset-providing circuit is an inverting amplifier using +5 VDC as its input, the required gain is

$$A_{v(off)} = -\frac{1.6}{5} = -0.32$$

Using the gain expression for an inverting amplifier rearranged, we can determine the appropriate setting for the combination of R_6 and R_7 (i.e. R_f) to be

$$R_f = -A_{v(off)} \cdot R_i = -(-0.32) \cdot 10\ k\Omega = 3.2\ k\Omega$$

Again, this is within the range of available resistances, which is from 2.7 kΩ to 3.2 kΩ.

Now for the expected output range of voltages:

When the R_3 sweeper is all the way to the bottom, using the voltage divider formula we can determine that the voltage at V_{in} will be

$$V_{in} = 5\left(\frac{R_5}{R_3 + R_4 + R_5}\right) = 0.0375\ V$$

In this position, the output voltage is expected to be

$$V_{out} = 41 \cdot (0.0375) - 1.6 \ = \ -0.0625\ V$$

and when the R_3 sweeper is all the way to the top, V_{in} will be

$$V_{in} = 5\left(\frac{R_3 + R_5}{R_3 + R_4 + R_5}\right) = 0.1625\ V$$

In this position, the output voltage is expected to be

$$V_{out} = 41 \cdot (0.1625) - 1.6 \ = \ 5.0625\ V$$

For an input voltage of 87.5 mV, the output voltage is expected to be

$$V_{out} = 41 \cdot (0.0875) - 1.6 \ = \ 1.9875\ V$$

Online Homework System

Assignment Worksheet
5/31/21 - 2:03:35 PM MDT

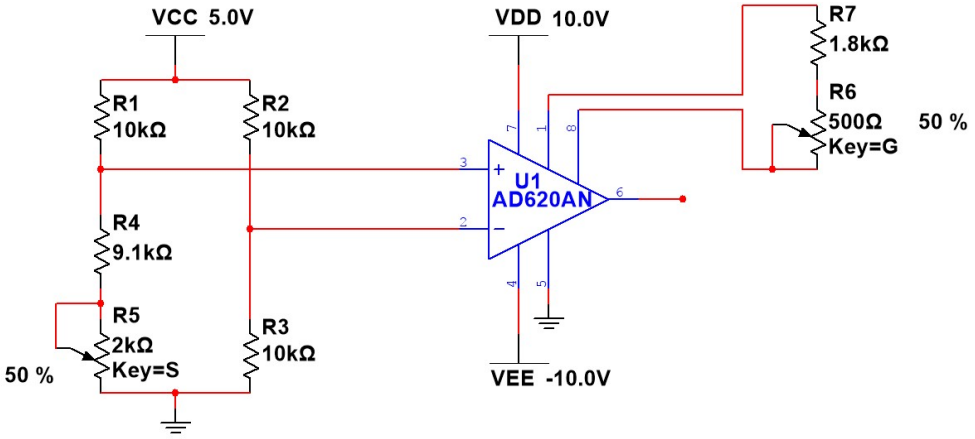
Name: _____ **Class:**

Class #: _____ **Section #:** _____

Instructor: Ross Taylor **Assignment:** SA15 Instrumentation Amplifier Activity

Question 1: (15 points)

Analyze the design below according to the information that follows:



If R_6 is set to midpoint (i.e. to 250 Ω), what is the theoretical gain of this amplifier, given that the internal resistances of an AD620 are 24.7 kΩ? Round your answer to the nearest whole number. _____ V/V.

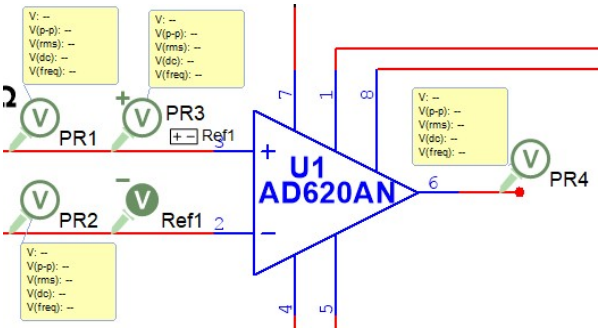
What is the theoretical offset voltage for the circuit as wired? _____ V.

Fill in the blanks in the following transfer function for this amplifier:

Vout = _____ *ΔVin + _____ , V

Using Multisim, build this circuit. The instrumentation amplifier is available under "Analog=>Instrumentation_Amplifiers", and the potentiometers are available under "Basic=>Potentiometer". You can create a "hanging wire" at the output by double-clicking to create a floating end.

Add three voltage probes (PR1, PR2, and PR4 in the following picture) and a differential voltage probe (PR3 and Ref1 in the following picture).



Run the simulator. Adjust the "Signal" potentiometer (R_5 in the schematic) to set the differential voltage as close as possible to 0 V. (You can right-click the potentiometer and change its increment to a finer value, like 1% or 0.5%.) Record the signal voltage, the differential input voltage, and the output voltage, which should be quite close to zero.

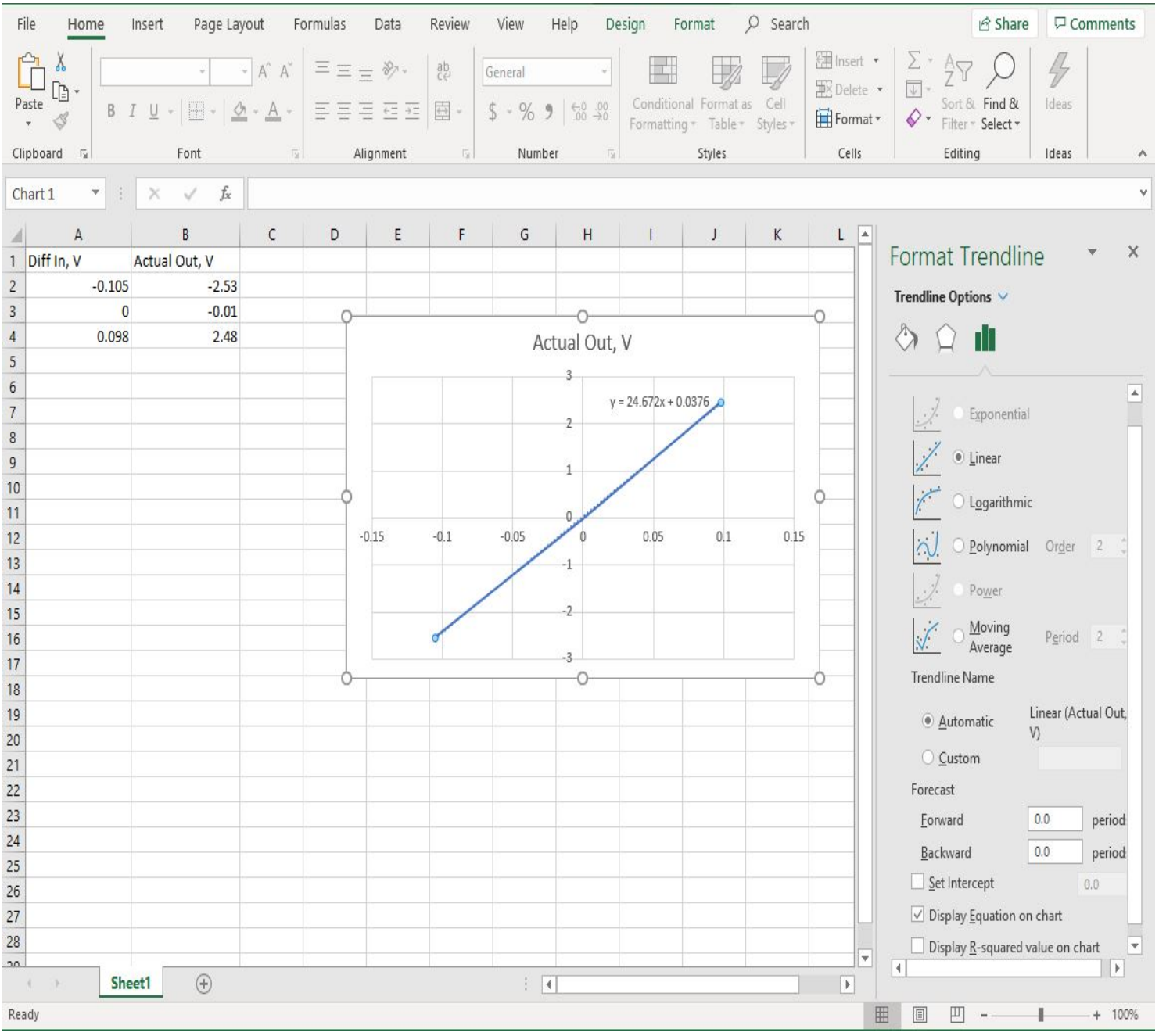
Your next task is to set the differential gain as close as possible to 25. (Again, you will want to set the potentiometer increment to 1% or 0.5%.) To calibrate the gain, set the "Signal" potentiometer so that the input signal is at 2.60 V. Note the differential input voltage below, multiply it by 25, and adjust the "Gain" potentiometer to set the output to the expected voltage. (If you're already getting the "right" answer, play with the potentiometer to see what it does.) Now that the circuit is calibrated, set the "Signal" potentiometer so that the input signal is at 2.40 V, and record the results below.

Signal V	Differential Input V	Expected Output V	Actual Output V

2.40 V	_____ V	_____ V	_____ V
_____ V	0.0 V	0.0 V	_____ V
2.60 V	_____ V	_____ V	_____ V

Use Excel or a similar spreadsheet program to do a "Scatter-plot" of your Actual Output voltages vs the Differential Input voltages.

Add a "Trendline", with "Display Equation on chart" checked. You should end up with something like this:



Enter the slope and offset values in the transfer function below:

Vout = _____ xΔVin+_____ , V

Verify that your transfer function works for a differential input voltage of 0.10 V. V_{out} = _____ V

Online Homework System

Assignment Worksheet
5/3/23 - 11:04:50 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Project 5 Op Amps and Instrumentation Amp

Question 1: (50 points)

Project 5 Preparation and Simulation

This Project must be submitted for grading at the time specified by your instructor. You will be given some class time to work on it, and will be expected to do other work on your own time.

As this is a more formal assessment than the lab activities, your instructor's involvement will be limited to clarification of the requirements and simple feedback on your work. This assessment is intended to show that you have a good grasp of the associated course outcomes, so please limit your interactions with others to points of clarification or improvement of your understanding of the material rather than working together to arrive at solutions.

The first part of this assessment will involve preparatory work and predictions regarding the circuit you will build later, culminating in a simulation to demonstrate operation of parts of the circuit. The second part will involve building and testing a real circuit, and will be graded primarily upon your technical skills of circuit building and use of test equipment.

Grading breakdown:

30% -- Preparatory Work and Predictions

20% -- Simulation

50% -- Circuit Building and Testing

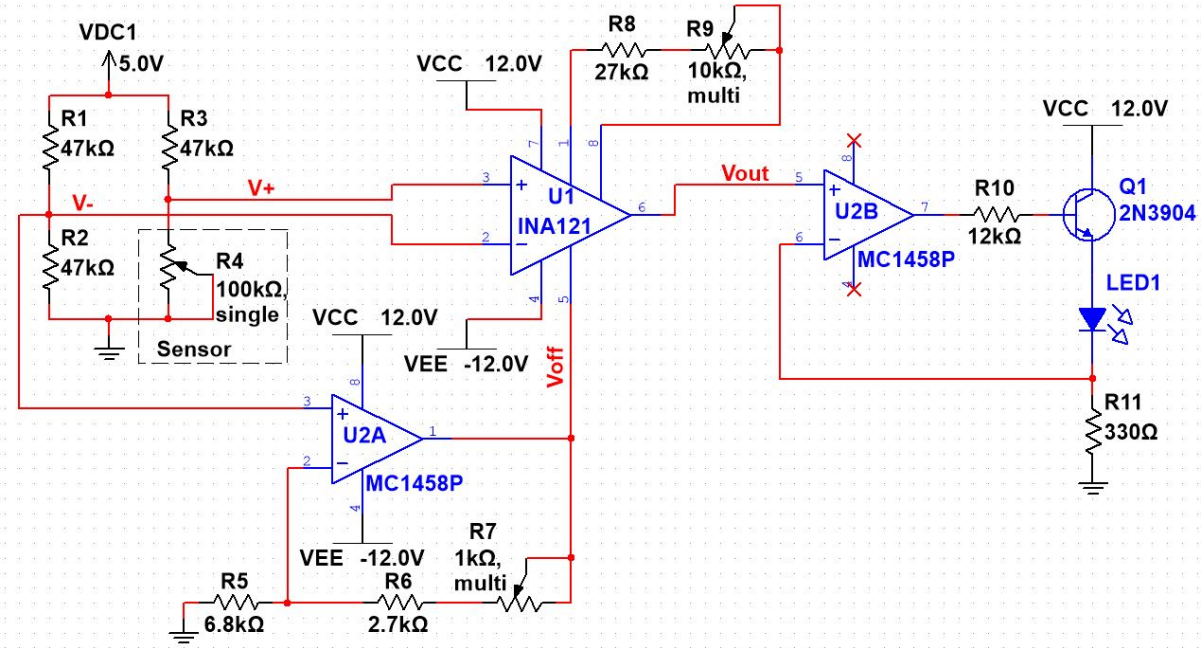
Note: Once you submit this first page and move on to the next, you will not be able to return to it! Instead of moving on to the next question, you can "Save and Close" if you intend to return later.

The "Printable Version" is also available for you to work through before submitting your answers.

You are allowed one "How Did I Do?" to check your answers to this part of the project.

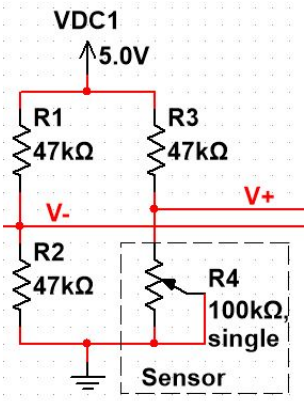
Complete Circuit

The schematic diagram below shows the circuit you will eventually be building, calibrating, and testing. We will analyze it in sections, simulate key components of the design, and then build, calibrate, and test it to ensure proper functionality.



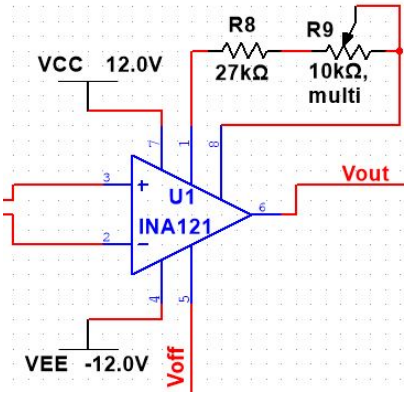
Sensor and Bridge

First, let's analyze the input signal source -- a Wheatstone bridge with three fixed resistors and a variable resistor to represent a sensor. To give it some meaning, consider this to be a pressure sensor. The rest of the circuit interprets the signal from the pressure sensor, and generates a control current through R11 which would control the release of excessive pressure built up in a digester tank.



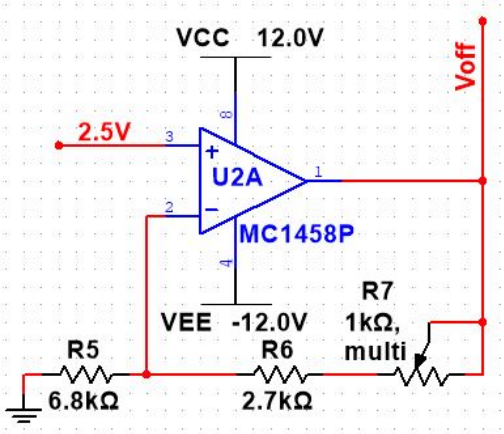
1. The two sides of the bridge are really just two independent voltage dividers. What voltage is expected at V_-? _____ V
2. When the sensor is at its maximum resistance, i.e. 100 kΩ, what voltage is expected at V_+? _____ V. At this setting, what would be the differential voltage between the two outputs from the bridge? _____ _____ V
3. When the sensor is at its minimum resistance, i.e. 0 kΩ, what voltage is expected at V_+? _____ V. At this setting, what would be the differential voltage between the two outputs from the bridge? _____ _____ V
4. For this application, the actual range of voltages for V_+ will be restricted to between +1.0 V and +3.0 V. What is the expected range for the differential voltage from the bridge? _____ V to _____ V

Instrumentation Amplifier



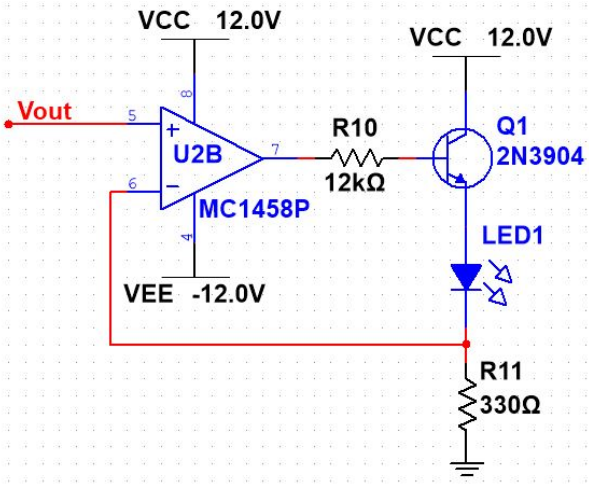
5. For the range of differential input voltages specified above, the expected output voltage range, V_{out}, is expected to be from 0.0 V to 5.0 V. What gain is required for the instrumentation amplifier? _____ .
6. Given that the internal resistances of the INA121 are all 25 kΩ, what is the ideal external gain resistance for the INA121? (Don't pick a standard 10% value.) _____ kΩ. From this, you should be able to verify that the components chosen for R8 and R9 meet the criteria of having a fixed resistor two to five times the size of the potentiometer, with the ideal setting of the potentiometer somewhere close to half its overall value. When the gain is properly calibrated, the resistance of R9 should be approximately _____ kΩ.
7. For the sake of argument, if the gain of the instrumentation amplifier is 2.5 and the output voltage ranges from 0 to 5 V for differential input voltages ranging from -1.5 V to +0.5 V, What offset voltage is required? _____ V

Offset-Generating Amplifier



8. If Voff is to be +3.75 V, what gain is required of the U2A op amp, given an input voltage of +2.5 V? _____
9. Notice the configuration chosen for this amplifier. What is the ideal value for the feedback resistance? (Don't pick a standard 10% value.) _____ kΩ. If this circuit is calibrated properly, what is the expected resistance setting for R7, in ohms, given that it is in series with R6? _____ Ω

Active Current Source and LED Driver

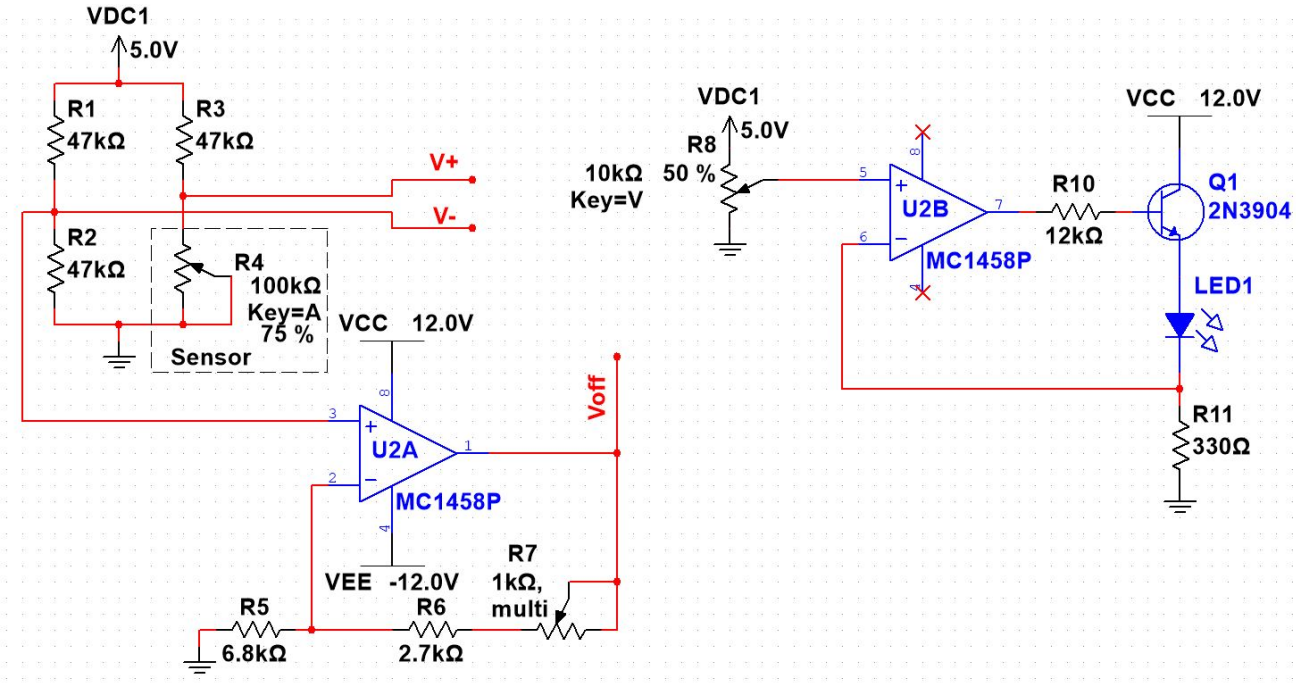


Although the output currents required of this circuit fall within the limits of the MC1458 dual op amp, it is best to use the amplifier as a small-signal device and use a transistor as the actual current source. The configuration above is arranged so that very little current is drawn from the op amp, and all the current generated by the 2N3904 BJT transistor passes through the LED and the current-setting resistor, R11. In our story line, the current through R11 would be used to control a pressure release valve in a manner proportional to the build-up of pressure, which in turn is directly related to the voltage generated by the instrumentation amplifier above.

10. According to the Op Amp Model studied in class, if Vout in the schematic is +3.50 V, what voltage appears across R11? _____ V
11. A suitable Transfer Function for this circuit is $I_{R11} = V_{out}/$_____, A
12. CHALLENGE QUESTION: If Vout = 5.00 V, β = 100, V_{BE} = 0.7 V, and V_{LED} = 1.8 V, what current would flow through R11? _____ mA. What current would flow through R10? _____ μA. What voltage would you expect to see at Pin 7 of U2B? _____ V. From this, hopefully, you can determine that, if U2B can drive a signal to within 2.0 V of the rails, the circuit should be able to operate correctly over the desired range of input values.

Simulation

This simulation covers all but the operation of the instrumentation amplifier. In Multisim, build the circuits shown below. Notes to follow.

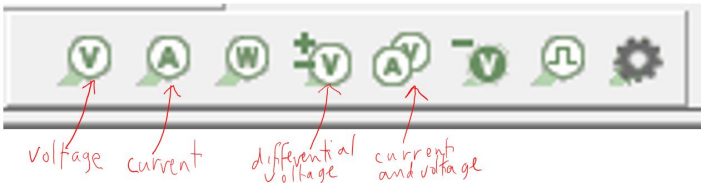


Notes:

- You can terminate or start a trace in "open space" by double-clicking on a given point
- Right-click on a trace and go to "Properties" to assign a "Net Name", and check the box to "Show net name".
- Use "Diodes -->LED-->LED_red" for the LED.
- Make sure the potentiometers are oriented as shown in the schematic above (i.e. take special care to make the centre-tap arrows point in the directions shown). If you do, increasing the percentage will increase the desired circuit characteristic. Ctrl-R rotates, Alt-X flips left to right, Alt-Y flips top to bottom.
- R4 is assigned to the key "S" for sensor, and its "Increment" is set to 1%.
- R7 is assigned to the key "O" for offset, and its "Increment" is set to 1%.
- R8 is assigned to the key "V" for Vout, and its "Increment" is set to 1%.
- Pressing an assigned Key will increase the potentiometer setting, pressing Shift-Key will decrease the setting.
- Make sure you don't have two different ICs in your schematic -- the MC1458 is a dual op amp, so we only need one IC.

Sensor and Bridge Simulation

- Place "Voltage Probes" on V_+ and V_-. Also place a "Differential Voltage Probe" on V_+ with its reference on V_-.
- Place a "Voltage Probe" on Voff.
- Place a "Voltage Probe" on U2B Pin 5
- Place a "Current and Voltage Probe" on the trace connecting the LED to R11 in the schematic. Placement of this probe is crucial -- don't put it on the trace to the op amp; and ensure that the direction of current flow to be measured is downwards.
- Place a "Voltage Probe" on Pin 7 of U2B.



If any of the signals below can't be recorded within three significant digits in the unit specified, indicate "0".

13. Adjust the "Sensor" to generate each of the specified values in the following table as closely as possible, and record the remaining missing values.

Sensor Setting, %	V_+	V_{diff}
0	_____	_____
X	_____	0.0
_____	1.00	_____
X	3.00	_____

100	_____	X

Offset Circuit Simulation -- Calibration

Notice that this circuit capitalizes on the fixed voltage generated by the V- branch of the Bridge Circuit. In most applications, a separate precision reference would be used here instead.

14. Adjust R7 until V_{off} is the desired +3.75 V. The Potentiometer setting for R7 is _____ %

Active Current Source and LED Driver Simulation

15. Verify that all the nodes in the last part of the schematic operate as expected, then set R8 to generate 4.50 V and record the following values:

- V_{R11} = _____ V
- I_{R11} = _____ mA
- V_{Pin7} = _____ V

Multisim Submission: Upload your schematic here for a grade out of three marks. Don't use any spaces or special characters in your filename, but personalize it for easy identification as belonging to you. Document Upload (Direct)

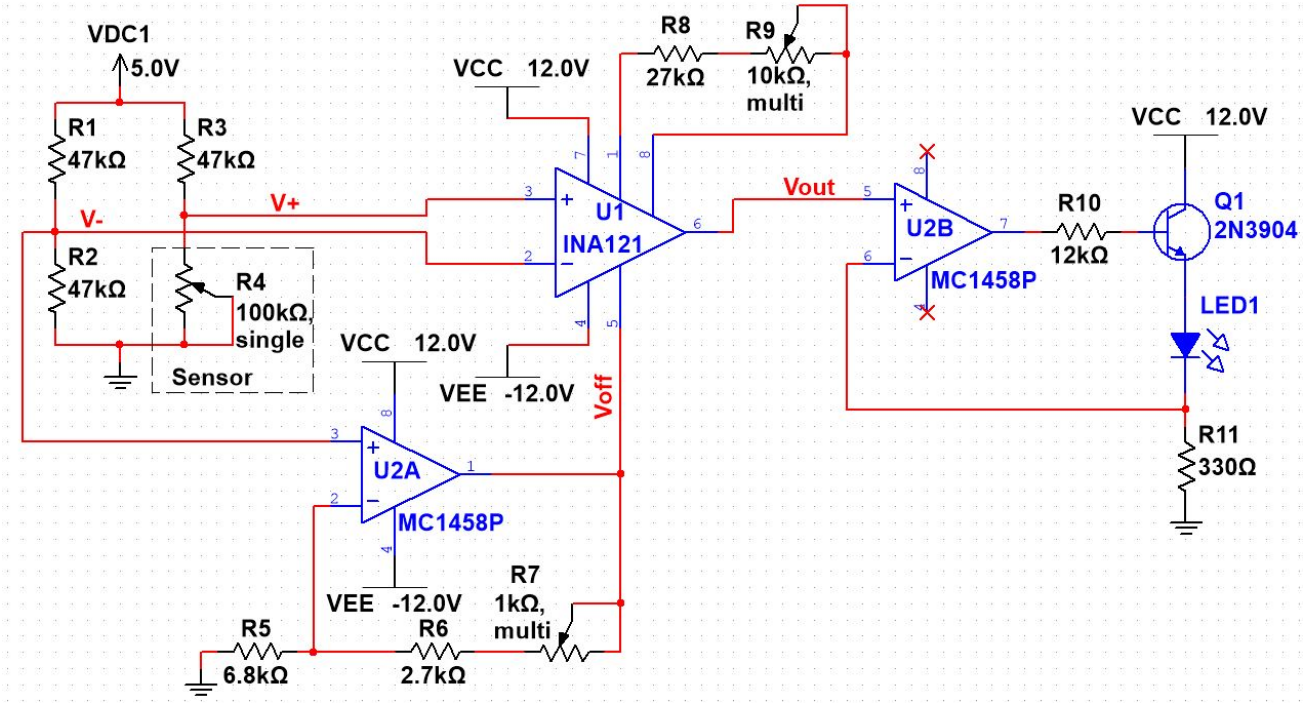
You have now completed the Preparation and Simulation components of this project. Save your work, then move on to the next question (Build, Calibrate, and Test). Once you move on, you will not be able to access this part of the project again!

Question 2: (50 points)

Project 5 Build, Calibrate, and Test

Build

On your breadboard, build the circuit shown below. Notes to follow.



Notes:

- The INA121 is in your "CNT Online Kit", and is a direct drop-in replacement for the more expensive INA114.
- R4 is intended to be a single-turn potentiometer for quick adjustment; it should look something like this -- just make sure it's the right resistance:

- R7 and R9 are intended to be multi-turn potentiometers for fine control during calibration, and should look something like this:

- If any of the potentiometers decreases the associated circuit characteristic when turned clockwise, pull it out of the breadboard and rotate it 180^{o} to get the correct action.
- Note that the two op amps are U2A and U2B; in other words, they are the two op amps in a single MC1458 IC.
- ***It is highly recommended that you build this circuit in stages, and test each stage before moving on!*** Build the bridge first, then the Offset Circuit, add the Instrumentation Amplifier, and end with the Current Source and LED Driver.

Calibrate

Once your circuit has been built and each stage has been tested, you will need to calibrate the Instrumentation Amplifier section. Calibration is much simpler when zero volts is one of the input values, which is the case for this circuit.

Here's the Transfer Function for the Instrumentation Amplifier:

$$V_{out} = 2.5\ V_{diff} + 3.75,\ V$$

- Adjust the "Sensor" until the voltage between V_+ and V_- is as close as possible to 0.00 V. You should now be able to adjust the OFFSET voltage to make the output from the INA121 exactly what you want it to be from the Transfer Function.
- Now, adjust the "Sensor" until the voltage between V_+ and V_- is as close as possible to -1.50 V. You should now be able to adjust the GAIN to get the expected output from the Transfer Function.
- Double-check your results by setting the "Sensor" until the voltage between V_+ and V_- is +0.50 V. Check to see if the output matches what's expected from the Transfer Function. If not, you may need to tweak the GAIN and OFFSET until the output range matches what's expected from the input range.

Final Test

Once your circuit is fully calibrated, fill in the following table to demonstrate how well it meets the specifications. For the Current, use Ohm's Law to calculate this using the resistance of R11 rather than using an ammeter, unless you have two meters available -- one to measure voltages and one to measure current. If you choose to measure current, make sure you insert the ammeter *in series* with R11, not in parallel across it!

V_{diff}, V	V_{R11}, V	I_{R11}, mA
-1.00 V	_____	_____
0.00 V	_____	_____
0.50 V	_____	_____

Submission: For a grade out of four, upload a picture of your working circuit, set to the last value in the table above, with a voltmeter showing the voltage across R11. If your instructor grades your work in class, upload a text file indicating the grade assigned. Document Upload (Direct)

You have now completed this project. Once you submit your work, you will not be able to return to any of these questions!

Online Homework System

Assignment Worksheet
5/20/22 - 9:35:03 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Digital To Analog Conversion

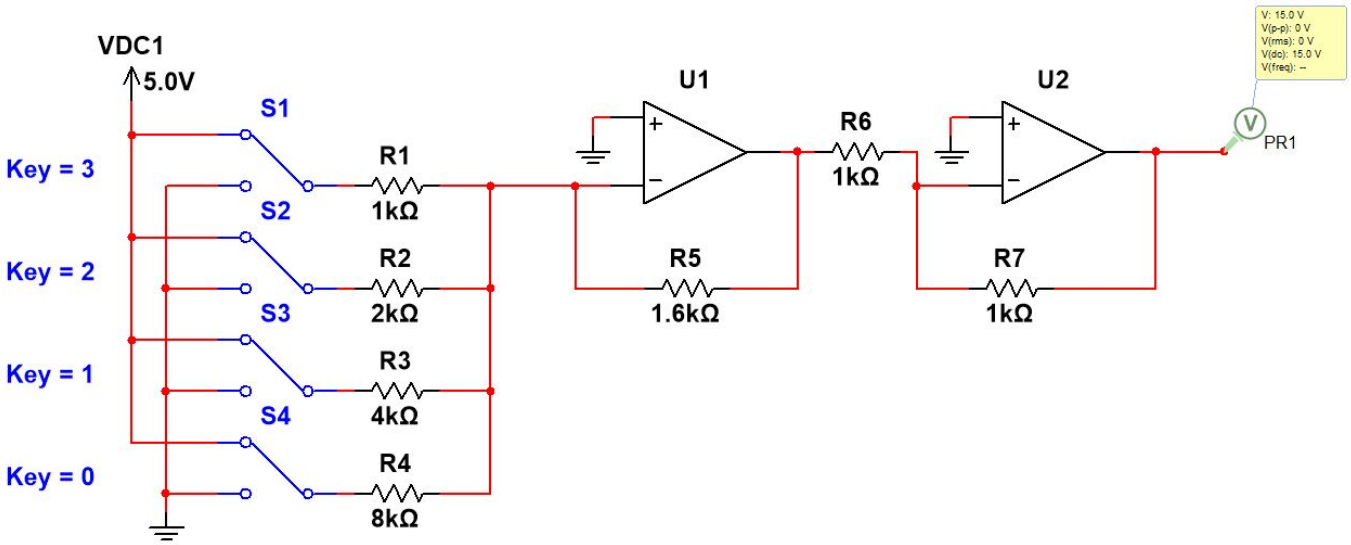
Question 1: (1 point)

Digital to Analog Conversion, DtoA, is one half of the interface between the "real world" and binary devices. The other half is Analog to Digital Conversion (AtoD). AtoD Conversion is the process whereby an analog electrical signal generated by something in the real world is sampled and converted by an Analog to Digital Converter (ADC) into a binary representation and stored in a memory device. Digital to Analog Conversion is done by a Digital to Analog Converter (DAC) which takes binary values and generates the electrical signals they represent in order to produce something recognizable in the real world.

For example, consider an audio recording. A human voice generates constantly-changing sound pressure levels that are picked up by a microphone, which converts them, with the help of a signal conditioning circuit, into a constantly-changing voltage signal. An ADC samples the signal at a clearly-defined sample rate, generating a binary representation of each sample, which it sends to a memory device. To play back the recording, a DAC, running at the same sample rate, reads the stored binary values in the same order as they were generated and converts them into voltages which are sent by means of an amplifier to speakers or headphones to recreate sound pressure levels that are intended to be a reasonable representation of the original audio signal.

It seems like we should start with AtoD. However, DtoA is a simpler process. In fact, the most common ADC actually has, as just one of its components, a DAC. So, we'll start with DtoA and revisit AtoD after we've learned about voltage comparators.

The following circuit is a somewhat contrived 4-bit DAC with a huge step size -- not great for producing a good representation of an analog signal, but something that will help us learn how a DAC works.



Using Multisim, build this circuit.

The op amps are from ANALOG_VIRTUAL. You need to edit them so that the Positive voltage swing(VSW+) is +20 V and the Negative voltage swing(VSW-) is -20 V.

VDC1 is from Sources, and is V_REF1.

The switches are SPDT (single pole double throw) from SWITCH in Basic.

Run your circuit and fill in the following table, assuming that 0 V is logic LOW and +5 V is logic HIGH:

Binary input	Vout, V
0000	_____
0001	_____
0010	_____

0011	_____
0100	_____
0101	_____
0110	_____
0111	_____
1000	_____
1001	_____
1010	_____
1011	_____
1100	_____
1101	_____
1110	_____
1111	_____

Given that a Binary Step is from one number to the next, what is the step size for this DAC? _____ V/step

Mathematically, the step size can be determined a number of ways. If you know the entire range of values, you can use the following formula:

$$V_{step} = \frac{V_{range}}{2^n - 1}$$

...where n is the number of bits in the binary value.

This works because there will always be one less step than the number of voltage levels possible. Notice in our example that there are sixteen possible voltage levels -- 0 through 15, but if you start at zero, there are only 15 steps to the top. Check that on a staircase sometime! Also notice that you have five fingers on your hand, but only four gaps between them -- same concept.

Use this formula to determine the step size. _____ V/step

Electrically, for a DAC or ADC to work, they need a voltage reference. For reasons we'll see later, that voltage reference is always one step above the top end of the range. So, if you know the voltage reference, you can use the following formula:

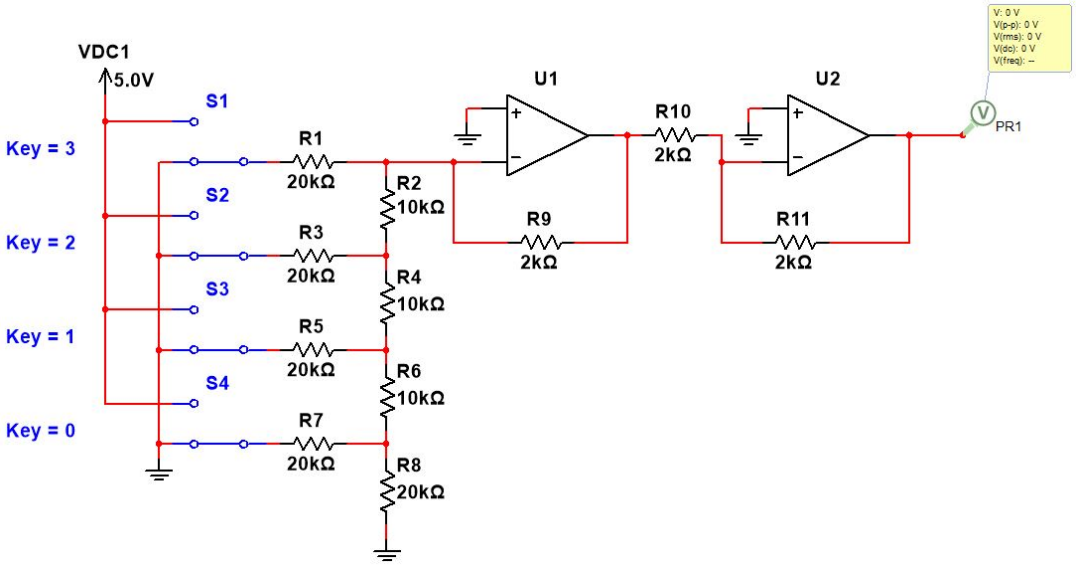
$$V_{step} = \frac{V_{ref}}{2^n}$$

In our example, the reference voltage would be 16 VDC. Use this to determine the step size. _____ V/step

Looking back at the circuit, notice the strange resistor values -- only one or two of them are commercially-available. Imagine if this circuit had eight or sixteen input bits. The values would not only not be available, but the largest one would be 128x the size of the smallest one. Since this in an inverting amplifier, it means that the input impedances for each bit would be different. If the bit sources were non-ideal, this would introduce some pretty strange inaccuracies in the output voltage. We'll investigate a better DAC on the next page.

Question 2: (1 point)

In the previous century, someone came up with a circuit that uses just two resistor values: a resistor, R, and twice that resistance, 2R. Here's a 4-bit DAC using what is called the R-2R Ladder at its input.



Using Multisim, build this circuit. Be really careful about the resistor values -- notice that R8 is 20 kΩ, and that R9 - R11 are all 2 kΩ.

Run your circuit, and fill in the following table of selected values. Make sure you record your answers in millivolts.

Binary Input	Output Voltage, mV
0000	_____
0001	_____
0100	_____
1000	_____
1111	_____

You should have seen that the values range from 0 to 937.5 mV. Using the "range" related formula, determine the step size _____ mV/step

The problem is predicting this step size without actually building the circuit and testing it. For this, we'll try another approach. Notice that, for any of the samples you took, you can get the step size by dividing the output by the binary input. That's because, for example, there are four steps between 0 and step 4. To prove this, divide your output for step 4 by 4 to get the step size: _____ mV/step

So, what we need to do is find an easily-analyzed input value, determine its output, and divide by that number of steps. Look back at the circuit: The easiest input combination to analyze is 1000, or eight. Here's why.

Notice that there's a virtual ground at the inverting input, because the non-inverting input is grounded.

If all the lower bits are grounded, no current will come to the summing point, because they will all be at zero potential.

Therefore, if the most significant bit is HIGH, it will be the only input contributing anything to the output signal.

So, let's use circuit analysis to predict the theoretical step size for this R-2R ladder DAC.

What is the gain of the first amplifier for just the MSB? _____

What is the gain of the second amplifier? _____

So, for the MSB, what is the overall gain? _____

Multiply the HIGH input voltage for the MSB by this gain to determine the expected output for 1000. _____ mV

Now, divide by the number of steps between 0000 and 1000 to get the step size. _____ mV/step

That's it! Extending what we just did, we should be able to predict the output voltage for any input by multiplying the step size by the binary input value. Fill in the following table of selected values.

Binary Input	Predicted Output, mV
0011	_____
0101	_____
0111	_____
1010	_____
1101	_____

Question 3: (1 point)

The following should provide you with an understanding of some of the theory and terminology related to DACs (and ADCs).

DAC Terminology

Single Quadrant DAC – The DACs we've been looking at have all used positive (unsigned) binary inputs to produce positive (or negative, if the amplifier is inverting) outputs. In other words, on a coordinate plane, all the results would fit into one quadrant, usually the top right quadrant.
Two-Quadrant DAC – We could level-shift the output so that the results would run from negative to positive, but still with unsigned binary inputs. In this arrangement, it would make sense to make zero volts match the middle of the binary scale. Our results would now occupy the two quadrants on the right side of the coordinate plane.
Four-Quadrant DAC – If we included some logic that converted signed binary inputs into signals that could produce positive to negative output voltages, we would have a DAC that used the entire coordinate plane. Most commercially-available DACs can be configured as Four-Quadrant DACs, and are well-suited to software applications that need to produce full-range output voltages from conventional 2's complement signed binary inputs.
Digitizing – An analog signal has an infinite number of possible voltages over the range between its upper and lower limits. However, a digital signal has discrete output voltages with nothing in between. When we represent an analog signal digitally, we lose some of the accuracy of the signal because we must round each value to the nearest digital equivalent.
Quantization Error – The error introduced will be between 0 and 1 LSB, i.e. the step size. Many DACs offset their values to make the minimum error ±0.5 LSB.
Step Size – The total range is one step less than the reference:

$$V_{step} = \frac{V_{range}}{2^n - 1}$$

or

$$V_{step} = \frac{V_{ref}}{2^n}$$

Sample Rate – For a DAC, the number of digital values converted to an analog output voltage per second is the Sample Rate. The sample rate must be at least twice the highest expected frequency component. (This comes from Nyquist communication theory.)
Resolution – The greater the possible number of digitizing values, the better the signal can be approximated. High resolution means low Quantization Error, but requires more bits.
Linearity – A linear DAC will show a straight-line relationship between the binary input and the voltage output. As a specification, Linearity states how close to a straight line you can expect the output to be.
Monotonicity – If, as the binary input ramps up, the output from a DAC does not always step up as expected, (i.e. some steps actually drop below the previous value), the DAC is not Monotonic.

Answer the following questions about an 8-bit Single Quadrant DAC.
If the output values range from 0 V to +10.0 V, what is the step size? Give your answer to five digits, in mV. _____ mV/step
Fill in the following table for selected input values. Provide your answers in volts this time, to four decimal places.

Input value, hexadecimal	Output Voltage, V
0x00	_____
0xFF	_____
0x80	_____
0x93	_____

Answer the following questions for an 8-bit Two-Quadrant DAC in which the outputs have been shifted to provide a range from -2.50 V to +2.50 V.

What is the step size for this DAC? Give your answer to 6 digits, in mV. _____ mV/step

Fill in the following table for selected input values. Provide your answers in volts, to four decimal places.

Input value, hexadecimal	Output Voltage, V
0x00	_____
0xFF	_____
0x7F	_____
0x80	_____

Hopefully, you just seen one of the conundrums of DACs: If the range of values is nice, the step size will be awkward, and critical values, like zero or half the scale, will not be available. If the step size is nice, the range will be off by a single step at the top end. That's enough to drive any OCD person just a bit crazy!

Here's an example of a Four-Quadrant DAC with a nice step size. Since this is a Four-Quadrant DAC, the binary inputs can be negative or positive, using the 2's Complement system. You'll probably need to convert the hexadecimal values into binary so you can see whether they're negative or positive, then, for the negative ones, you'll have to do a 2's Complement conversion to see what each negative number is.

A particular 12-bit Four-Quadrant DAC has a step size of 2.5 mV/step.

What is the most positive input value, in hexadecimal? _____ What is this, as a decimal number? _____

What is the expected output voltage, based on the step size of 2.5 mV/step? Give your answer in volts, to four decimal places. _____ V

What is the most negative input value, in hexadecimal? _____ What is this, as a decimal number? _____

What is the expected output voltage? _____ V

Fill in the following table to analyze the predicted outputs for two selected values.

Input, hexadecimal	Decimal equivalent	Output, V
0x42D	_____	_____
0xA3C	_____	_____

One of the issues with digitizing analog signals is the amount of memory required for storage. Here's an example to quantify that statement.

Let's analyze one minute of uncompressed video recording that's 1024x768 pixels, each in 32-bit colour, if the sample rate is 24 frames per second.

1024x768 pixels x 32 bits/pixel is just over 25 megabits (Mb) per frame. Multiply that by 24 frames per second to get about 604 Mb per second. Now, multiply by 60 seconds, and you get over 36 Gb of required storage! Divide by 8 bits per byte, and the result is 4.53 GB of required memory for just one minute of uncompressed video, and that's not even HD! In storage values, which are off by a factor of 1.024, this is 4.42 GB. Given that a standard DVD can store 4.7 GB, one minute of uncompressed video of this quality would take essentially one whole DVD!

That brings up a very significant advancement that makes storage and distribution of digitized information possible: Compression.

Compression involves the use of algorithms to reduce the number of bits that need to be stored, while still containing enough information to represent the original data. Compression comes in two general forms: Lossless, where none of the data is lost, and Lossy, where the decompressed information does not contain all of the original data, but is a close approximation. JPEG compression is lossy -- if you zoom in on a JPEG picture, you'll see blocks of pixels that are all the same colour and density -- those regions were determined to have similar enough characteristics that they were treated as identical. In the compression algorithm, the characteristic is recorded once and is assigned to the matching group of pixels, saving a lot of memory. MPEG-4 is also lossy. One of the techniques in this algorithm is only to record when pixels change enough to require an update. So, a blue sky doesn't need to be stored. If you're sitting in front of a stationary camera doing a recording, none of the background needs to be updated -- just the parts of your face that are changing.

So, it's clear there is a lot more that could be learned about digitizing real world events and storing them, but hopefully this has been an informative introduction.

Online Homework System

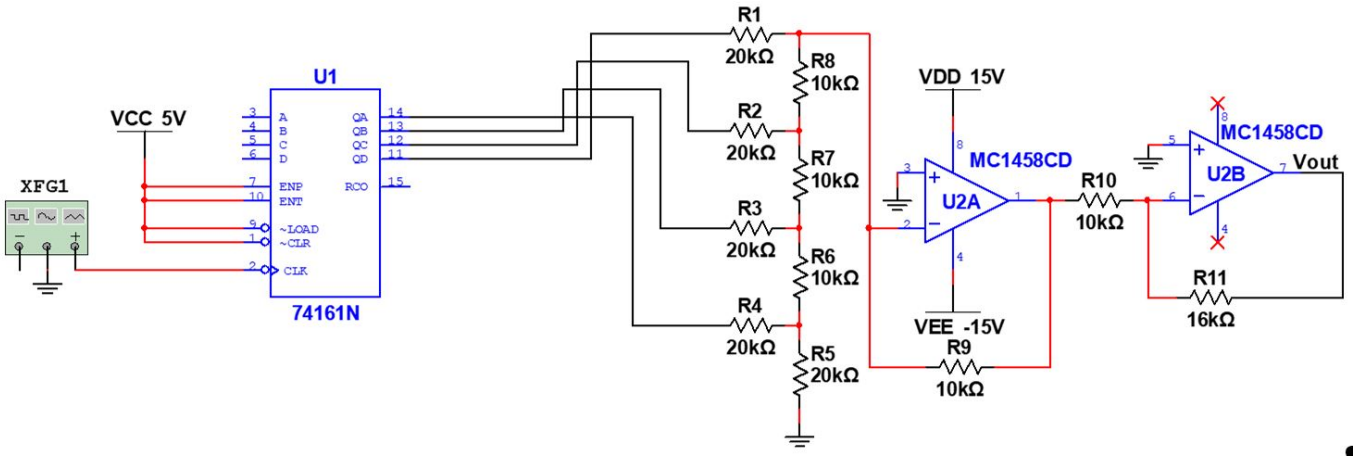
Assignment Worksheet
11/7/22 - 8:30:07 AM MST

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Lab07 Digital to Analog Conversion

Question 1: (10 points)

Lab 07 Pre-Lab Assignment

Use the circuit shown below to answer the questions that follow.



Using the technique described in the Online Lesson for determining the step size for an R-2R Ladder DAC, start by assuming the digital inputs are set to 1000_2. If a HIGH is +5 V and a LOW is 0 V, determine the expected output voltage for the binary input 1000_2. _____ V

From your output voltage and the binary input value, determine the step size for this DAC, in millivolts. _____ mV/step

Using the DAC step size, fill in the following table of selected values. Record your answer in volts, rounded to one decimal place.

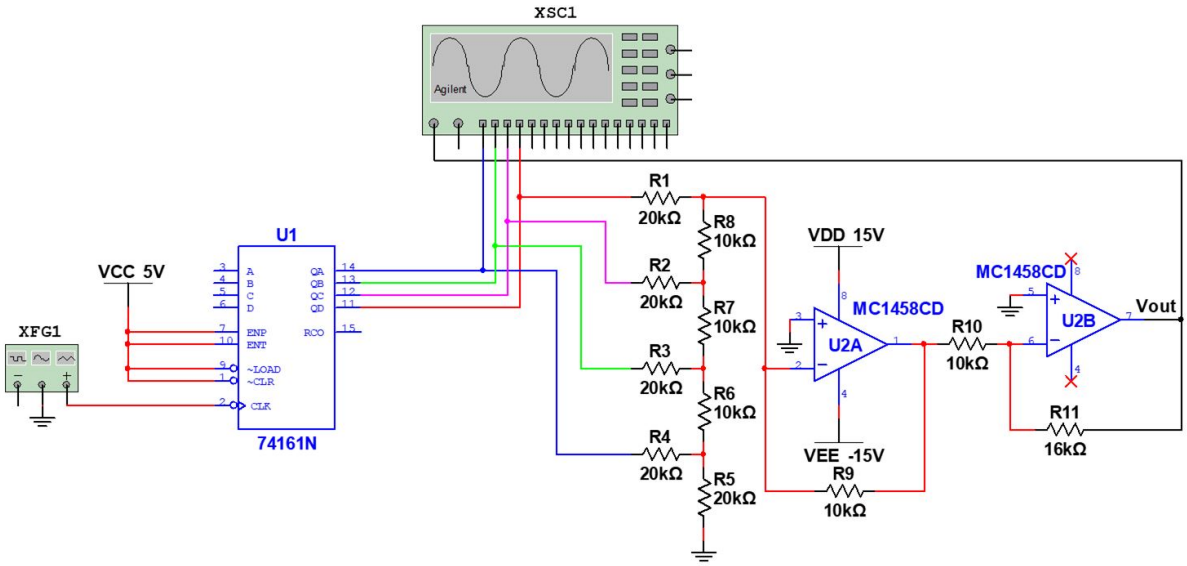
Binary Input	Predicted Output, V
0000	_____
0001	_____
0111	_____
1010	_____
1101	_____
1111	_____

You have now finished the Pre-Lab. Move on to the Lab Activities. Do not click "submit" yet!

Question 2: (10 points)

Lab 07 Activity, Part 1: R-2R Ladder DAC

Use Multisim to build and test the R-2R Ladder DAC from the Pre-Lab exercise, shown below. The 74161N is found in the TTL logic group.



Set up the function generator to produce a square wave with a frequency of 200 Hz, a duty cycle of 50%, an amplitude of 2.5Vp, and a DC offset of 2.5 VDC. This will produce a 0.0 V to 5.0 V pulse to drive the clock of the 74161.

The 74161 is a Synchronous 4-bit Binary Counter, so it will cycle through an output count from 0000 to 1111, then start again.

Use an Agilent 2-channel oscilloscope. On this scope, the first two inputs are actual oscilloscope channels, and you will use the first of these to observe Vout. The next sixteen inputs are for a logic analyzer function in the scope. As shown in the picture above, we're connecting to the bottom four bits of the logic analyzer -- b3, b2, b1, and b0. To view these, press the "D7 Thru D0" button.

You'll notice that the wires are differently-coloured in the picture above. That's because, with the Agilent scope, the colour of the displayed trace matches the colour of the wire connected to it. This will help you tell your traces apart. You can change the colour of a wire by double-clicking on it to bring up the appropriate menu.

Adjust your oscilloscope settings so that one or two complete ramps of the generated output signal appear on screen. Hint: the clock is running at 200 Hz, and each ramp takes a full count of 16 clock cycles. Also, the signal ranges between 0 and 7.5 V, according to your Pre-Lab.

Once your circuit is working and you have suitable settings for your oscilloscope, Use the snipping tool or something similar to screen-capture your circuit and the oscilloscope display. Submit your picture here for a mark out of two. Document Upload (Direct)

By locating the correct binary sequence on the logic analyzer traces and measuring the output voltage (you could try the cursors, unless you come up with a better way), fill in the following table for selected values.

Binary Input	Output, V
0011	_____
0111	_____
1010	_____

Based upon the number of steps in a complete ramp and the clock frequency of 200 Hz, what do you expect to see for the frequency of the ramp signal at the output? _____ Hz (You can verify this with the oscilloscope.)

Lab 07 Activity, Part 2: DAC Characteristics

In this exercise, you will investigate the effect of increasing the number of bits, and hence the resolution, of a digitized signal using Excel. You will find a template file in Moodle as a starting point. Please locate that file, download it, and open it in Excel.

Column A is time in 200 μs intervals up to one full second. Needless to say, that's a lot of lines! You definitely don't want to be dragging values down that far, so you'll be given some hints in how to get around Excel as this exercise unfolds.

First, let's look at what's already in the spreadsheet.

Click on cell 2B, and look at the formula in the formula bar above. This is the standard form for a sine wave with DC offset. In regular form (i.e. not Excel formatting), this looks like

$$v_t = V_{off} + Vp \sin(2 \pi f t)$$

The frequency is found in cell L1. click on this cell, and you'll see that its name has been changed to the variable "f". You can try this, if you've never done so before, in some unused cell with some variable that won't influence the spreadsheet. For example, click on V1. Before you do anything else, change its name in the box in the top left corner by the formula bar to "Var". Now, any time you want to use V1, you can type Var instead.

In the formula, the time, t, is the time for that line found in column A. If you look at B2, for example, you'll see A2; in B3 you'll see A3, etc.

Notice that π is given as Pi(). Just as you've experienced in high level languages like C#, this is a void method that returns the value of Pi, hence the brackets.

Now look at C2. In this cell, the voltage in cell B2 is converted into a 2-bit binary value. The voltage is divided by "step2", which is found in L5. Take a look at L5 -- the step size is generated using Vstep = Vrange(2^n - 1). Back in C2, after the division, 0.5 is added to round the answer up, then the result is converted into an integer. Finally, the result is converted from decimal to binary with only 2 bits (",2").

From that discussion, you should be able to create a formula for E2, which should result in a 4-bit code for the same voltage. If all went well, you should get 1000 in E2.

Now look at D2. In this cell, the binary value is converted back into the corresponding voltage by multiplying the binary value by the step size for the 2-bit converter. From this, you should be able to create a formula for F2, which should result in a voltage based on the 4-bit code in E2. If all went well, you should get the results shown in row two of the spreadsheet below.

Continue across, generating formulas for G2, H2, I2, and J2.

You should now have the following:

	A	B	C	D	E	F	G	H	I	J	K	L	M
1	Time	V	2b code	2b V	4b code	4b V	6b code	6b V	8b code	8b V	f=	1	Hz
2	0	2.5	10	3.333333	1000	2.666667	100000	2.539683	10000000	2.509804	Vmax=	5	V
3	0.0002	2.503142	10	3.333333							Vp=	2.5	V
4	0.0004	2.506283	10	3.333333							Voff=	2.5	V
5	0.0006	2.509425	10	3.333333							2bit step=	1.666667	V
6	0.0008	2.512566	10	3.333333							4bit step=	0.333333	V
7	0.001	2.515708	10	3.333333							6bit step=	0.079365	V
8	0.0012	2.518849	10	3.333333							8bit step=	0.019608	V
9	0.0014	2.521991	10	3.333333									

Now comes one of Excel's "magic tricks". By dragging your mouse across from E2 to J2, select the cells you've just modified.

In the bottom right corner of your selection, you'll see a tiny green square. Double-click on this. If all went well, all of your formulas will now have copied down to the end of the data to their left!

Next, we want to see the results of our efforts. For this, we'll do x-y graphs of each of the DAC outputs compared to the analog input.

With your mouse, click and highlight the A and B at the top of the first two columns. Select "Insert" "Scatter Plot" (that's the picture of a set of axes with dots between them, probably directly above the word "Charts"). I recommend using the straight-line version without data points displayed. You should now see a graph of a single cycle of a sine wave, ranging from 0 to just over 5 V, and a period of 1 s.

Now, click on the F at the top of the sixth column to select that whole column. Press "CTRL-C" to copy that column. Now, in the graph you just created, in the white-space beside the title, right-click and paste. You should now have the 4-bit digitized version of the data superimposed over the analog input, just like the 2-bit version that was already present in the template.

Repeat these steps to create similar graphs for the 6-bit data and the 8-bit data.

Adjust your graphs and data on screen, do a screen-shot, and upload it here for your instructor to give you a mark out of 2. Document Upload (Direct)

Now, change "Vp" to 0.1 V. Which of the DACs produces the best representation of the input signal, even for this small a signal?

(a) 2-bit

(b) 4-bit

(c) 6-bit

(d) 8-bit

Notice that the step size for the 8-bit DAC is a value that would be difficult to work with mathematically. Rounding this step size up to the nearest 1/100th gives us a nice 20 mV/step. Use the step size formula to determine what Vmax would need to be to generate this step size.

_____

You have now completed this Lab. Click "Submit" to send out your work for grading.

Online Homework System

Assignment Worksheet
5/3/23 - 9:59:46 AM MDT

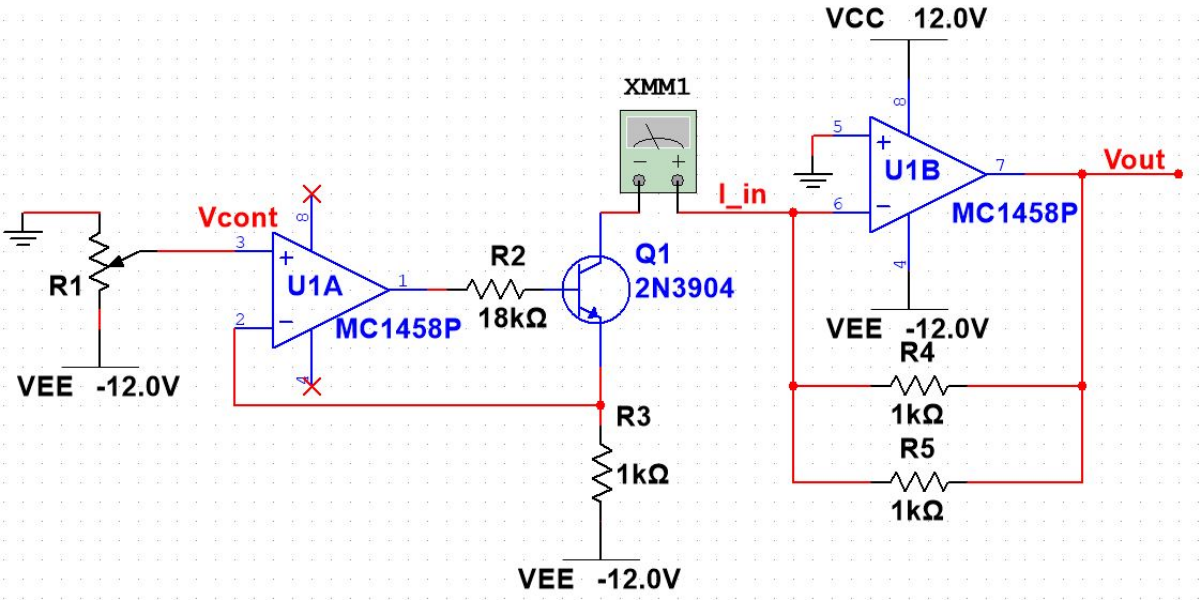
Name: _____ **Class:**

Class #: _____ **Section #:** _____

Instructor: Ross Taylor **Assignment:** SA16 Active Current to Voltage Converter Activity

Question 1: (20 points)

Various devices, such as the AD590 temperature sensor, generate a controlled current rather than a voltage. To convert a current to a voltage, all that's needed is a resistance of known value and Ohm's Law. However, it is often useful to include an op amp in the circuit in order to establish gain and offset values. In the schematic below, the transistor acts as a current source (remember, a BJT is a current-controlled current source). In order to produce a useful current, the first op amp is used as a unity gain buffer to establish a controlled voltage across the current-limiting resistor. The input of the unity gain buffer is supplied by a potentiometer set up as a variable voltage divider. The second op amp circuit translates the transistor's collector current to a voltage. The Base resistor, R_2, has been chosen to limit the Base current while keeping the output voltage of U1A within the available range of output voltages for the op amp. As a practice exercise, you could verify that the value chosen is suitable.



1. Using the Op Amp Model, if the input control voltage V_{cont} = -5.0 V, what will the voltage be at the Emitter of Q_1? _____ V
2. If V_{cont} = -5.0 V, what will be the current through R_2? _____ mA
3. Since the transistor β is more than 100, we can assume that the Emitter current (the current through R_3) is essentially the same as the Collector current, which is I_{in}. When I_{in} = 7 mA, V_{out} will be _____ _____ V
4. Fill in the following Transfer Function for the second op amp (the current to voltage converter): $V_{out} =$ _____ $\cdot I_{in}$, V

Using your breadboard, build this circuit, using a single MC1458CD dual op amp IC. Use a +/-12 V power supply to power the circuit. Use a 10 kΩ single-turn potentiometer for R1.

One issue we face is measuring the input current. Since using a DMM as a current meter always seems fraught with catastrophic errors on the part of students, we normally hesitate to proceed with it, but hopefully if you're properly forewarned, you won't do anything that will kill your power supply or your circuits.

- A current meter is the same as a piece of copper wire -- it acts as a dead short between two points in a circuit.
- If you wouldn't put a piece of wire there, don't put your current meter there!

Unlike when measuring voltages, we do NOT use ground as a reference point -- that would mean whatever we touch in the circuit with the other lead would be shorted to ground, usually resulting in a dead power supply, a burned out component, or a blown fuse in the meter. (Your DMM probably came with extra fuses, but replacing them is not an easy task.)

OK, hopefully we've scared you enough that you will follow these instructions carefully!

Start by configuring your DMM as an Ammeter -- you need to plug the test leads into different jacks than for the other measurements done by the meter. Set the meter to measure milliamps. (If you're using the HT118A, it will flash to show you where to connect the leads.)

As shown, insert your DMM, configured as an ammeter, ***in series*** with your transistor. Notice the polarity of the connections on the multi-meter: this will give you positive current readings, as current will be flowing from the virtual ground toward the negative supply.

Measure the voltage at the output from your circuit. You could use a DC-coupled oscilloscope or your Analog Discovery 2, configured as a voltmeter.

5. Adjust the potentiometer to set the output voltage to values close to those suggested in the following table, and record the actual values for input current and output voltage. For grading purposes, make sure you enter the input current in milliamps.

Input Current, mA	Target Output Voltage	Actual Output Voltage
_____	1.0 V	_____
_____	2.0 V	_____
_____	2.5 V	_____
_____	3.0 V	_____
_____	4.0 V	_____

Use Excel or a similar spreadsheet program to plot your points in a "Scatter Plot".

On your Scatter Plot, add a "Trendline" with "Display Equation on chart" selected.

6. Read the slope of your graph from the Equation displayed on the scatter plot. record the slope, and select the base units (i.e. don't use an S.I. prefix) below.

_____

7. Use Ohm's Law to help you determine the correct base units for the slope of your graph.

   (a) A

   (b) V

   (c) Ω

8. Measure the Emitter voltage of the transistor when the output voltage of your circuit is 4.0 V: _____ V
9. Determine the current using the voltage drop across R_3: _____ mA
10. True/False: The current through R_3 is essentially the same as I_{in}.

    (a) True

    (b) False

Online Homework System

Assignment Worksheet
5/20/22 - 9:35:33 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Intro to Frequency Response

Question 1: (1 point)

In this exercise, you will be accessing audio and video from Moodle. Please ensure you have suitable hardware.

Frequency Response: The Last (op amp) Frontier

In our introduction to the op amp, we said there were some goals designers had in mind when developing a useful operational amplifier:

- differential inputs
- infinite input impedance
- zero output impedance
- infinite gain
- bandwidth from zero to infinity

So far, we've seen that even the cheapest of op amps does a pretty good job of the first four:

- differential inputs allow for inverting, non-inverting, difference, and summing configurations
- input impedances are greater than the resistance of air
- output impedances are less than the resistance of wire
- gains in the hundreds of thousands to millions allow us to reduce the gain with negative feedback, and provide us with a model that says the voltage between the two inputs will be essentially zero whenever the amplifier's output is linear

However, we haven't tackled the bandwidth question. Here, unfortunately, things aren't so rosy. The frequency characteristics of inexpensive op amps are really not that great, so we need to know what their limitations are and we need to come up with design techniques to ensure that the circuit response is at least predictable if not desirable.

Frequency Response Background

Over the past two semesters, you've learned a lot of things related to frequency response, and yet we find that many students have a very tenuous grasp on what that was all about.

- You've learned about complex numbers and applied these to the impedances of inductors and capacitors, learning that the impedance of a capacitor decreases as frequency increases, whereas the impedance of an inductor increases as frequency increases. That means that inductors appear as short circuits to low frequency signals and capacitors appear as shorts to high frequency signals.
- You've learned how to do all sorts of complicated math with resistors, capacitors, and inductors in circuits -- Vectors and Phasors, Laplace Transforms, and Fourier Analysis, all of which are frequency-based (that's the ω or s in all those calculations) and help to explain the effects of electronic components on signals of different frequencies.
- You've combined capacitors with resistors, inductors with resistors, and capacitors with inductors in various voltage divider arrangements that showed how the change in frequency resulted in different output amplitudes (and phases) depending on the frequency of the input signal.
- These various arrangements of capacitors, resistors, and inductors all formed filters -- low pass filters, high pass filters, band pass filters, and even band reject filters. For these filters, you've both mathematically predicted and empirically determined the cut-off frequencies.

But still I find many students can't tell me what a cut-off frequency means or how to use an oscilloscope to find one.

So lets get back to the basics of AC signals and what different frequencies are all about, and then discuss the effects of different filters on signals containing a mixture of frequency components, and also on a single sinewave as its frequency changes.

Listen to the audio recording "Audio Demo on Frequencies", available in Moodle.

What was the highest frequency you could hear? _____ kHz

Listen to the audio recording "Alice Cooper Demo", also available in Moodle. Please don't share this outside the "class" setting for copyright purposes!

Here's a summary:

- A Low Pass Filter (LPF) allows the lower and midrange frequencies (bass guitar, bass drum, human voice) through but removes the higher frequencies (cymbals, hissing vocal sounds like 's')
- A High Pass Filter (HPF) allows the higher and midrange frequencies through but removes the lower frequencies
- A Band Pass Filter (BPF) allows the midrange frequencies (voice, guitar) but removes the lower and higher frequencies
- A Band Reject Filter (BRF) allows both the low and high frequencies through but removes the midrange frequencies

Now, watch the video "Various Filters with Frequency Sweep". https://nait.hosted.panopto.com/Panopto/Pages/Viewer.aspx?id=fb646365-370a-44dd-bfb2-ab8a01786a6e (https://nait.hosted.panopto.com/Panopto/Pages/Viewer.aspx?id=fb646365-370a-44dd-bfb2-ab8a01786a6e)

Match the following:

_____

Question 2: (1 point)

You noticed in the introductory audio and video recordings that filters don't completely block frequencies we want removed. Instead, the amplitude of the unwanted frequencies starts to drop off at some point and keeps dropping as we move further away. Any two people listening to the output of a particular audio filter would have different opinions as to when the volume started dropping and when they consider the output to be "quiet enough" to be filtered out, and different filters will drop off at different rates as the frequency moves away from the starting point.

As a result of these issues, the scholarly community has come up with standardized ways of defining what is referred to as the cutoff frequency, as well as the roll-off rate.

Mathematically, the cutoff frequency, f_c, is defined as the point at which the power of the signal drops to half what it was in the pass band. This results in a few different expressions that all mean the same thing:

$$P_{fc} = \frac{P_{pass}}{2}$$

Since $P=V^2/R$,

$${V_{fc}}^2 = \frac{{V_{pass}}^2}{2}$$

which reduces to the most important empirical version of this formula (i.e. based on measured values):

$$V_{fc} = \frac{V_{pass}}{\sqrt{2}}$$

In decibels, 10log(.5) = 3 dB, so the cutoff frequency happens when the signal drops by 3 dB.

Also, this is the point at which $|X_c| = R$ for a capacitive filter. This results in

$$R = \frac{1}{2\ \pi f_c C}$$

which can be rearranged to the most important theoretical version of this formula (i.e. based on component values):

$$f_c = \frac{1}{2\ \pi RC}$$

The rate at which the voltage decreases past the cutoff frequency is also based upon the reactance of the capacitor. In essence, the resistor and capacitor in a filter form a voltage divider in which the impedance of one of the components, the capacitor changes with frequency. Well past the cutoff frequency, the phase of the complex resultant of the math involved swings almost entirely to the capacitor, so, in rough terms, the output amplitude is dependent on the reactance of the capacitor. For example, an increase in frequency of 10 (a decade) results in a decrease in capacitive reactance to 1/10th, and the output of the filter will change by either an increase of 10x (HPF) or a decrease to 1/10th (LPF). Converting 10 to dB is 20 dB, and 1/10th is -20 dB. Therefore, a circuit with only one capacitor will have a **Rolloff** in the reject band with a magnitude of 20 dB/decade -- rising for a HPF and falling for a LPF.

Question:

A particular low pass filter has a "corner frequency" (cutoff frequency) of 3 kHz. If the amplitude of its output signal is 5 V_p at 1 kHz (that's in the passband), what is the expected amplitude at the cutoff frequency, 3 kHz? _____ V_p

Since this filter has only one capacitor, at what frequency would we expect the signal amplitude to drop by 20 dB from the passband amplitude? _____ kHz.

What would the signal amplitude be at a frequency one decade above the cutoff frequency? _____ mV_p

If the resistor in this filter is 10 kΩ, what must the capacitance be? _____ nF.

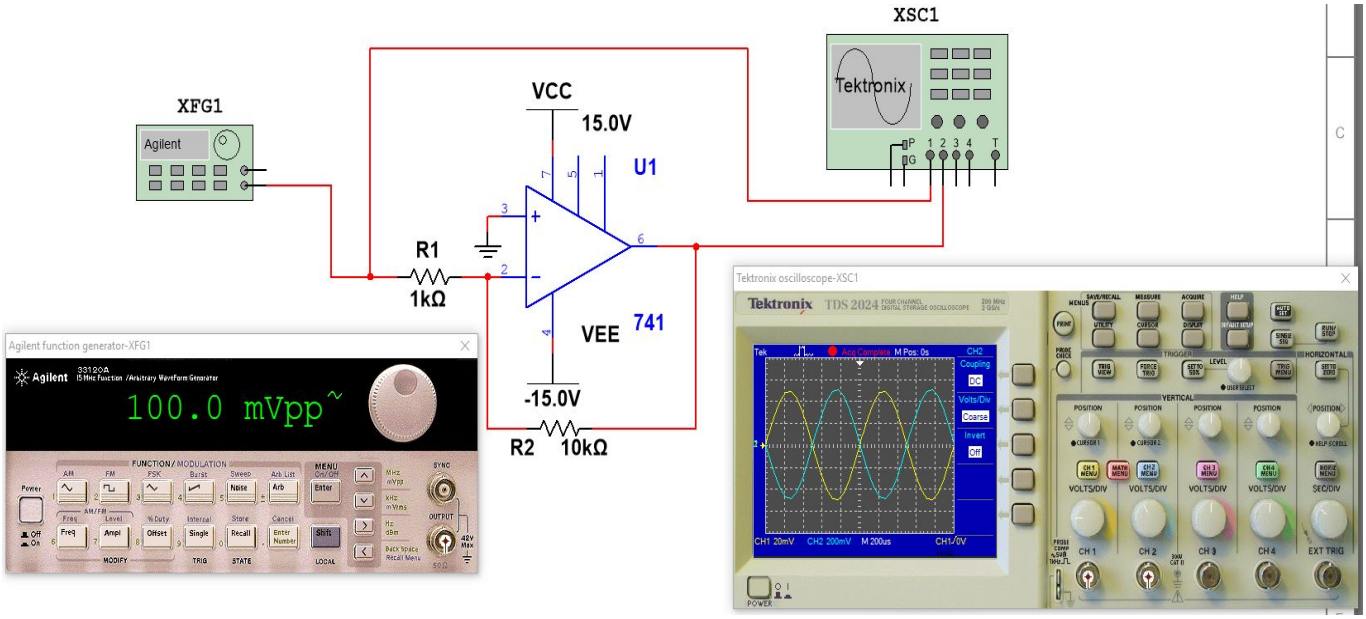
Online Homework System

Assignment Worksheet
4/3/23 - 9:37:11 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Op Amp Frequency Issues and Filters

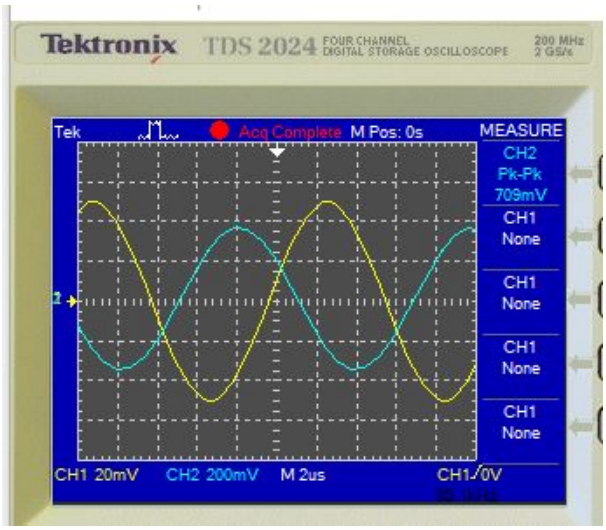
Question 1: (1 point)

The biggest issue with op amps is the problem of frequency limitations. Using Multisim, build the following circuit and test it as follows. the Agilent Function generator is a bit difficult to work with, but we need something we can change the frequency on easily. Set it up to generate a sine wave with an amplitude of 100 mV_{p-p} and a frequency of 1.0 kHz with no DC offset.



1. What is the gain of this amplifier, from the components? _____
2. Measure the output voltage, in V_{p-p}. _____ V_{p-p}
3. What is the gain of this amplifier, from a voltage calculation? _____
4. All op amps have an upper limit to their useful frequency, so they act as Low Pass Filters. Using the output voltage, calculate the magnitude of the amplitude of the output signal you expect to see at the cutoff frequency for this circuit, in mV_{p-p} (don't worry about the phase). _____ mV_{p-p}
5. We refer to the voltage you just calculated as the "target voltage", because we will now increase the frequency until the amplitude drops to this voltage. Do that, and as you increase the frequency, adjust the oscilloscope time base so that the signal stays clearly displayed. Record the frequency when you hit the target voltage. _____ kHz. This is the cutoff frequency.

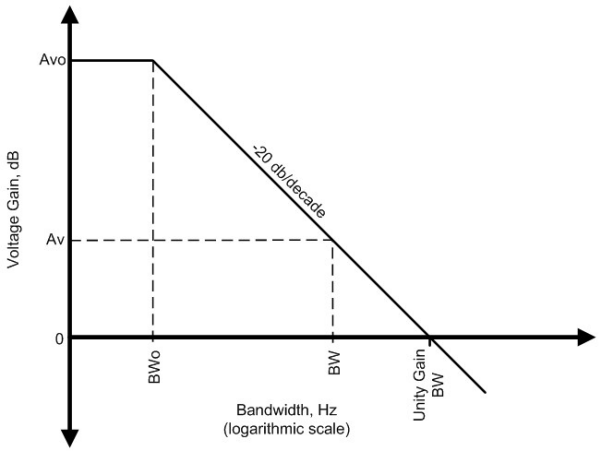
Your oscilloscope display should look something like the following:



Notice two things: First, the amplitude has dropped as closely as I can get it to the target voltage of 707 mV_{p-p}. Second, the output signal is no longer just "inverted" -- it now lags by another 45º from where it started. If we kept going, at very high frequencies it would lag by a full 90º for a single capacitor (that's from the "-j" in all of the frequency-related math that you've done in other courses).

Small Signal Frequency Limitation: Gain-Bandwidth Product

Why does the op amp act like a single-capacitor low pass filter? All high-gain circuits will go into oscillation at some frequency, so the designers of the 741 op amp have deliberately limited the output frequencies so the 741 never reaches that frequency and "goes crazy". As a result, we get the following frequency response curve, generalized for all op amps:



"BWo" is the cutoff frequency built into the device by the manufacturers.

Notice that the graph is "log-log" -- the frequency axis is a logarithmic scale, and the Gain axis is in dB, which is logarithmic.

Also notice that the Rolloff is -20 dB/decade, as expected for a single-capacitor filter.

A key point of this graph is where the line crosses the 'x' axis. At that point, the gain is 0 dB, which, in V/V gain is 1.0, or unity gain. The frequency at this point is called the "Unity Gain Bandwidth". That's the number the manufacturers report in the specification sheet as the Bandwidth. From what we saw earlier, with a Low Pass Filter that has only one capacitor, as the frequency increases by a decade (x10), the voltage decreases by 1/10th (that's the same as -20 dB/decade). In other words, the voltage decrease is always the reciprocal of the increase in frequency. So, as we increase the gain, the bandwidth, BW, decreases proportionately. As a result, the gain multiplied by the bandwidth will always be the same as the Unity Gain Bandwidth. Consequently, the Unity Gain Bandwidth is also called the Gain Bandwidth Product.

From this, we can come up with an important formula to tell us the limitations of our op amp:

BW = GBP/Av

6. From the circuit you built above, what must the Gain-Bandwidth Product (GBP) of the op amp be? _____ kHz.

On the data sheet for the 741A op amp, the "Bandwidth" is listed as 0.437 MHz. This is the Unity Gain Bandwidth or the Gain Bandwidth Product. Our result is about double what the spec sheet says, which isn't surprising -- they're giving us the worst allowable value, and they will try to aim for something considerably better.

7. Using the specified 437 kHz, what would the bandwidth limit be for an inverting amplifier with Rf = 56 kΩ and Ri = 10 k Ω? _____ kHz
8. What is the maximum gain for a 741-based amplifier that needs a bandwidth of 100 kHz? _____

As you can see, this seriously limits the usable gain and bandwidth of circuits using "cheap" op amps like the 741. We can, to some extent, overcome this limitation by cascading amplifiers together, because the overall gain is the product of the two amplifiers. However, when we do that, we also introduce a further limitation to the bandwidth. If we have multiple stages with the same bandwidth, the resulting overall bandwidth is reduced to

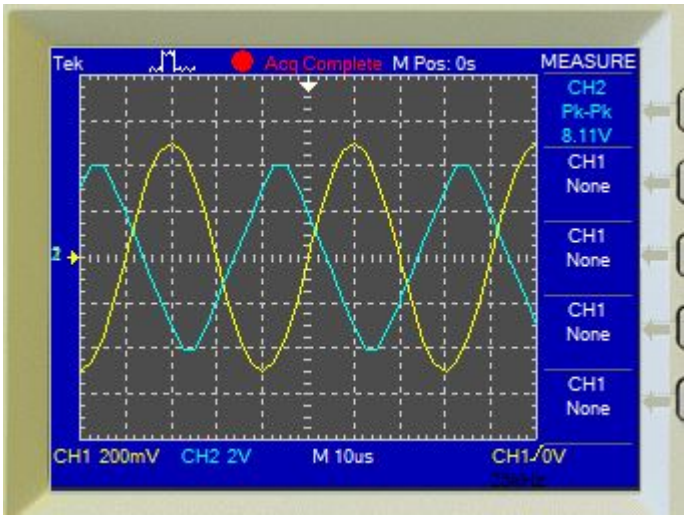
$$BW_{circuit} = BW_{stage}\sqrt{2^{\frac{1}{n}} - 1}$$

where "n" is the number of stages.

9. If we want to use two 741 op amps to get an overall bandwidth of 100 kHz, what overall gain could we get? First, use the formula to determine the Stage Bandwidth: _____ kHz. Now, use the GBP to get a single stage gain: _____ Finally, multiply the two gains together to get the overall gain: _____ At least, that's an improvement!

Large Signal Frequency Limitations: Slew Rate

If you think that the small-signal limitations were an issue, it's only part of the problem. Using the circuit above, set up the function generator to produce a 1.0 $V_{p\text{-}p}$ sine wave at 1.0 kHz. After adjusting your oscilloscope settings, you should see that the output is still 10x the input, and is an inverted sine wave. Now, set the frequency to 25 kHz. You should now be seeing something like this:



What happened to our nice sine wave?!?

The problem we're seeing arises from the time it takes for a signal to pass through the op amp. Because of all the circuitry in the op amp, the rate of change of the output voltage is limited. Whenever the input signal requires a more rapid change than this maximum, the op amp will ignore that request and continue on its merry way at its maximum rate of change. This rate of change is called the "Slew Rate".

Try changing the input signal in Multisim to a square wave -- same result as the sine wave! Try a triangle wave input -- same result! When we hit the slew rate, the op amp turns everything into triangles. We call this Triangular Distortion, and the results are not acceptable.

10. Set the function generator back to a square wave, and stretch out one of the sloping edges until it covers the oscilloscope screen. Determine the coordinates of two points from the screen, and calculate the slope using the base SI units for voltage and time. _____ V/s
11. This is usually reported in V/μs: _____ V/μs

The 741 op amp spec sheet reports this as 0.3 V/μs, so our simulated op amp is slightly better.

For those of you who are interested in the math involved in coming up with the following formula, it's just simple calculus: The instantaneous slope of a function is its derivative, and the greatest slope for a sine wave is at its zero crossing point. Simple manipulation of the derivative for a sine wave tells us the maximum slope, or the Slew Rate, is $2\pi f V_p$. Since the maximum rate of change of a sinewave depends on the amplitude of the sine wave, we call the limitation based on slew rate the **Power Bandwidth**, f_{PBW}:

$$f_{PBW} = \frac{SR}{2\ \pi V_p}$$

12. If the slew rate for our circuit is 0.5 V/μs and the output signal amplitude is 5 V_p, what is the usable power bandwidth? _____ kHz
13. In Multisim, make sure the input is a sine wave, and slowly reduce the frequency until you see the last indication of Triangular Distortion disappear -- in other words, when the output is a sine wave again. _____ kHz. This is the usable Power Bandwidth of the circuit.
14. Set your function generator back to 25 kHz. What is the maximum amplitude that would allow us to have a power bandwidth of 25 kHz? _____ V_p or _____ V_{p-p} What input amplitude would produce this output amplitude? _____ mV_{p-p} Set your function generator output to this value, and verify that the output is now sinusoidal.
    (a) True
    (b) False

So, when it comes to op amps, we need to consider two things:

- Small Signal Bandwidth, based on the Gain Bandwidth Product,
- Power Bandwidth, based on the Slew Rate

The smaller of these two results defines the usable bandwidth of our circuit.

Question 2: (1 point)

The frequency limitations of the op amp turn all op amp circuits into low pass filters. However, when it comes to controlling frequency response, we don't usually want to rely on the amplifier's internal characteristics -- we want to build our own filters with predictable characteristics.

When it comes to filters, we use the term "Passive Filter" to refer to a filter made using just capacitors, resistors, and inductors. We use the term "Active Filter" to refer to any filter that uses op amps or transistors as well. We'll stick to op amp circuits in this course.

The simplest Active Filters add only one capacitor to the inverting amplifier configuration we've been using.

Single-Pole Low-Pass Filter

Add a 15 nF in parallel with R2 in your Multisim circuit. Set your function generator to produce a sine wave 500 mV_{p-p} at a frequency of 100 Hz.

1. Measure the output voltage, and from this calculate the "target voltage" for the cutoff frequency. _____ V_{p-p}
2. Now, increase the frequency until you hit the target voltage. Record the cutoff frequency: _____ kHz.
3. Given that cutoff frequencies are always based on the formula $f_c=1/(2\pi RC)$, which of the two resistors works with the capacitor to produce this cutoff frequency?

   (a) Ri

   (b) Rf

Some of you may be wondering why we put the capacitor in parallel with Rf instead of putting it from R1 to ground, the way you did when you made passive filters last semester. That won't work for an inverting op amp configuration, because, due to the virtual short, the inverting pin is at zero volts, so a capacitor connected here would have zero volts at both ends and would have no effect on the signal! So, for a simple active low-pass filter, the cutoff frequency can be predicted using

$$f_c = \frac{1}{2\ \pi R_f C}$$

Single Pole High-Pass Filter

Move the capacitor so that it is in series with Ri instead. It doesn't matter which side, but we usually put it next to the inverting pin. Notice that having a capacitor in series with the input means that DC would be blocked. That's a quick way to determine that this is a High Pass Filter, since DC is the lowest frequency possible, so blocking DC means blocking low frequencies and passing high frequencies.

Set the function generator initially to produce a sine wave 500 mV_{p-p} initially at 30 kHz.

4. Again, measure the output voltage and from this calculate the "target voltage" for the cutoff frequency _____ V_{p-p}
5. This time, DECREASE the frequency until you hit the target voltage, since the pass band for a HPF is ABOVE the cutoff frequency. Record the cutoff frequency. _____ kHz
6. Again, since cutoff frequencies are always based on a resistor and a capacitor, which of the two resistors works with the capacitor to product this cutoff frequency?

   (a) Ri

   (b) Rf

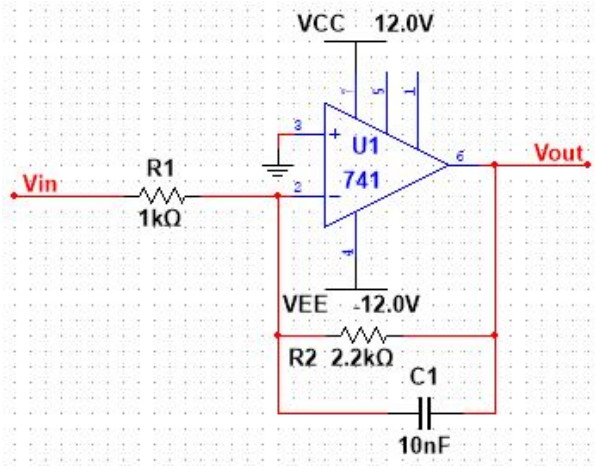
So, for a simple active HPF, the cutoff frequency can be predicted using

$$f_c = \frac{1}{2\ \pi R_i C}$$

For all filters, if the signal is within the pass-band, the capacitor can be ignored so that the rest of the circuit can be treated simply as an amplifier. So, for both of these circuits as you have seen, the gain in the pass band is just

$$A_v = -\frac{R_f}{R_i}$$

Worked Examples



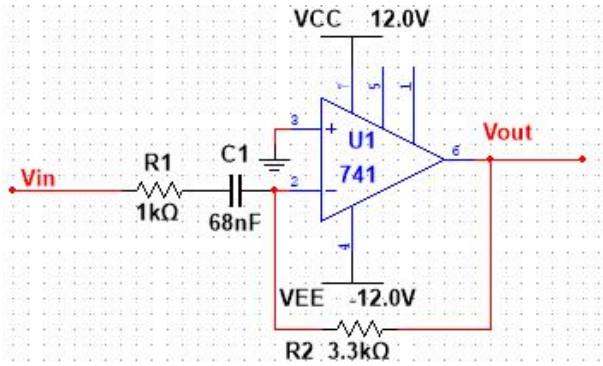
Quick analysis: this is an inverting amplifier, and the capacitor in parallel with the feedback resistor makes it a Low-Pass Filter (LPF).

Its passband gain would be -2.2kΩ/1.0kΩ = -2.2

The predicted cutoff frequency would be 1/(2*π*R_f*C) = 7.23 kHz.

If the input signal was a sinewave with an amplitude of 250 mV_p:

- at 700 Hz (about a decade inside the passband, which is from 0 Hz to 7.23 kHz) the output amplitude would be -2.2*250 mV_p = 550 mV_p, inverted
- at 7.23 kHz (the cut-off frequency) the output amplitude would be 550 mV_p/ sqrt(2) = 389 mV_p
- at 72.3 kHz (one decade past the cut-off frequency) the output amplitude would be 550 mV_p/10 = 55 mV_p
- at 14.26 kHz (one octave past the cut-off frequency) the output amplitude would be 550 mV_p/2 = 275 mV_p
- to determine the cut-off frequency empirically:
    - set the frequency to about 700 Hz (a decade below the expected cut-off frequency)
    - measure the output voltage, $V_{out(pass)}$
    - determine the target voltage: V_{fc} = $V_{out(pass)}$/sqrt(2)
    - INCREASE the frequency until the amplitude drops to V_{fc}
    - record the frequency as f_c



Quick analysis: this is an inverting amplifier, and the capacitor in series with the input resistor makes it a High Pass Filter (HPF).

Its passband gain would be -3.3kΩ/1kΩ = -3.3

The predicted cut-off frequency would be 1/(2*π*R_i*C) = 2.34 kHz

If the input signal was a sinewave with an amplitude of 1.0 V_p:

- at 23 kHz (about a decade within the passband, which is 2.34 kHz and up) the output amplitude would be -3.3*1.0 V_p = 3.3 V_p, inverted
- at 2.34 kHz (the cut-off frequency) the amplitude would be 3.3 V_p/sqrt(2) = 2.33 V_p
- at 234 Hz (one decade before the cut-off frequency) the amplitude would be 330 mV_p (one tenth)
- at 1.17 kHz (one octave before the cut-off frequency) the amplitude would be 1.65 V_p (one half)
- to determine the cut-off frequency empirically:
    - set the frequency to 23 kHz (about a decade within the pass-band)
    - measure $V_{out(pass)}$
    - determine the target voltage from V_{fc} = $V_{out(pass)}$/sqrt(2)
    - DECREASE the frequency until the voltage drops to the target voltage, V_{fc}

- record the frequency as f_c

Multi-Pole Butterworth Sallen-Key Filters

The problem with the circuits we've designed is that they only have a 20 dB/decade rolloff. This means that they don't very effectively remove frequency components close to the cutoff frequency. To improve on this, we need to introduce more capacitors. At a given frequency, having additional R-C pairs increases the rolloff by

20 dB/decade per capacitor

also known as

20 dB/decade per pole.

The term "pole" comes from an infinitely high spike that shows up in the 3-D impedance graph for a capacitor in a filter.

The problem with just adding more R-C pairs is that they cause instability in the circuit. Many different active filter designs have been made that overcome this problem. We'll just teach you one well-known one that produces very dependable results -- one designed by two people whose last names were Sallen and Key. The Sallen-Key Filter is also known as the VCVS Filter (Voltage-Controlled Voltage Source).

Having op amps in a circuit means that, unless things are done just right, the circuit could go into oscillation. What we're looking for in this course is what's called a "maximally flat" response, or a Butterworth response. With this arrangement, the output voltage stays constant until as close as possible to the cutoff frequency, then rounds down in the shape expected for a single capacitor filter before dropping at the predicted rolloff rate. These filters are called "Critically Damped" as opposed to "Underdamped" filters, which oscillate a bit near the cutoff frequency, or "Overdamped" filters which start to round down well before the cutoff frequency.

For a Butterworth Sallen-Key Filter, the required gains are defined by a group of S-Domain polynomials called the "Normalized Butterworth Polynomials", shown below.

n	**Normalized Butterworth Polynomial**
1	$s+1$
2	$s^2+1.414s+1$
3	$(s+1)(s^2+s+1)$
4	$(s^2+0.765s+1)(s^2+1.848s+1)$
5	$(s+1)(s^2+0.618s+1)(s^2+1.618s+1)$
6	$(s^2+0.518s+1)(s^2+1.414s+1)(s^2+1.932s+1)$

In this table, the monomials (s+1) all represent single-pole filter components. The binomials all represent two-pole filter components, which we will look at soon. The single pole components can have any gain we want them to have. However, the binomial components must have a voltage gain, A_v, that is equal to 3 minus the middle term coefficient. So, for example, the gains required for the three parts of a 5-pole filter would be

Stage 1: X (any gain)

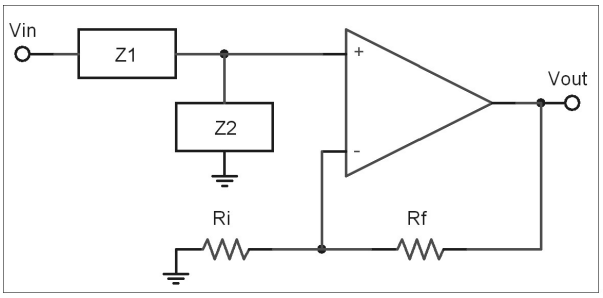
Stage 2: 2.382 (that's from 3 - 0.618)

Stage 3: 1.382 (that's from 3 - 1.618)

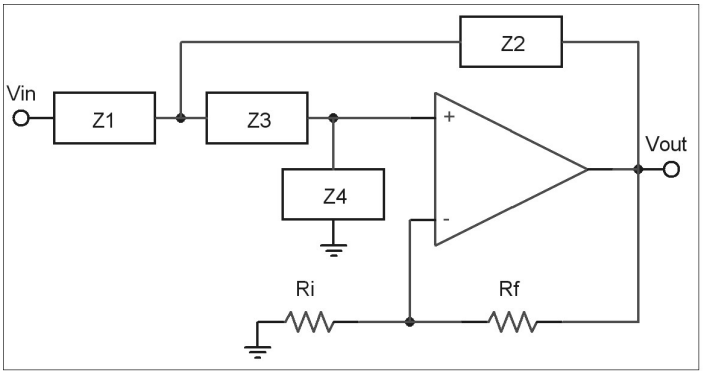
The last column in this table (which also appears in this course's formula sheet) shows the resulting gains for multi-pole filters up to six poles.

n	Normalized Butterworth Polynomial	Stage Gains
1	$s+1$	(*x*)
2	$s^2+1.414s+1$	(1.586)
3	$(s+1)(s^2+s+1)$	(*x*)(2.000)
4	$(s^2+0.765s+1)(s^2+1.848s+1)$	(2.235)(1.152)
5	$(s+1)(s^2+0.618s+1)(s^2+1.618s+1)$	(*x*)(2.382)(1.382)
6	$(s^2+0.518s+1)(s^2+1.414s+1)(s^2+1.932s+1)$	(2.482)(1.586)(1.068)

Now, for the actual circuits that embody these polynomials.



-- Single-Pole Component



-- Two-Pole Component

In each case, the "Z" elements are either resistors or capacitors. Z1 and Z3 have to be the same type of component, and Z2 and Z4 have to be the other type of component. If the odd-numbered ones are resistors, the result is a LPF. If the odd-numbered ones are capacitors, the result is a HPF.

If all the capacitors and all the resistors in the filter-related feedback (the Zs) are the same, the cutoff frequency is the usual:

$$f_c = \frac{1}{2\ \pi RC}$$

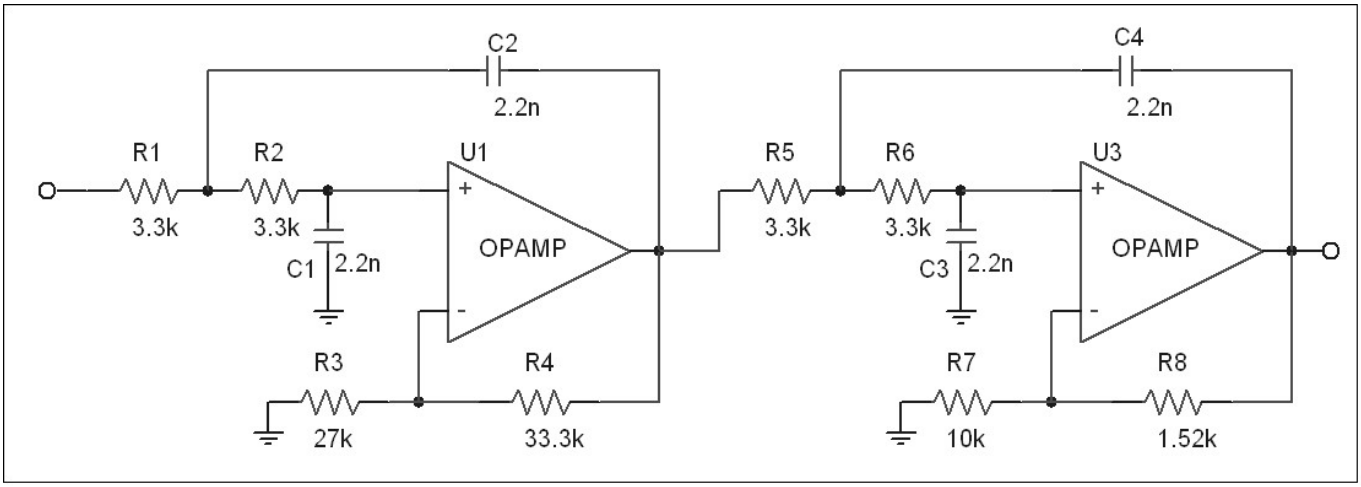
Lucky for you, we won't ever use combinations of different resistors and capacitors in the filter-related feedback.

In the negative feedback component, the gain is what you would expect for a non-inverting amplifier:

$$A_v = \frac{R_f}{R_i} + 1$$

The big limitation, though, is that these gains must match the ones in the table in order to produce a Butterworth, or maximally flat, characteristic.

Here's an example:



7. What type of filter is this?

(a) Low Pass

(b) High Pass

(c) Band Pass

(d) Band Reject

8. How many poles does it have (also known as the "order" of the filter)?

_____

9. What is the expected rolloff past the cutoff frequency?

_____ dB/decade

10. What is the cutoff frequency? _____ kHz
11. What is the pass band gain for the first stage? _____
12. What should it be, from the table? _____
13. What is the pass band gain for the second stage? _____
14. What should it be? _____

These gains are pretty close to optimal, so this filter should be maximally-flat.

15. What is the overall passband gain of the circuit? _____

This last question points out one of the limitations of even-ordered filters -- their overall gain can't be played with. However, the odd-ordered filters have a single-pole stage, so the gain can be set to what you wish it to be.

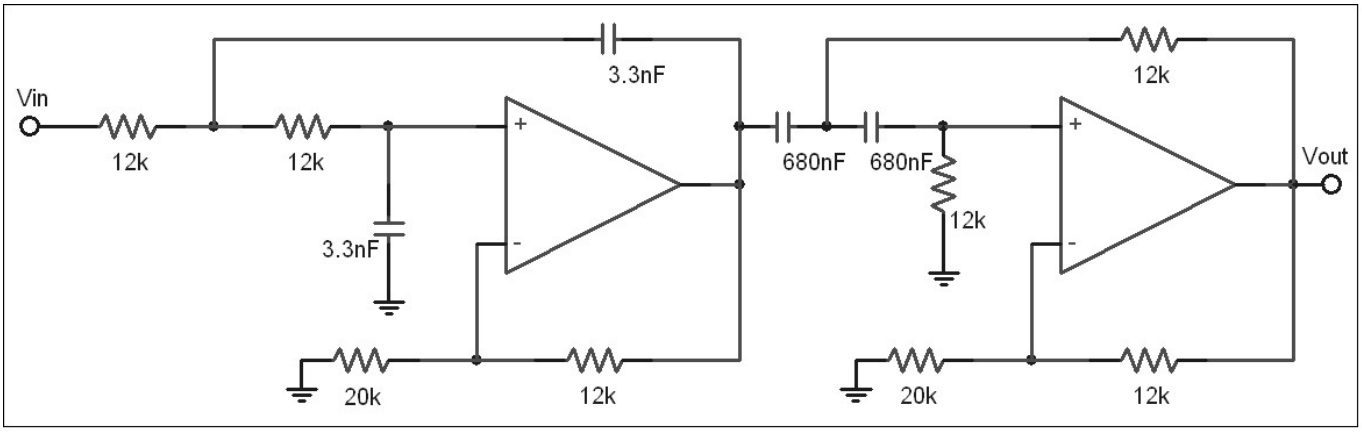
Band Pass and Band Reject filters

A Band Pass Filter is made by putting a HPF in SERIES with a LPF, and setting the cutoff frequency of the LPF to be HIGHER than the cutoff frequency of the HPF. That way, there will be a pass band of frequencies between the two cutoffs.

A Band Reject Filter is made by adding the outputs of a HPF filter and a LPF filter using a summing amplifier. That way, the two pieces of the spectrum that you want are joined together in the final output signal.

It's important to realize that you can't just add up the capacitors to determine how many poles a BPF or BRF have, since the two components of the filter are active at different frequencies.

Here's an example.



16. If the cutoff frequencies are chosen properly, what kind of filter is this?

    (a) LPF

    (b) HPF

    (c) BPF

    (d) BRF

17. What is the cutoff frequency for the first stage? _____ kHz
18. What is the cutoff frequency for the second stage? _____ Hz
19. The cutoff frequencies are chosen to allow a range of pass band frequencies.
    (a) True
    (b) False

20. How many poles are there in the LPF component? _____
21. How many poles are there in the HPF component? _____
22. What is the expected rolloff for the filters in this circuit? _____ dB/decade
23. Notice that the two components have the same gain-setting resistors. What is the gain of each section? _____
24. What should the gain be, from the table? _____
25. The gains should be close enough to be maximally-flat, or Butterworth.
26. What is the overall gain of the circuit? _____

That's a lot of information! Hard as it may be to believe, you've only scratched the surface of the topic of frequency response. These are the most important things to remember:

- Filters remove, or at least attenuate, signals outside of their pass bands
- Low Pass Filters remove high frequencies
- High Pass Filters remove low frequencies
- Band Pass Filters remove low and high frequencies, passing a "mid" band
- Band Reject Filters keep low and high frequencies, rejecting a "mid" band
- The cutoff frequency is found empirically by changing the frequency until the output signal drops to half power, or V/sqrt(2)
- The cutoff frequency can be predicted using $f_c=1/(2\pi RC)$
- In the rejected region, the amplitude drops off at 20 dB/decade per pole
- Sallen-Key filter stage gains must match the table of polynomials for maximally-flat or Butterworth response

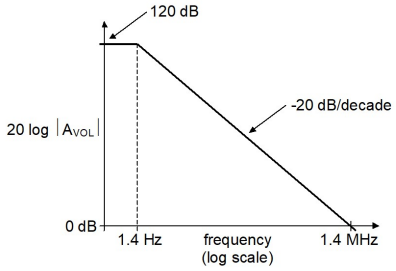
Online Homework System

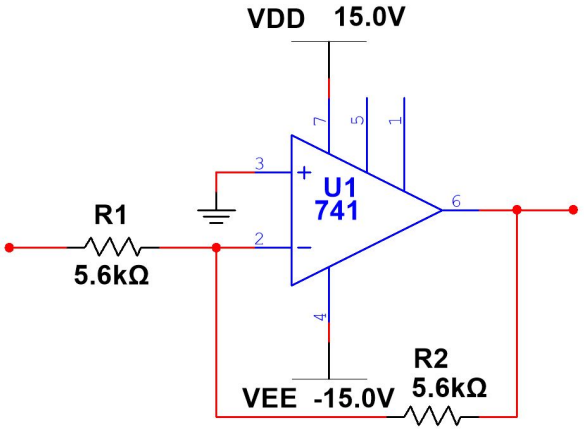
Assignment Worksheet
5/31/21 - 2:31:04 PM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA17 Active Filters Quiz

Question 1: (2 points)

Use the open-gain magnitude Bode plot and the schematic circuit below to answer the questions that follow.



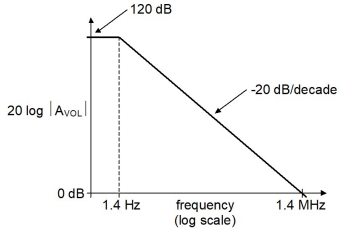


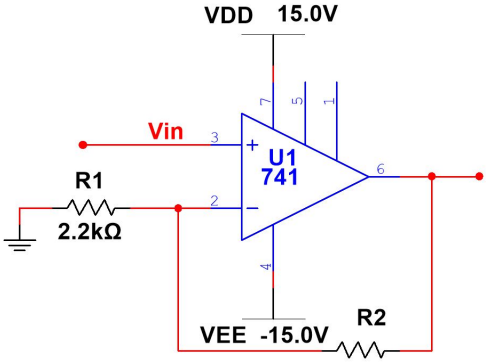
What is the gain of this amplifier? Include the appropriate sign to indicate polarity. _____

What is the small-signal bandwidth for this amplifier? _____ MHz.

Question 2: (2 points)

Use the open-gain magnitude Bode plot and the schematic shown below to answer the questions that follow.



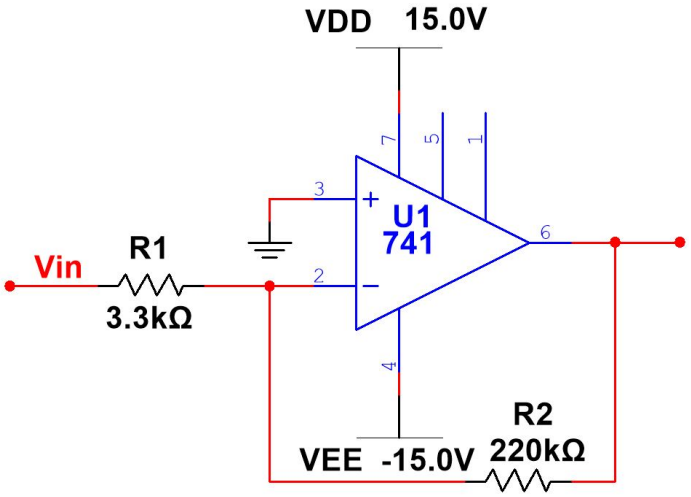


If this amplifier is to have a small-signal bandwidth of at least 350 kHz, what is its maximum gain? _____ .

What would be the maximum theoretical value for R2 to provide the maximum gain calculated above? _____ kΩ.

Question 3: (2 points)

Use the schematic shown below to answer the question that follows.



What is the gain of this amplifier? _____ .

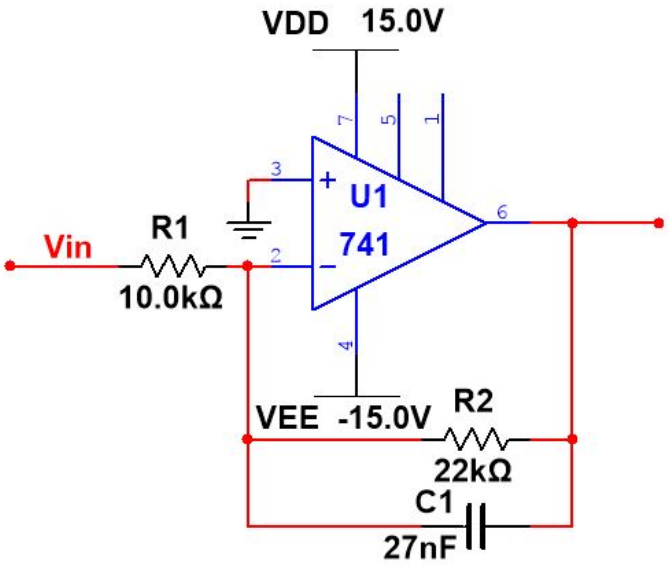
If this amplifier is to have a small-signal bandwidth of 20 kHz, what is the minimum gain-bandwidth product, GBP, needed when choosing an op amp? _____ MHz.

Question 4: (1 point)

A certain op amp has a slew rate of 3.5 V/us. The output signal is intended to swing between +13.5 V and -13.5 V. What is the power bandwidth of this circuit? _____ kHz.

Question 5: (2 points)

Use the following schematic diagram to answer the questions that follow.



This circuit is a

(a) Band Reject Filter

(b) Low Pass Filter

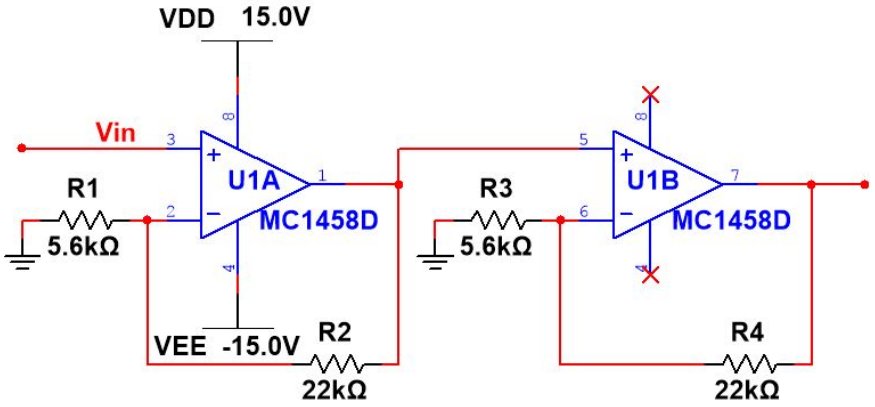
(c) High Pass Filter

(d) Band Pass Filter

What is the cut-off frequency for this filter? _____ Hz.

Question 6: (3 points)

For the following circuit, assume that the gain-bandwidth product of the 1458 op amp is 680 kHz. What is the small-signal bandwidth of this circuit? Include appropriate units.



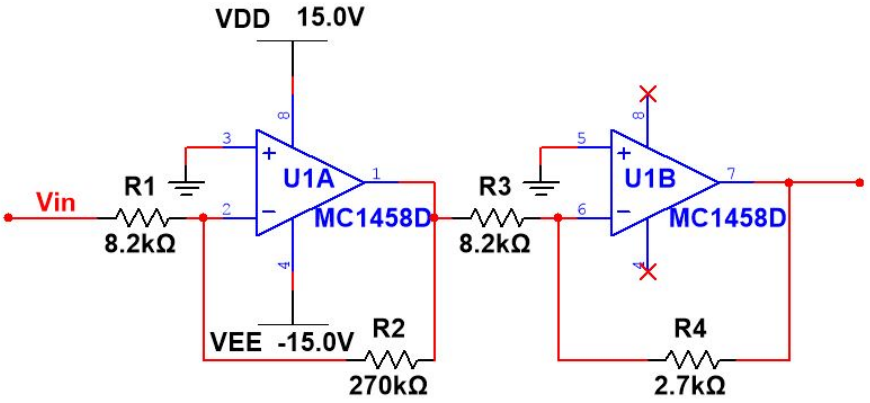
What is the gain of the first stage? _____

What is the gain of the second stage? _____

What is the small-signal bandwidth for this circuit? _____ kHz.

Question 7: (3 points)

For the following circuit, assume that the gain-bandwidth product of the 1458 op amp is 680 kHz. What is the small-signal bandwidth of this circuit? Include appropriate units.



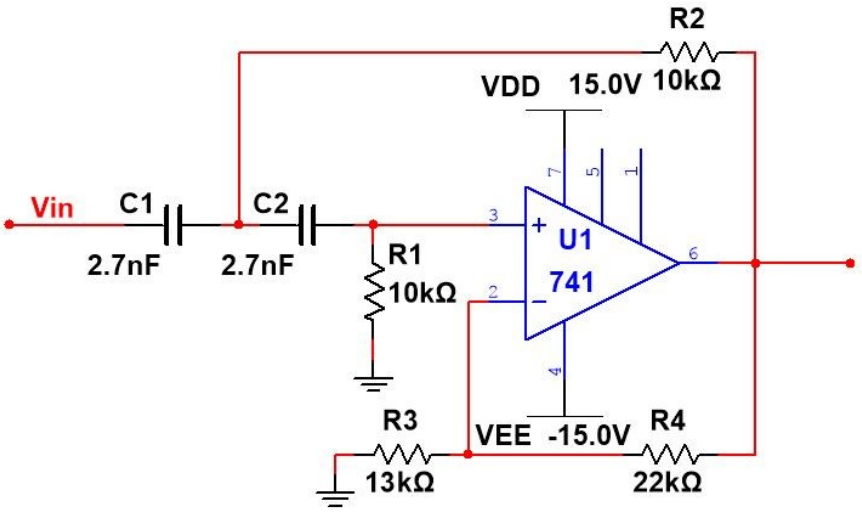
What is the gain of the first stage? _____

What is the gain of the second stage? _____

What is the small signal bandwidth of this circuit? _____ kHz.

Question 8: (5 points)

Use the schematic diagram below to answer the questions that follow.



This circuit is a

(a) Band Pass Filter

(b) High Pass Filter

(c) Band Reject Filter

(d) Low Pass Filter

What is the gain of this circuit? _____

The gain of this circuit is suitable to produce a Butterworth characteristic.

(a) True

(b) False

What is the cut-off frequency for this circuit? _____ kHz

Past the cutoff frequency, the gain would be expected to change by _____ dB/decade.

Online Homework System

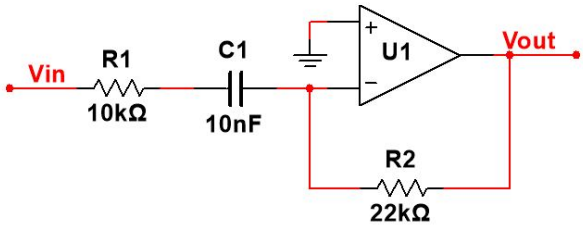
Assignment Worksheet
11/11/22 - 7:57:22 PM MST

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Project 6 Op Amps and Filtering

Question 1: (50 points)

Single-Pole Active Filter

Answer the following questions related to the partial schematic below.



This circuit is:

(a) LPF

(b) HPF

(c) BPF

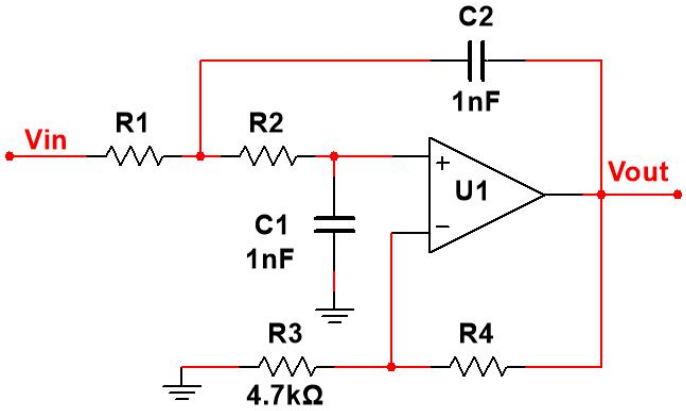
(d) BRF

Its cutoff frequency is _____ kHz

What is its gain in the passband? (Don't forget polarity.) _____

Sallen-Key Active Filter

Answer the following questions for the partial schematic below.



If the cut-off frequency is to be 2.341 kHz, what 10% resistor value should both R_1 and R_2 be? _____ kΩ

Determine the ideal value for R_4 to make this a "maximally flat" filter. _____ kΩ

Pick a suitable 10% resistor value for R_4. _____ kΩ

Simulation

Build and test the Sallen-Key filter above using Multisim.

- Use a 741 op amp, and power it from +12V and -12 V

- Use an Agilent Function Generator (available toward the bottom of the instruments on the right side of the screen), as this device allows you to dial in the frequency during simulation
    - The actual "Output" is the lower of the two connections -- the one above is a "Sync" output, and will always be a 2.4 V square wave regardless of the settings you've selected; you don't need a "ground" connection to the function generator -- it assumes a common earth ground
    - Use a Sine wave with an amplitude of 1.0 V_p, and start at a frequency of 200 Hz.
- If in doubt, check your resistor values with your instructor
- Use a Tektronix Oscilloscope to display and measure V_{in} and V_{out}

Make the following measurements and calculations for the 200 Hz signal, which should be well within the pass-band:

V_{in} = _____ V_p, V_{out} = _____ V_p, A_v = _____ _____

Calculate the target output voltage expected at the cut-off frequency: _____ V_p

Adjust the frequency (make sure you know whether to increase or decrease the frequency based on the type of filter -- maybe sketch a Bode plot) until the amplitude drops to the target voltage, and record the cutoff frequency here: _____ kHz.

For a grade out of two marks, upload a screenshot of your circuit and the oscilloscope screen displaying the input and output signals at the cut-off frequency. Document Upload (Direct)

Increase the frequency to 10x the cutoff frequency (i.e. up by one decade). Adjust the oscilloscope to display the remaining signal as well as you can, and record the amplitude now, in millivolts: _____ mV. Calculate the drop in dB using $20\ \log\left(\frac{V_{1\ decade}}{V_{passband}}\right)$

This drop is closest to _____

Frequency Limitations of the 741 Op Amp

From the data sheet, what is the "Minimum Bandwidth" (GBP) of the 741A op amp, in kHz? _____ kHz

In Multisim, create a unity gain buffer using a 741 op amp and +/- 12 V_{DC} for power. Insert a screen capture of your completed schematic here for one mark. Document Upload (Direct)

From the data sheet, what is the Minimum Slew Rate for the 741A Op Amp, in V/s? _____ V/s

If a particular circuit using a 741A op amp is expected to generate a 5.0 V_p output, determine the expected power bandwidth for this circuit. _____ kHz

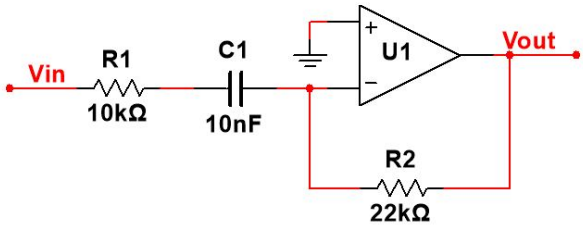
You will need the values predicted in this Pre-Lab when you do the Lab Activity. Copy them before moving on to the next page, as you will not be able to return to this page.

You have now finished the Preparation and Simulation components of this project. Move on to the Build and Test section. Don't "Submit" yet!

Question 2: (50 points)

Single-Pole Active Filter

On your breadboard, use a 741 Op Amp and +/- 12 V power to build a completed version of the single-pole filter shown in the partial schematic below.



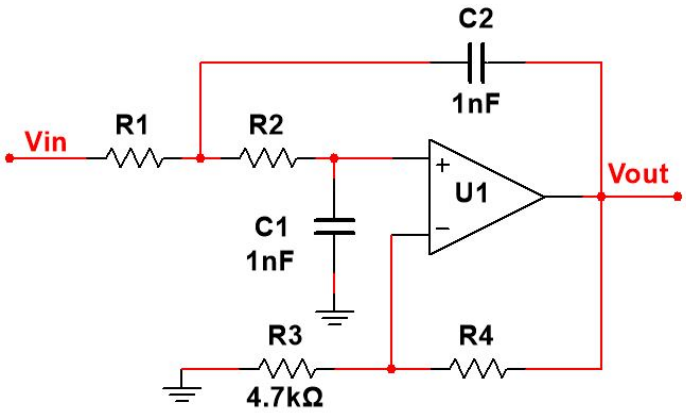
1. Set the function generator initially to produce a 1.0 V_p (not V_{p-p}) sine wave at a frequency approximately 10x the expected cutoff frequency from the Pre-Lab. This should be well within the passband for this filter. Determine the passband gain, including the polarity: _____

Follow the appropriate procedure to find the cut-off frequency (Hint: for this kind of filter, should you increase or decrease the frequency?)

2. What should the voltage be at the cut-off frequency (i.e. what is the target voltage)? _____ V_p
3. Record the empirically-determined cut-off frequency here. _____ kHz
4. Ask your instructor to give you a grade out of three marks, based upon your oscilloscope settings and the measurements used in the process above. _____

Sallen-Key Multi-Pole Filter

On your breadboard, use a 741 op amp and the +/-12 V Power to build the partially-complete Sallen-Key Filter shown below. Use 68 k Ω resistors for R1 and R2; use 2.7 kΩ for R4.



Set up an input signal as a 1.0 V_p sine wave set initially to 200 Hz. Again, this should be well within the pass-band for this filter, since we designed it for a cut-off frequency of 2.341 kHz.

5. Use the oscilloscope to observe the input and output signals. Determine the pass-band gain. _____
6. Use the appropriate procedure to determine the cut-off frequency. _____ kHz
7. Now, set the function generator to 10x the cut-off frequency (i.e. one decade into the reject band). Adjust your oscilloscope to observe the signals appropriately, and determine the gain at this frequency. It should be very small. Do the following calculation to convert this to decibels (this should give you the roll-off in dB/decade for this filter):

$$Rolloff = 20 \log\left(\frac{Av_{1\ decade}}{Av_{passband}}\right) = \_\_\_\_\_$$

Frequency Limitations of the 741 Op Amp

On your breadboard, build the unity gain 741 circuit you designed in the Pre-Lab.

Set the function generator up initially as follows:

- Sine wave
- 1.0 kHz
- 200 mV_p
- No offset

8. Use Oscilloscope Channel 1 to display the input signal and Channel 2 to display the output signal. Using the Amplitude measurements for the input and output signals, determine the gain of this amplifier. _____

Since the op amp by itself acts as a LPF, slowly increase the frequency until you find the cut-off frequency. Don't be surprised if it is much higher than you predicted in the Pre-Lab -- the data sheet is providing the "worst case".

You will need to keep the signal displayed properly as you increase the frequency by adjusting the timebase of your oscilloscope periodically.

You may notice a bit of triangular distortion close to the cutoff frequency -- just ignore this, as the peaks and troughs should still be undistorted.

9. Record the cutoff frequency here. _____ kHz
10. Set the function generator to produce a 5.0 V_p 1.0 kHz sine wave signal. Now, slowly increase the frequency until you see the expected distortion on the output generated by exceeding the slew rate, and back off the frequency until the distortion just disappears. Record the Power Bandwidth here. _____ kHz.
11. Ask your instructor to check your work for a grade out of three marks. _____

Again, don't be surprised if this is much higher than your prediction in the Pre-Lab.

You have been provided with more detailed instructions than you would receive on an exam. Make sure you know the process for determining both the Small-Signal Bandwidth and the Power Bandwidth!

You have now completed this Project. Once you submit your work, you will not be able to return to any of these questions!

Online Homework System

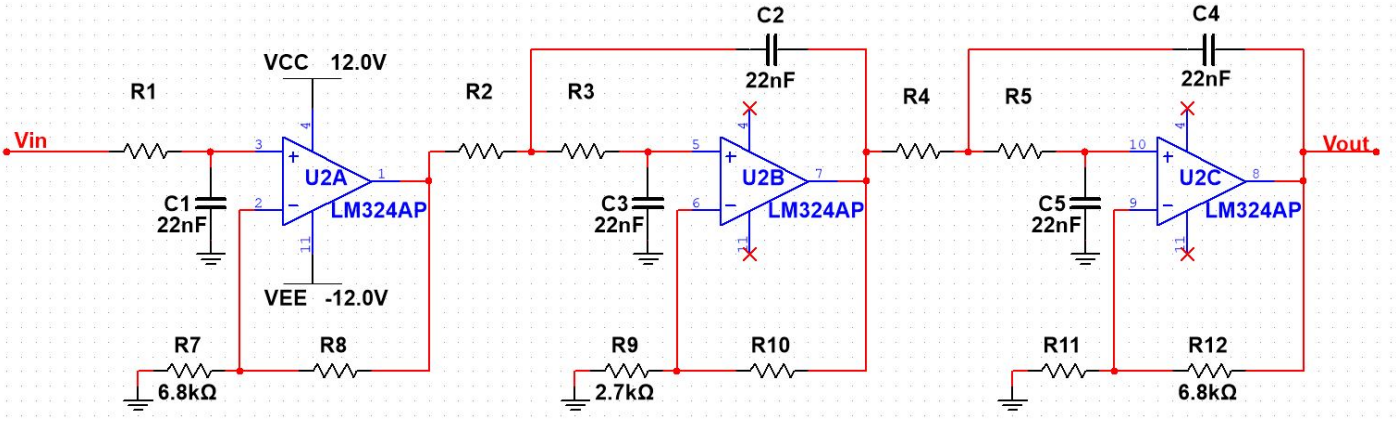
Assignment Worksheet
11/30/22 - 2:12:03 PM MST

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Project 7 5-Pole Filter and R2R DAC

Question 1: (50 points)

Five-Pole Filter (with Simulation)

Consider the following partially-completed schematic diagram when answering the questions below.



1. This five-pole filter is

   (a) Low Pass

   (b) Band Reject

   (c) High Pass

   (d) Band Pass

2. What rolloff is expected for this circuit past the cutoff frequency?

   (a) -20 dB/decade

   (b) -40 dB/decade

   (c) -60 dB/decade

   (d) -80 dB/decade

   (e) -100 dB/decade

   (f) -120 dB/decade

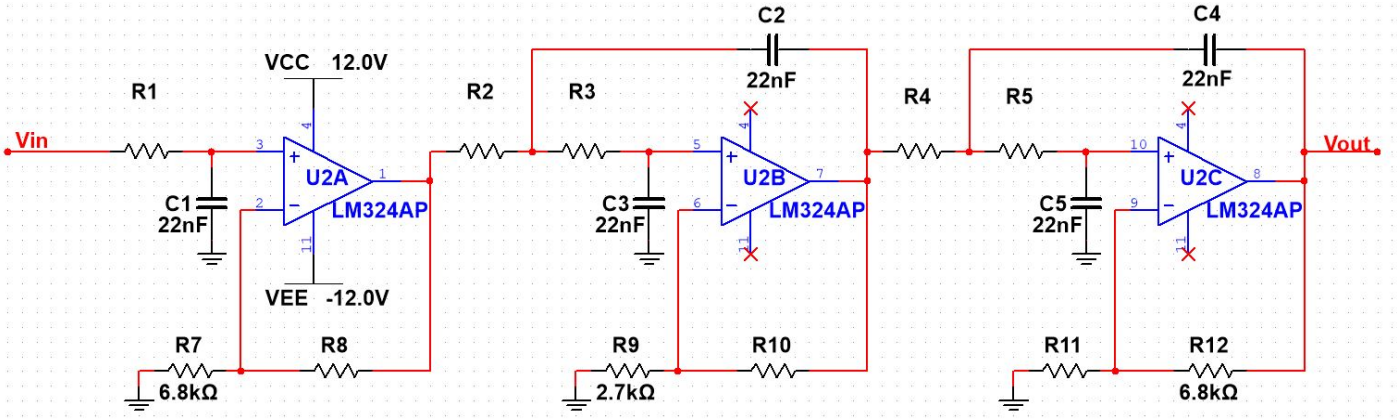
3. The intent is to design the filter to have a cutoff frequency of approximately 2.5 kHz. What would be the ideal resistance for the R-C filter resistors, in kiloohms? (Don't pick a standard resistor value yet.) _____ kΩ
4. Pick the **closest** standard 10% resistor value, to be used for R1, R2, R3, R4, and R5: _____ kΩ
5. With your chosen value, calculate the theoretical cutoff frequency, in kilohertz: _____ kHz
6. From the Butterworth Filter table, what gains are expected for the second and third op amps? _____ and _____

7. From the gains specified in the table, calculate the ideal resistances for R10 and R11 in kiloohms (Don't pick standard 10% resistor values yet.): R10 = _____ kΩ and R11 = _____ kΩ.
8. Pick the **closest** 10% standard resistor values to the ideal resistances, in kiloohms: R10 = _____ kΩ and R11 = _____ kΩ.
9. With your chosen resistors, calculate the theoretical gains of the second and third amplifier stages: $A_{v(U2B)}$ = _____ and $A_{v(U2C)}$ = _____ .
10. The overall passband gain for this circuit is intended to be 5.00. Based upon the theoretical gains of the last two stages, what should the gain of the first stage be? _____
11. Based upon the calculated gain of the first stage, what is the ideal resistance for R8, in kiloohms? (Don't pick a standard value yet.) _____ kΩ
12. Pick the **closest** standard 10% resistor to the ideal value, in kiloohms: R8 = _____ kΩ
13. Calculate the theoretical overall passband gain for this circuit: _____
14. If the input signal has an amplitude of 1.0 V_p, determine the theoretical amplitude in the following regions or points of the frequency response curve:

within the passband	_____ V_p
at the cutoff frequency, f_c	_____ V_p
one decade beyond f_c	_____ μV_p

Simulation

In Multisim, build the filter from the previous question, shown again here for convenience.



Notes:

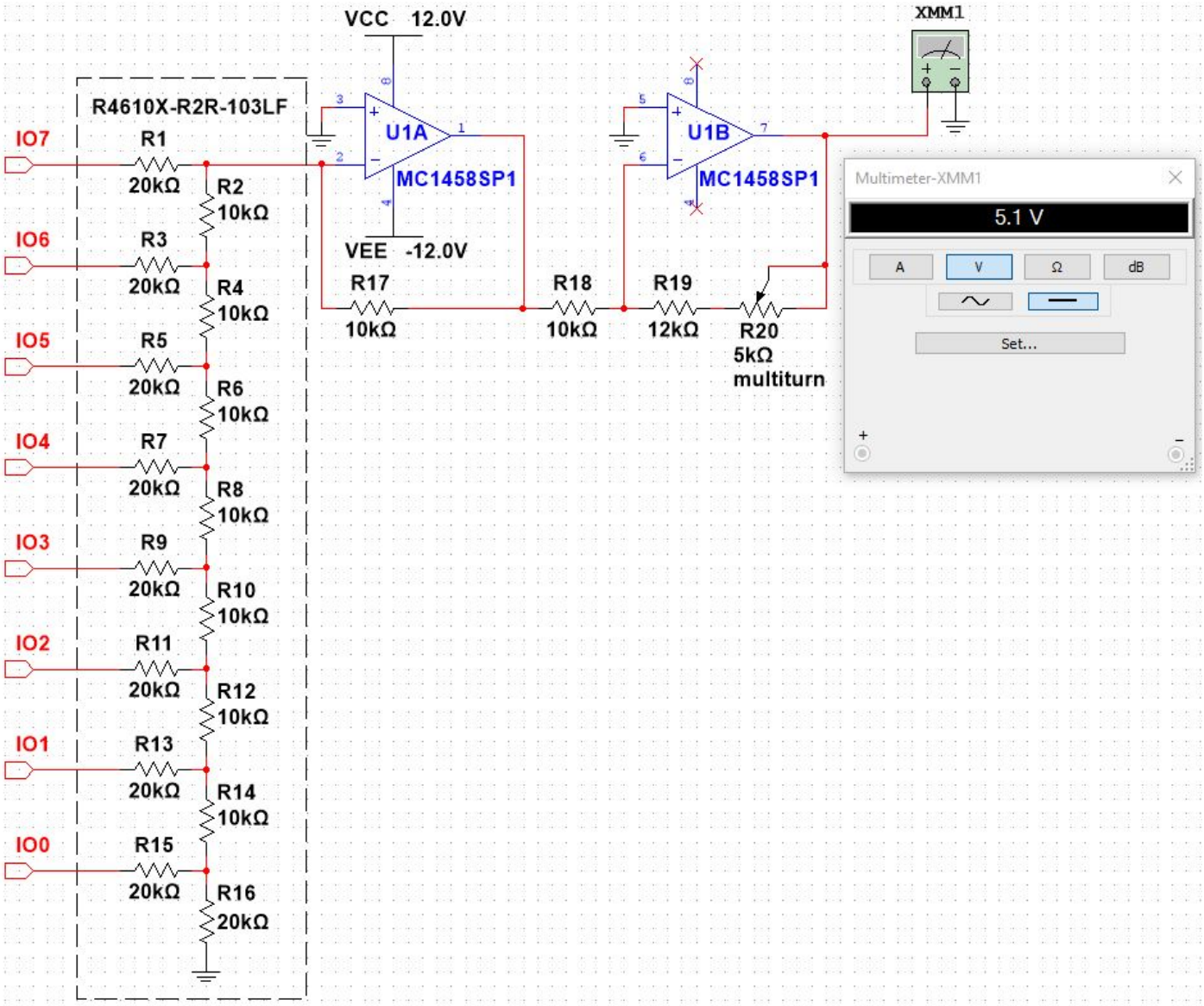
- Use the resistors chosen in the previous exercise. If in doubt, verify your values with your instructor. (If your values aren't correct, this would be a good time to determine why!)
- Note there is only one IC in this design -- it uses three out of the four op amps in a single quad op amp IC. (By the way, notice the strange pin choices for the two power pins -- be aware of this anytime you build a circuit using an LM324!)
- Use an ***Agilent*** function generator, as this allows you to sweep through a range of frequencies with the turn of a dial
  - Sine wave
  - 1.0 V_p (make sure your signal is 1.0 V_p, not 1.0 $V_{p\text{-}p}$)
  - Start at a frequency one decade below the expected cutoff frequency
- Use a ***Tektronix*** four-channel oscilloscope to observe V_{in} (Ch1) and V_{out} (Ch2)

15. Verify that the circuit is working correctly. Set both oscilloscope channels to **maximize** the circuits (in other words, don't use the same settings for the two channels this time) and upload a screenshot showing your circuit and your oscilloscope screen for a grade out of five marks. If your instructor grades this work in class, upload a textfile with the grade assigned instead. Document Upload (Direct)
16. From the amplitudes of the input and output signals, calculate the passband gain for this circuit: _____
17. From the output signal amplitude, determine the target voltage for determining the cutoff frequency, and record it here in peak volts: _____ V_p
18. Empirically determine the cutoff frequency: _____ kHz

19. For a grade out of four marks, upload a screenshot showing your oscilloscope screen, with the necessary measurements, as seen at the cutoff frequency. If your instructor grades this in class, upload a textfile with the grade assigned instead. Document Upload (Direct)
20. Set the frequency to exactly **double** the cutoff frequency you determined empirically, and measure the output voltage amplitude. Make sure you adjust your oscilloscope to provide you with accurate measurements. Record your measurement here, in peak millivolts: _____ mV_p
21. Determine the rolloff for this filter, in decibels per octave (i.e. at double the frequency). Your answer should be negative, as the slope is down to the right. _____ dB/octave
22. Convert this to decibels per decade by dividing by log(2): _____ dB/decade
23. Your answer should verify that this is a _____ -pole filter.
24. For a grade out of four marks, upload a screenshot of your oscilloscope with the settings and measurements described above for one octave above the cutoff frequency. If your instructor grades this in class, upload a textfile with the grade assigned instead. Document Upload (Direct)

R-2R Ladder DAC

Consider the following schematic diagram while answering the questions below.



25. How many bits is this DAC? _____
26. If all the digital inputs are LOW, what is the expected output voltage? _____ V
27. This DAC is

(a) Single Quadrant

(b) Two Quadrant

(c) Four Quadrant

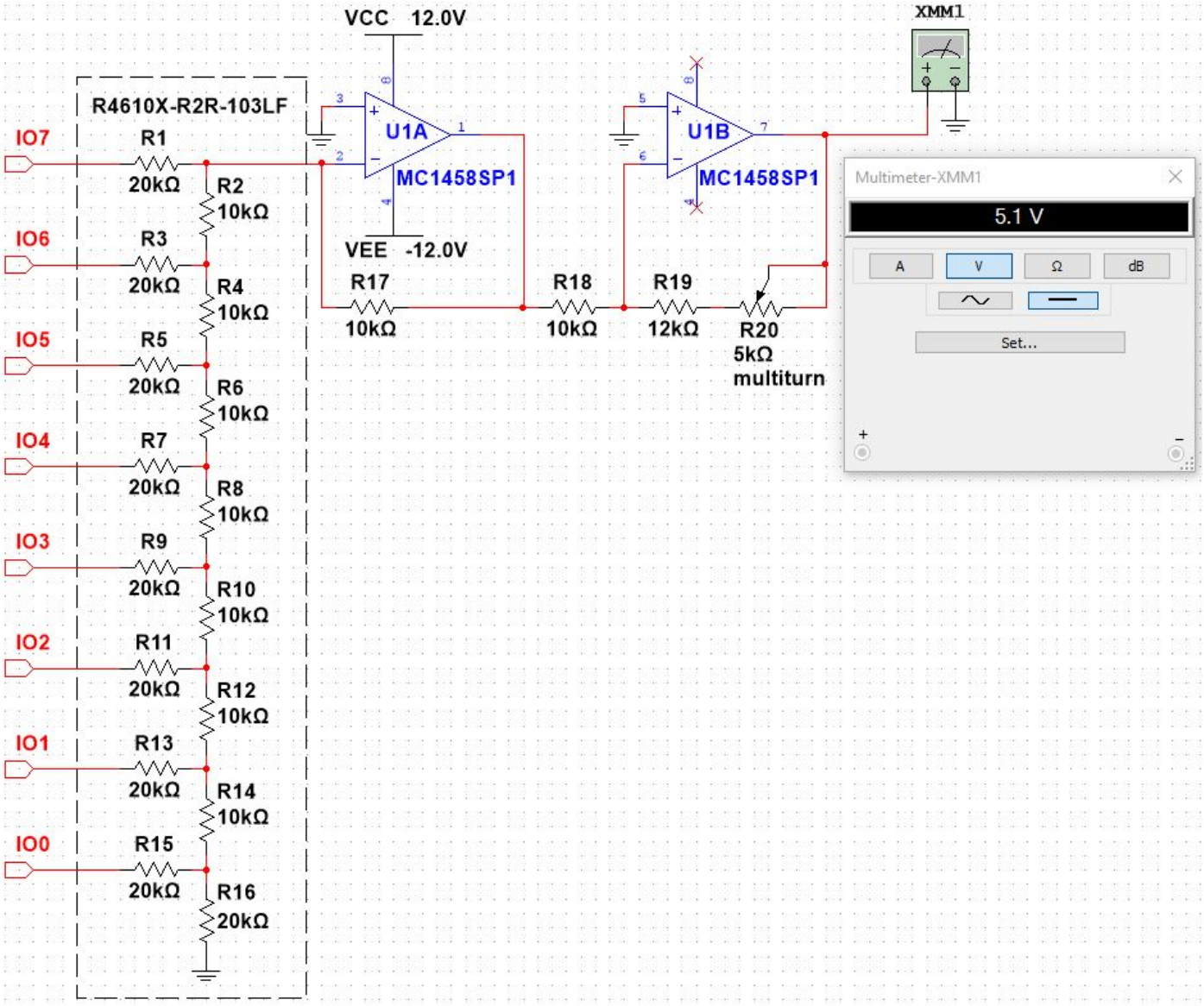
28. The intent for this circuit is to have the maximum digital input value generate the maximum range value of 5.100 V, as shown in the simulation shown above. What is the maximum digital input value, as a decimal number? _____ . From this, determine the desired step size, in millivolts per step: _____ mV/step.
29. Assume input logic levels of 0.0 V and 3.3 V. If just the MSB is set (all the rest of the inputs are cleared to zero), what is the expected output voltage? _____ V. From this, determine the total circuit gain required for just the MSB: _____ . What is the theoretical gain of the first op amp stage, for just the MSB? (Don't forget polarity.) _____ Now, using the gain of the first stage and the overall gain required for just the MSB, determine the required gain for the second op amp (record four significant digits, and don't forget polarity): _____ . Finally, determine the ideal value for the feedback resistance of the second stage (don't pick a 10% standard resistor value, and record four significant digits): _____ kΩ. This should verify that the combination of fixed resistor and potentiometer will allow for proper adjustment of the gain to meet the specifications for this circuit.

You have now completed the Preparation and Simulation component of this project. Move on to the Circuit Build and Test section. Don't "Submit" yet!

Question 2: (50 points)

DAC Build and Test

On your breadboard, build the circuit shown in the schematic diagram below. Notes to follow.



Notes:

- This circuit looks complicated, but isn't that bad -- the sixteen resistors of the R-2R ladder are contained in a single 10-pin SIP, provided to you by your instructor.
- There's only one DIP IC -- a 1458 dual op amp.
- Provide the eight digital inputs using your Analog Discovery 2.
    - Establish a common ground using one of the black fly-wires from the AD2 to your board's ground
    - Select "Static IO" from the main menu
    - Change DIO 0-7 to "Switch --> Push/Pull (1/0)"
    - Connect the digital flywires for DIO 0-7 to the appropriate inputs of your circuit
- Use a digital multimeter (DMM) to measure the output voltage

Start by calibrating your circuit. Set all the inputs to generate the maximum possible digital input, then adjust the gain-setting potentiometer to give you as close as possible to the expected output voltage, as shown in the schematic.

For a grade out of five marks, take a picture of your printed circuit board and DMM showing the output for the maximum digital input value. If your instructor grades this in class, upload a textfile with the assigned grade instead. Document Upload (Direct)

Set the inputs to each of the following hexadecimal values, and record the output voltage displayed on your DMM, accurate to two decimal places.

Digital input, hexadecimal	Output voltage, V
00	_____
1F	_____

80	_____
9C	_____
FF	_____

You have now completed this Project. Once you submit your work, you will not be able to return to any of these questions!

Online Homework System

Assignment Worksheet
5/20/22 - 9:37:23 AM MDT

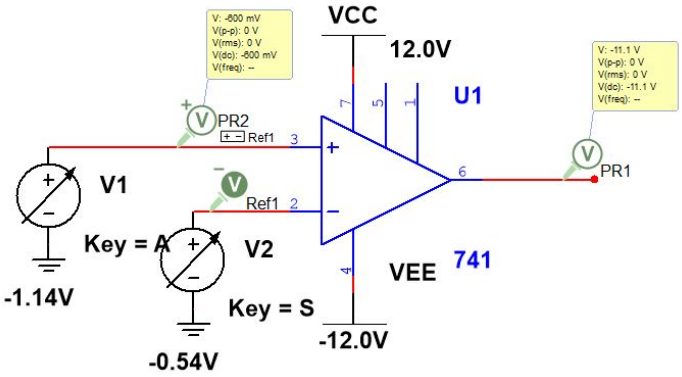
Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Comparators

Question 1: (1 point)

When you were introduced to op amps, you briefly investigated what happens with a high gain amplifier if there is a measurable differential input voltage. From that, you developed a model for op amps ***when they are acting as amplifiers***: the Virtual Short. You've been using that model for so long you may have come to believe that there can never be a difference in voltage between the inputs.

Using Multisim, create the following circuit.

- V1 and V2 are DC_INTERACTIVE_VOLTAGE, available under Sources->SIGNAL_VOLTAGE_SOURCES
- Set both V1 and V2 to Maximum Value = 5 V, Minimum Value = -5V, Increment =0.1%
- Monitor the output using a standard voltage probe, as shown
- Monitor the differential input voltage using a differential voltage probe  , with the probe on the non-inverting input and its reference on the inverting input.
- Use +/- 12 VDC to power the 741 op amp.



Set V1 and V2 to the following values, and record the results seen on the voltage probes.

V1 (non-inv), V	V2 (invert), V	Vdiff, V	Vout, V
1.00	-1.00	_____	_____
-0.05	0.10	_____	_____
3.50	2.50	_____	_____
2.25	2.29	_____	_____
-0.01	-0.07	_____	_____

So, when there is a measurable difference in voltage between the two pins of an op amp, there are only two possible outputs: maximum positive voltage or maximum negative voltage. This is affectionately known as "nailed to the rails". Why does this happen? Let's look at the first example above. In this case, the differential voltage between the pins is +2 V. If the amplifier has an open circuit gain of 200,000, what would the theoretical output voltage be? Record the numeric part as a number between 1 and 999 _____ and select the correct unit:

(a) mV

(b) V

(c) kV

Our amplifier is only powered from +/- 12 VDC, so there is no possible way it can achieve the voltage predicted by the gain formula. In this case, using terminology we learned with transistors, it is saturated, and its output is dictated by components external to the op amp itself, in this case the power supplies. As with transistors, op amps that are not operating in the active linear region are said to be in switch mode. Actually, since this is not a "rail to rail" op amp, it can only come to within about 1 V of the rails.

The good news is that, if there are only two possible outputs, the device is binary. That means it can be used as an interface between the real world and binary digital devices.

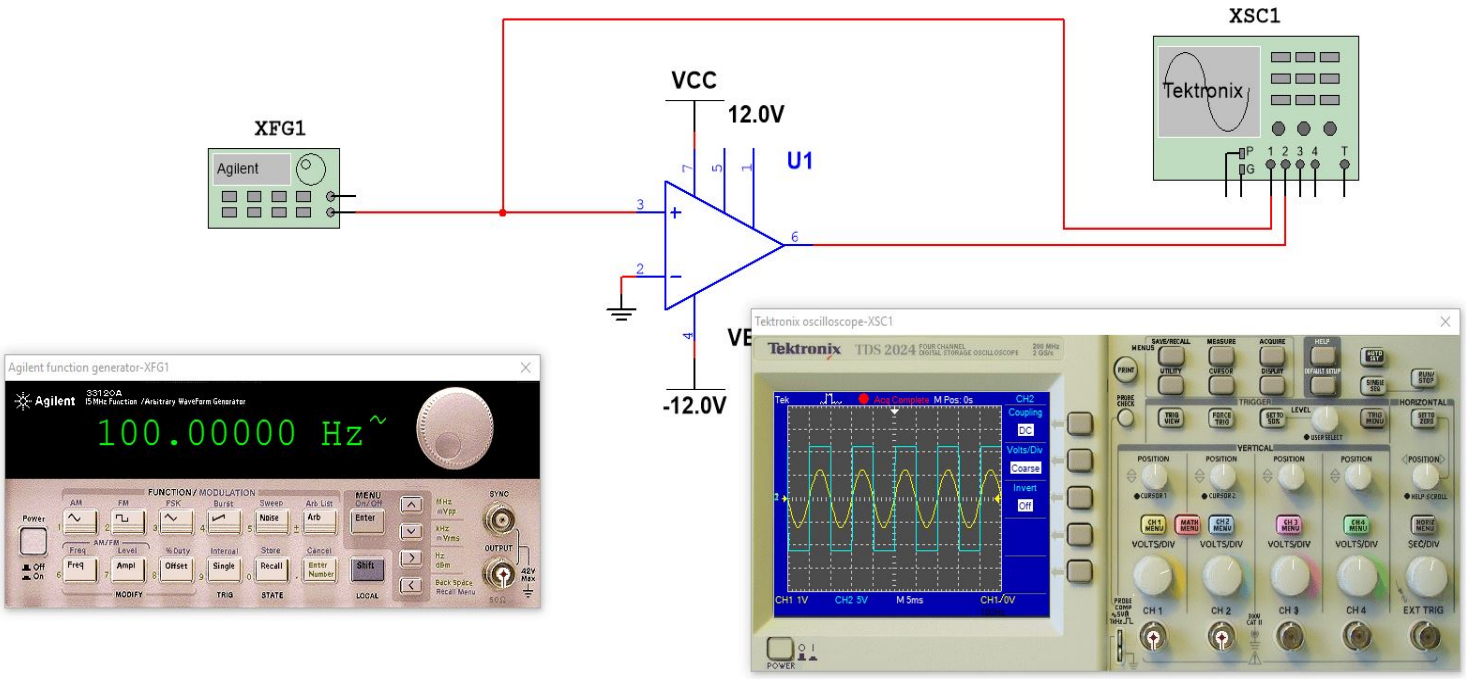
Comparators

The two possible outcomes, in fact, tell us which of the inputs is at a more positive voltage. If the non-inverting input is more positive, the output will be positive; if the inverting input is more positive, the output will be negative. So, in switch mode, the op amp "compares" the two signals and reports which one is more positive; therefore, when in this configuration, we don't call it an ampifier, we call it a ***Comparator***.

Zero Crossing Detectors

If one of the inputs is grounded, the output of the comparator will change states when the other input changes from positive to negative or *vice versa*. Therefore, the comparator detects when the input signal crosses the zero voltage line, and we call it a Zero Crossing Detector.

Modify your circuit in Multisim as shown. Please note that the Agilent Function Generator's true Output is the lower of the two "pins" shown -- the other on is called "Sync", and always generates a large unipolar square pulse, regardless of the waveform settings.



Set up the function generator to produce a 100 Hz sine wave with an amplitude of 2.5 $V_{p\text{-}p}$. Adjust your oscilloscope to display this signal adequately, as shown above.

Notice that, even though the input is a sine wave, the output is square -- there are only two possible output voltages: max+ and max-.

Also notice that, with the input signal connected to the non-inverting terminal, the output is positive when the input is positive, and negative when the input is negative. This makes it a ***Non-Inverting Zero Crossing Detector***.

Now, decrease the amplitude of the input signal slowly, all the way down to 50 $mV_{p\text{-}p}$. The amplitude of the input signal

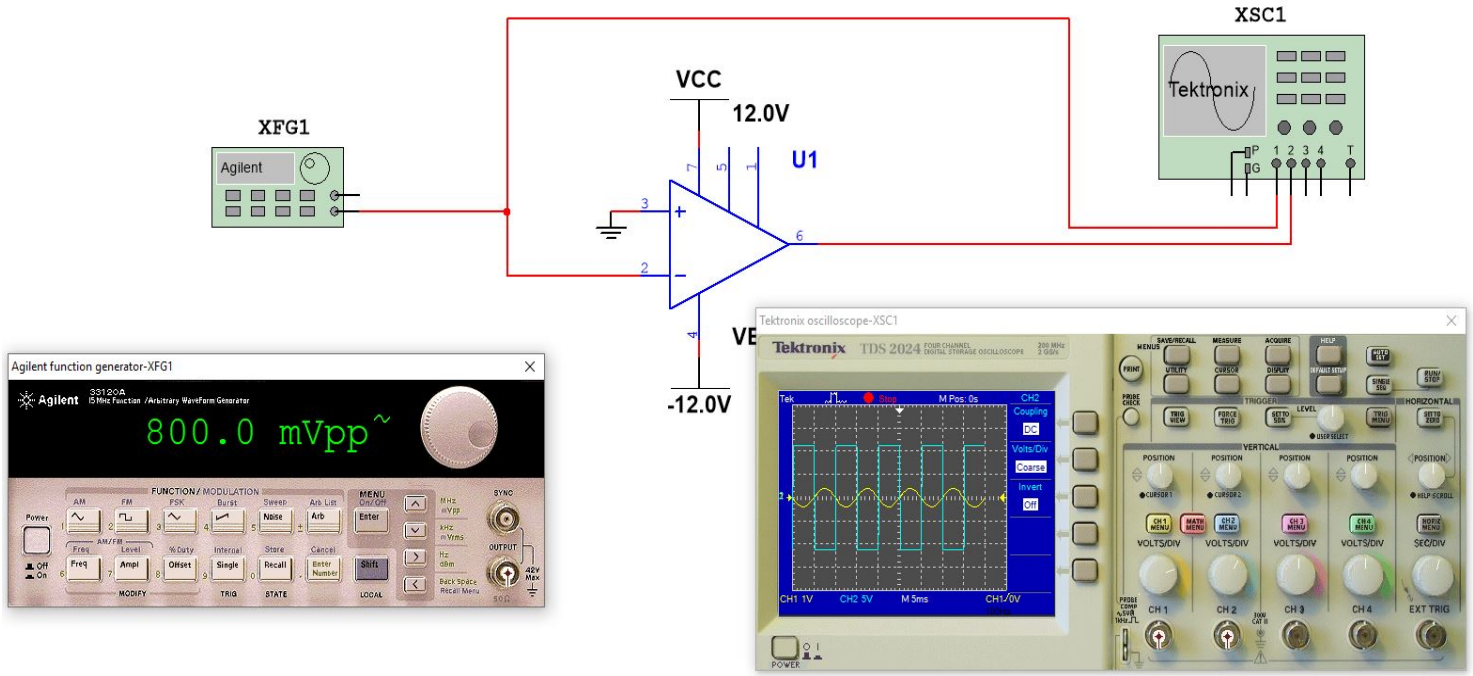
(a) Directly affects the amplitude of the output signal.

(b) Does not affect the amplitude of the output signal.

(c) Directly controls the shape of the output signal.

To prove that the last statement is not true, try switching to a square wave input, then a triangle wave input.

Now, ground the non-inverting input and connect the function generator to the inverting input, as shown. You can increase the amplitude back to where the input signal is clearly visible again.



Notice now that, although the output looks the same (rail to rail), it is positive when the input is negative and negative when the input is positive. This makes it an ***Inverting Zero-Crossing Detector***.

Dedicated comparators

While we have the previous circuit operational, increase the frequency slowly from the 100 Hz you started with up to 10 kHz. You should notice that the output is no longer a square wave. This is caused by

(a) Slew Rate

(b) Small-Signal Bandwidth

(c) Low-Pass Filtering

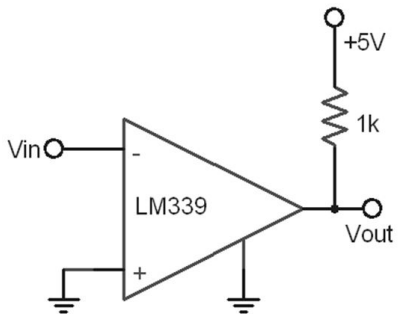
(d) High-Pass Filtering

To overcome this problem, IC manufacturers have developed "dedicated comparators" -- op-amp-based ICs that can only be used as comparators. Most of these have transistor switches in their outputs to make sure the output level shifts are as rapid as possible. ***Dedicated Comparators*** come in two basic flavours:

- Open Collector (or Open Drain) Outputs
- Driven Outputs

The ones with driven outputs do not need any external components to make them work. However, the Open Collector or Open Drain output devices require an external pullup resistor in order to work. The Collector (or Drain, if it's a FET) of the internal transistor is simply presented to the user to connect as desired. If the desired logic levels are to be 0 and 5 V, the user would connect a pullup resistor to a $+5V_{DC}$ supply. Any other supply could be used, regardless of what is being used to power the comparator. Typically, comparators reference their outputs to ground, so they automatically generate "Unipolar" signals -- signals with only one non-zero voltage and zero volts as the other option.

The LM339 is one such open collector comparator, pictured below. This is actually just one of four comparators in an LM339 quad IC.

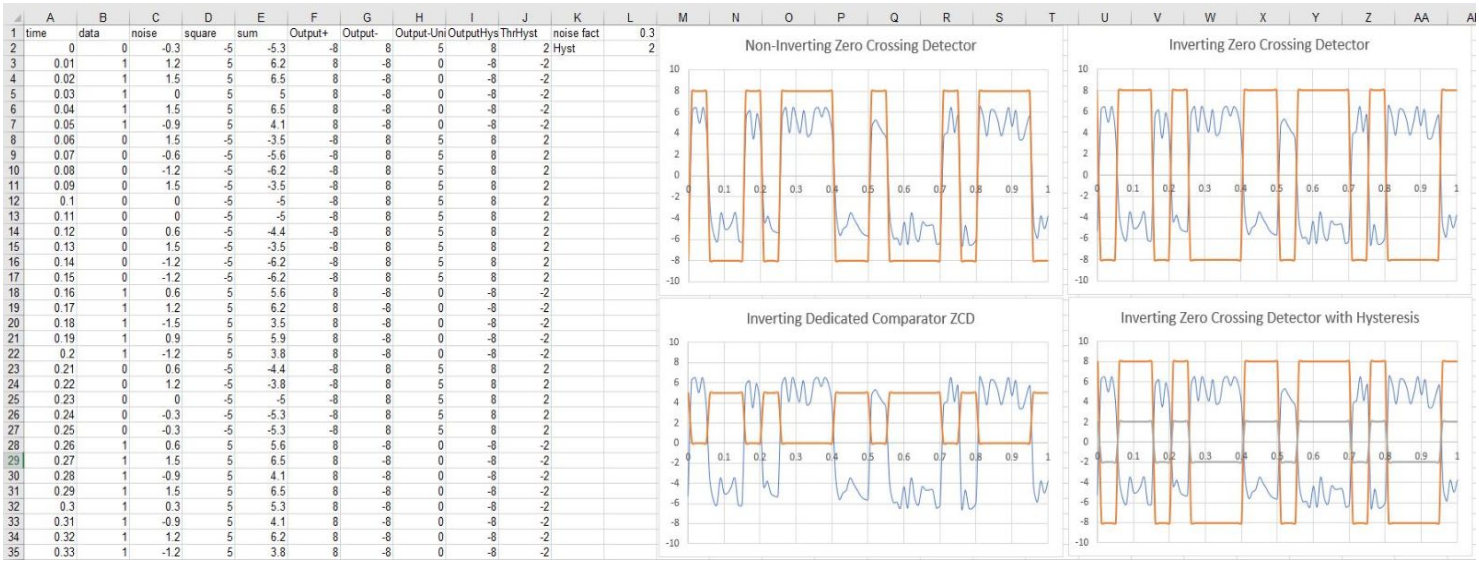


In this configuration, it is set up as an inverting zero crossing detector with TTL Logic outputs.

Since the dedicated comparators are designed to be very fast, and since their outputs are single transistors, the issue of Slew Rate is dealt with.

Data Regeneration

One application for Zero Crossing Detectors is in regenerating digital signals that have deteriorated during transmission due to amplitude attenuation and the introduction of noise. In Moodle, you'll find an Excel file called "Data Regeneration". Open it up, and you should see something like the following:



	A	B	C	D	E	F	G	H	I	J	K	L
1	time	data	noise	square	sum	Output+	Output-	Output-Uni	OutputHys	ThrHyst	noise fact	0.3
2	0	0	-0.3	-5	-5.3	-8	8	5	8	2	Hyst	2
3	0.01	1	1.2	5	6.2	8	-8	0	-8	-2		
4	0.02	1	1.5	5	6.5	8	-8	0	-8	-2		
5	0.03	1	0	5	5	8	-8	0	-8	-2		
6	0.04	1	1.5	5	6.5	8	-8	0	-8	-2		
7	0.05	1	-0.9	5	4.1	8	-8	0	-8	-2		
8	0.06	0	1.5	-5	-3.5	-8	8	5	8	2		
9	0.07	0	-0.6	-5	-5.6	-8	8	5	8	2		
10	0.08	0	-1.2	-5	-6.2	-8	8	5	8	2		
11	0.09	0	1.5	-5	-3.5	-8	8	5	8	2		
12	0.1	0	0	-5	-5	-8	8	5	8	2		
13	0.11	0	0	-5	-5	-8	8	5	8	2		
14	0.12	0	0.6	-5	-4.4	-8	8	5	8	2		
15	0.13	0	1.5	-5	-3.5	-8	8	5	8	2		
16	0.14	0	-1.2	-5	-6.2	-8	8	5	8	2		
17	0.15	0	-1.2	-5	-6.2	-8	8	5	8	2		
18	0.16	1	0.6	5	5.6	8	-8	0	-8	-2		
19	0.17	1	1.2	5	6.2	8	-8	0	-8	-2		
20	0.18	1	-1.5	5	3.5	8	-8	0	-8	-2		
21	0.19	1	0.9	5	5.9	8	-8	0	-8	-2		
22	0.2	1	-1.2	5	3.8	8	-8	0	-8	-2		
23	0.21	0	0.6	-5	-4.4	-8	8	5	8	2		
24	0.22	0	1.2	-5	-3.8	-8	8	5	8	2		
25	0.23	0	0	-5	-5	-8	8	5	8	2		
26	0.24	0	-0.3	-5	-5.3	-8	8	5	8	2		
27	0.25	0	-0.3	-5	-5.3	-8	8	5	8	2		
28	0.26	1	0.6	5	5.6	8	-8	0	-8	-2		
29	0.27	1	1.5	5	6.5	8	-8	0	-8	-2		
30	0.28	1	-0.9	5	4.1	8	-8	0	-8	-2		
31	0.29	1	1.5	5	6.5	8	-8	0	-8	-2		
32	0.3	1	0.3	5	5.3	8	-8	0	-8	-2		
33	0.31	1	-0.9	5	4.1	8	-8	0	-8	-2		
34	0.32	1	1.2	5	6.2	8	-8	0	-8	-2		
35	0.33	1	-1.2	5	3.8	8	-8	0	-8	-2		

This file is dynamic. If you press F9 (or do almost anything in the spreadsheet), the data and output graphs will change. The "noise" on the signal is controlled by a random generator that can be refreshed at any time.

The thin blue line in each of the graphs represents a degraded digital signal, and the heavier sepia (I think that's its colour) line represents the output of the particular comparator circuit described in each chart title.

Notice how, with the initial settings, the fairly noisy input signal is always "regenerated" to the same correct data, in all of the charts. Since the new signal could now be transmitted again without the noise, Zero-Crossing Detectors as applied to data are called ***Data Regenerators***.

The top two charts are very similar, except for the polarity. Satisfy yourself that one of them in non-inverting and the other is inverting.

The bottom left chart shows the output for a Dedicated Comparator, like the LM339, configured as an inverting zero-crossing detector, with a pullup resistor to $+5V_{DC}$. This is the circuit shown previously. Notice that this circuit generates logic levels like the ones you've become accustomed to in you Digital Logic course.

The "noise fact" number in the spreadsheet represents the ratio of the noise to the signal size. Slowly increase this from 0.3 to 1.4. When is the noise big enough to start to introduce transitions that aren't in the original data, for the three charts previously discussed?

(a) 0.5

(b) 0.8

(c) 1.0

(d) 1.2

The reason these two Zero Crossing Detectors start to fail is that the noise is now big enough to cross the zero line even when the data is not supposed to.

But take a look at the bottom right chart. It doesn't show the false transitions the other ones are showing. With the "Hyst" setting at 2, further increase the noise factor until this one starts failing. This happens at

(a) 0.8

(b) 1.0

(c) 1.2

(d) 1.4

Notice how badly the other ones are failing, but that the bottom right one is just catching the occasional noise spike. Set the "Hyst" to 1.35 to return to a clean output on this one. The bottom right chart represents the output from a comparator with positive feedback, also known as "Hysteresis", which is a topic in the next Online Lesson.

So, from this lesson, you've learned:

- Op amps with measurable voltages between the input pins will be in saturation, with only two output options: max+ and max-.
- Comparators indicate which input is more positive by the polarity of the output voltage.
- Zero Crossing Detectors compare an input signal to ground, and therefore report whether the input is positive or negative.
- Depending on which input is grounded, a zero crossing detector can be inverting or non-inverting.
- The slew rate of a standard op amp limits its usefulness; Dedicated comparators overcome this issue, and may provide additional external control if they are open collector or open drain. Typically, these devices produce Unipolar output signals.
- Zero Crossing Detectors can be used as Data Regenerators to clean up data that has been degraded due to attenuation and noise during transmission over a distance.
- If the noise is too great, even a Zero Crossing Detector will allow errors to be re-transmitted.

Online Homework System

Assignment Worksheet
5/20/22 - 9:36:48 AM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Comparator Applications

Question 1: (1 point)

In a previous lesson, you learned how op amps are used to compare two voltages and report which of them is more positive. That seems like a pretty simple concept. As with any simple concept, humans will think of all sorts of complicated things to do with it. We've already seen how comparators can be used to regenerate digital information that has been degraded during transmission over a distance. However, there are times when the noise is too great to be rejected by a simple comparator.

Hysteresis

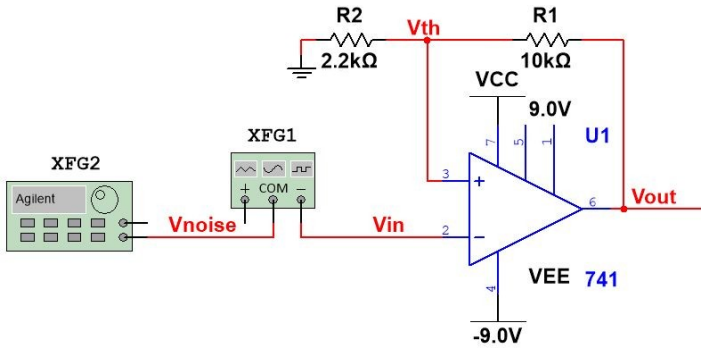
Hysteresis adds improved noise rejection to a comparator circuit. In a simple comparator, the voltage that's being compared to, typically called the "Threshold", is constant. For a zero crossing detector, that threshold is always zero.

Hysteresis introduces a changing threshold. The threshold moves "farther away" from the noise, and shifts depending on whether the output is positive or negative.

From Moodle, open up the Excel spreadsheet called "Data Regeneration". Notice that, in the bottom right chart, there's an extra grey line. That's the Threshold voltage. Notice also that the comparator is in Inverting mode -- that's a requirement for hysteresis.

Increase the noise factor to 1.3, and "refresh (F9)" the screen a few times. Notice that the other three windows are failing consistently, as the noise is crossing the zero line frequently. However, the Hysteresis screen doesn't show any failures. Although the noise is crossing the zero line, it isn't crossing the grey threshold line. When the signal is negative, the threshold line is positive, or "farther away" so the noise doesn't cross it; then the signal is positive, the threshold is negative, so again the noise doesn't cross it. In essence, the improvement in noise rejection is equal to the difference between zero and the threshold, in volts peak, or equal to the difference between the upper and lower thresholds, in volts peak to peak.

But how do we add hysteresis? The clue is in the phrase "move farther away". Unlike with amplification, where negative feedback made the variations smaller by reducing the gain, here we need ***positive feedback*** to increase the variations.



Notice the feedback network. It looks very like what we've used for linear amplifiers, except that it is connected to the non-inverting input. That means it is providing positive feedback instead of negative feedback, and will therefore be a comparator, not an amplifier.

Using Multisim, build the circuit shown above. The odd series arrangement of the two function generators allows us to produce the equivalent of a data pulse with variable noise.

Set up the generic function generator, XFG1 in the schematic, to produce a Square Wave with a frequency of 100 Hz, a duty cycle of 50%, an amplitude of 2.5 V_p (i.e. 5.0 V_{p-p}), and an offset of 0.

Set up the Agilent function generator, XFG2 in the schematic, to produce a Sine Wave with a frequency of 980 Hz, an amplitude of 1 V_{p-p} to begin with, and an offset of 0.

Use a Tektronix 4-channel oscilloscope to display the following:

Channel 1 to display V_{in} on the inverting pin of the op amp

Channel 2 to display V_{th} on the non-inverting pin of the op amp

Channel 3 to display V_{out}

Set all three channels to 5 V/div, and adjust the time base (Horizontal) to display about two cycles of the output signal.

Now, increase the noise signal (Agilent) slowly. At about 5 V_{p-p}, you should see that the noise touches the zero line from both top and bottom. However, the output signal remains unchanged. If this were a simple zero crossing detector, the output would, at this point, start to produce unwanted transitions.

Continue to increase the noise signal slowly. At some point, you should see the output signal start to produce unwanted transitions. Record the noise voltage, in peak-to-peak volts. _____ V_{p-p}

Subtract the 5 V_{p-p} that you observed when the noise reached the zero line: _____ V_{p-p} This is the improvement in noise rejection resulting from the hysteresis, or positive feedback.

Now, use the measurement features of the Tektronix oscilloscope to measure the difference between the upper threshold and lower threshold voltages (i.e. peak-to-peak voltage of Channel 2). _____ V_{p-p}

The improvement in noise rejection correlates most closely to

(a) The noise voltage

(b) The difference between the thresholds

(c) The digital signal voltage

Look at the traces on your oscilloscope, with the noise set so the output is just beginning to produce unwanted transitions. You should be able to see that the noise is just touching the trace for the threshold voltage as it appears at the non-inverting terminal of the op amp.

Mathematically, the threshold voltage, and hence, the improvement in noise rejection, is easy to determine. Use the oscilloscope to determine the maximum and minimum voltages on the output signal.

$V_{out(max)}$ _____ V

$V_{out(min)}$ _____ V

Notice that V_{th} is in the middle of a voltage divider between V_{out} and ground. For the two possible output voltages, determine the associated threshold voltages:

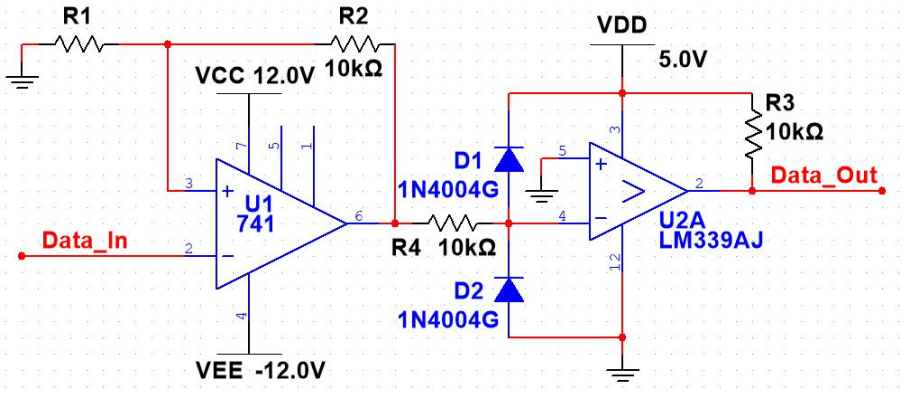
$V_{th(+)}$ = _____ V

$V_{th(-)}$ = _____ V

Find the difference between the upper and lower threshold voltages. This should be very close to the improvement in noise rejection seen earlier, so we'll make the jump and call this the noise improvement in peak to peak volts: _____ V_{p-p}

Worked Example

The following circuit is expected to increase the noise immunity in the output signal by 3.0 V_{p-p} over a simple zero crossing detector.



First, let's figure out what this circuit does.

- The noisy data at Data_In arrives at the inverting pin of U1, and there's a positive feedback network on the non-inverting pin, referenced to ground. That makes the U1 circuit an inverting zero crossing detector with hysteresis.
- In order for this circuit to work, the noisy Data_In must be "bipolar" (i.e. positive to negative) in order to cross the threshold voltage and trigger the comparator.
- The output voltages from U1 will be approximately +/- 11 V, as the 741 isn't a rail-to-rail op amp.
- U2A is one of four comparators in an LM339 IC. The signal from U1 eventually arrives at the inverting pin of U2A, so, with the non-inverting pin grounded, U2A is an inverting zero crossing detector. With two inversions in the path, the polarity of the cleaned-up Data_Out is the same as the polarity of the noisy Data_In.

- U2A is an open-collector device, so R3 is installed to pull the signal up to +5 V when the internal transistor in U2A isn't pulling Data_Out to ground. So, the output logic is 0 V to +5 V, or standard TTL signalling.
- Notice that U2A is powered from +5 V to ground. This IC is picky about the input signal not exceeding the power rails by very much. That's what R4, D1, and D2 are about:
    - When the output from U1 is +11 V, D1 will be forward biased because current will flow from +11 V to +5 V through D1. That means D1 provides a 0.7 V drop to the +5 V supply, and the input signal to U2A will not exceed +5.7 V.
    - When the output from U1 is -11 V, D2 will be forward biased because current will flow from ground (0 V) to -11 V through D2. That means D2 provides a 0.7 V drop from ground, and the input signal to U2A will not go below -0.7 V.
    - In both directions, R4 provides a resistance across which the remaining voltage from the U1 output can be dropped.
    - This is referred to as either as a clipping circuit because it clips the input signals off at +5.7 V and -0.7 V or as a clamping circuit, because it clamps the input circuit to within 0.7 V of U2A's power rails.

Now, back to the problem at hand: How do we make this circuit improve the noise immunity by 3.0 $V_{p\text{-}p}$?

To do this, the Threshold voltage at the non-inverting pin would have to switch between +1.5 V and -1.5 V. Since the output of U1 switches between +11 V and -11 V, we can rework the voltage divider formula to provide a suitable value for R1:

$$V_{TH} = V_{out}\left(\frac{R_1}{R_1+R_2}\right)$$

so

$$R_1 = R_2\left(\frac{V_{TH}}{V_{out}-V_{TH}}\right) = 10\ k\Omega\left(\frac{1.5\ V}{11\ V\ -\ 1.5\ V}\right) = 1.58\ k\Omega$$

Since we don't have a 1.58 kΩ resistor in our kits, we'll pick the next biggest, because that will increase the noise rejection slightly. So, let's see what the theoretical results will be using a 1.8 kΩ resistor:

$$V_{TH} = V_{out}\left(\frac{R_1}{R_1+R_2}\right) = 11\left(\frac{1.8\ k\Omega}{1.8\ k\Omega+10\ k\Omega}\right) = 1.68\ V$$

Therefore, the improvement in noise rejection is 1.68 V_p or 3.36 $V_{p\text{-}p}$.

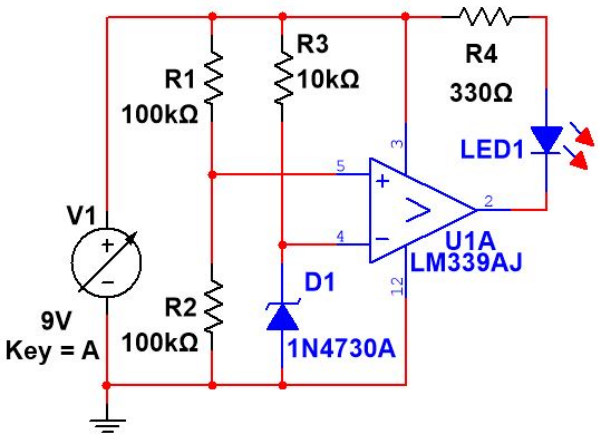
Summary

In this lesson, you have learned that

- Noise rejection can be improved using hysteresis
- Hysteresis employs positive feedback to move the threshold voltage "away" from the noise; in other words, the threshold voltage is no longer simply zero, as it would be in a zero crossing detector. It becomes positive when the noisy input is negative, and it becomes negative when the noisy input is positive.
- The threshold voltages are determined from the voltage divider between the output signal and ground.
- The improvement in noise rejection is equal to the difference between the thresholds, in volts peak to peak.

Question 2: (1 point)

As we saw in the introduction to comparators, we can compare an input signal to any voltage -- not just ground. The following circuit is a "Battery Low" indicator.



Build this circuit in Multisim. V1 is a DC_INTERACTIVE_VOLTAGE source. Make sure you select the "LED_red" from "LED" under "Diodes".

Start with V1 set to 9 V, to simulate a 9 V battery. Also set its "increment" to 1% for finer adjustment.

Run the simulator, and slowly decrease the "Battery" voltage until the LED lights. Record the voltage here. _____ V_{DC}

At this voltage, a 9 V battery would be considered "Dead".

Now to analyze this circuit to see why it works.

First, look up the 1N4730A Zener diode to see what its reverse breakdown voltage is. _____ V

Since the Zener diode is connected between the inverting terminal and ground, when the circuit is working, the voltage at the inverting terminal will be _____ V

When the battery is "good", i.e. 9.0 V_{DC}, what voltage will appear at the non-inverting terminal? _____ V_{DC}

(That's because of the voltage divider created by R_1 and R_2, since no current can flow into the input.)

When the battery is "good", the output will be _____

In this condition, no current can flow through the LED, so it will be OFF.

What would the battery voltage need to be to produce a voltage at the non-inverting input that matches the inverting input voltage? _____ V_{DC}

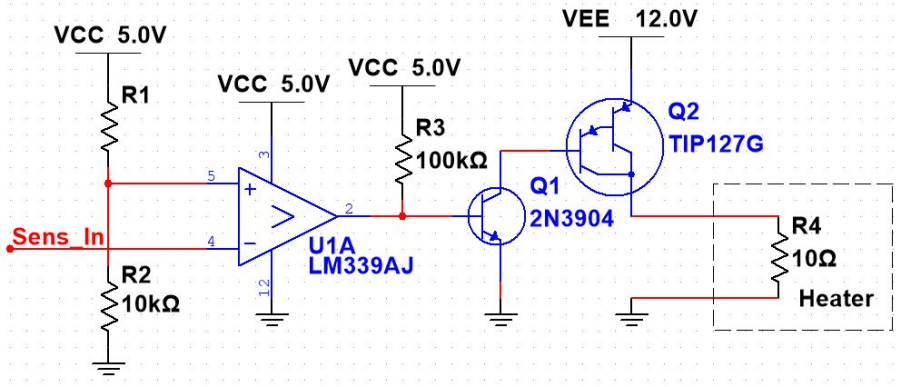
When the battery voltage is too low, the output will be _____

Recall that the LM339 is an Open Collector device -- its output is the collector of an internal transistor. The output goes LOW when this transistor is turned ON, allowing current to flow through the LED.

Note that in this circuit the Zener diode provides a constant reference voltage regardless of the condition of the battery, as long as the battery voltage is high enough to put the Zener into reverse breakdown.

Worked Example

The following circuit receives an input voltage from a temperature sensor. When the temperature is too low (i.e. when the sensor voltage drops below 1.25 V), the Heater turns on.



First, let's analyze this circuit:

- The Sensor signal connects to the inverting input, so when the temperature is high, the output of U1A will be LOW, with its internal transistor turned on; when the temperature is too low, the output of U1A will be pulled up to +5.0 V. No current will flow into U1A's output, but R3 will act as the Base resistor for Q1.

- Q1 will be turned on, with a Base current of (5.0 V - 0.7 V)/100k = 43 μA. This means that the Collector of Q1 could draw up to βI_B = 100*43 μA = 4.3 mA from the Base of Q2.
- Q2 is a Darlington Pair PNP Power Transistor, which you'll learn more about in a subsequent course. Suffice it to say that it has a β of about 1200. The maximum Collector current that could be drawn through the heater is $I=V_{EE}/R4$ = 12 V/10 Ω = 1.2 A. Q2's Base current therefore would be 1.2 A/1200 = 1 mA, so Q1's Collector current is sufficient to turn Q2 on.
- So, when the Sensor voltage is lower than the Threshold voltage at the non-inverting input of U1A, the output of U1A goes high, allowing Q1 to conduct which draws Base current from Q2 which will turn it on and run about 1.2 A through the heater.
- When the Sensor voltage is higher than the Threshold voltage at the non-inverting input of U1A, the output of U1A goes low, turning off Q1 so no Base current is available to Q2, and Q2 will be off -- no current through the heater.

So, back to the original problem. The heater is supposed to come on if the Sensor voltage drops below 1.25 V. That means the Threshold voltage at the non-inverting input has to be set to 1.25 V. Reworking the voltage divider formula gives us the following:

$$V_{TH} = V_{CC}\left(\frac{R_2}{R_1+R_2}\right)$$

so

$$R_1 = R_2\left(\frac{V_{CC}-V_{TH}}{V_{TH}}\right) = 10\ k\Omega\left(\frac{5\ V-1.25\ V}{1.25\ V}\right) = 30\ k\Omega$$

In this case, we'll assume that the 1.25 V is critical, so we'll come up with a way to make 30 kΩ; and since we're doing that, we might as well make it adjustable! If we pick a standard potentiometer (with only 1, 2, and 5 available as multipliers) and a fixed resistor that's between 2x and 5x its size, it looks like we could use a 10 kΩ potentiometer and a 27 kΩ fixed resistor to provide a range of resistances from 27 kΩ to 37 kΩ.

Question 3: (1 point)

When we discussed digital to analog conversion (D to A), we mentioned that D to A was the simpler process, and that one of the better known A to D conversion processes actually relies upon the DAC as one of its components. Now that we've been introduced to the comparator, a device that compares two voltages to indicate which is more positive, we have the tools necessary to tackle A to D conversion.

Approaches to A to D Conversion

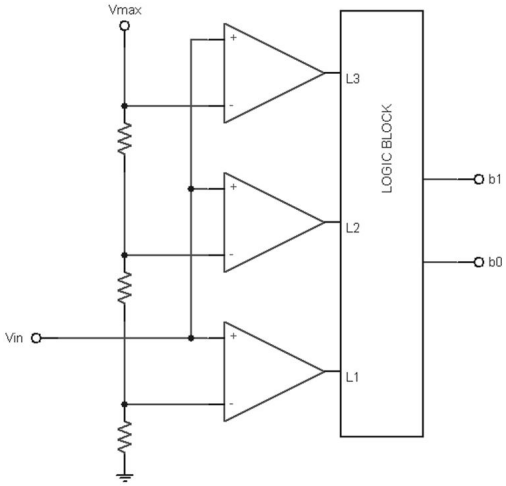
There are a number of different ways in which analog characteristics from the real world are digitized. The three main ways are:

1. Direct Conversion (also called Flash Conversion)
2. Fast Ramp Conversion
3. Successive Approximation Conversion

There are variations of the second one (Fast Ramp Conversion) which attempt to speed it up (contrary to its promising name, it is definitely the slowest of the approaches!) These are called things like Delta Conversion, Sigma Conversion, Delta-Sigma Conversion, etc. For this course, however, we will stick to the three main techniques.

Direct Conversion

Direct Conversion produces a binary result as a single event, or, in digital logic terms, in one clock cycle. As a result, this is a very fast technique, but the down-side to it is that it is very hardware intensive. Here's a simple 2-bit direct converter. (This is a pretty lousy A to D converter, as it only has four levels and three steps -- you're definitely not going to be listening to Tchaikovsky with this one!)



You'll get to build a 3-bit version of this circuit in the Lab, so instead of building and testing this circuit, we'll simply analyze it.

If V_{max} is 5.000 V and all three resistors are the same, we can analyze the thresholds for the comparators using a 3-resistor voltage divider as follows.

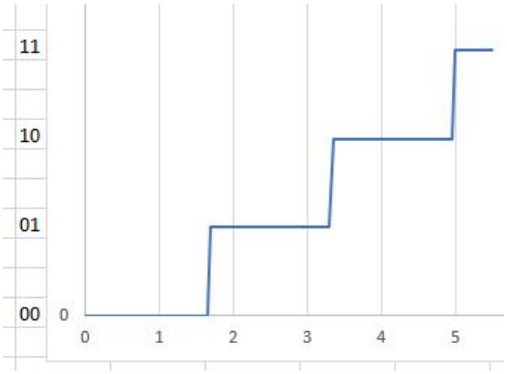
The current through the voltage divider would be

$I = \frac{V_{\max}}{3\ R}$, since the total resistance is the series combination of the three resistors.

The voltage for "L1" would then be

$$V_{L1} = R\left(\frac{V_{\max}}{3\ R}\right) \ = \ \frac{5}{3} = 1.667\ V$$

Following the same logic, the threshold for "L2" would be 3.333 V, and the threshold for "L3" would be 5.000 V. Here, then, is the relationship between the input voltage and the output binary code, given that we simply need to count the steps in binary:



Any voltage below 1.667 V is considered as 00. Any voltage between 1.667 V and 3.333 V is considered as 01. Any voltage between 3.333 V and 5.000 is considered as 10. Any voltage above 5.000 V is considered 11. This example really demonstrates that digitizing an analog signal can result in the loss of a lot of the original data! That's what we called "Quantization Error".

The "Logic Block" for this circuit needs to take the three comparator outputs and convert them into binary. Typically, this would be a Priority Encoder -- a circuit that generates a binary combination that represents the highest active input. By the way, all the lower inputs will also be active, because the input voltage is high enough to trigger them all.

This example is deceptively simple. Increasing the number of bits in the output increases the resolution of the circuit, but with an exponential increase in the hardware complexity. Notice that two bits were generated by four different voltage levels, three of which were supplied by comparators and the fourth was zero.

Let's consider what would be needed for more complex Direct Converters.

If we wanted three bits, we would need:

_____ levels

_____ comparators (one for each step), and a

_____ input _____ output priority encoder.

Now, repeat for a sixteen bit Direct Converter.

_____ levels

_____ comparators and a logic circuit with

_____ inputs and _____ outputs. I'd like to see that circuit on a breadboard (or maybe a thousand breadboards!)

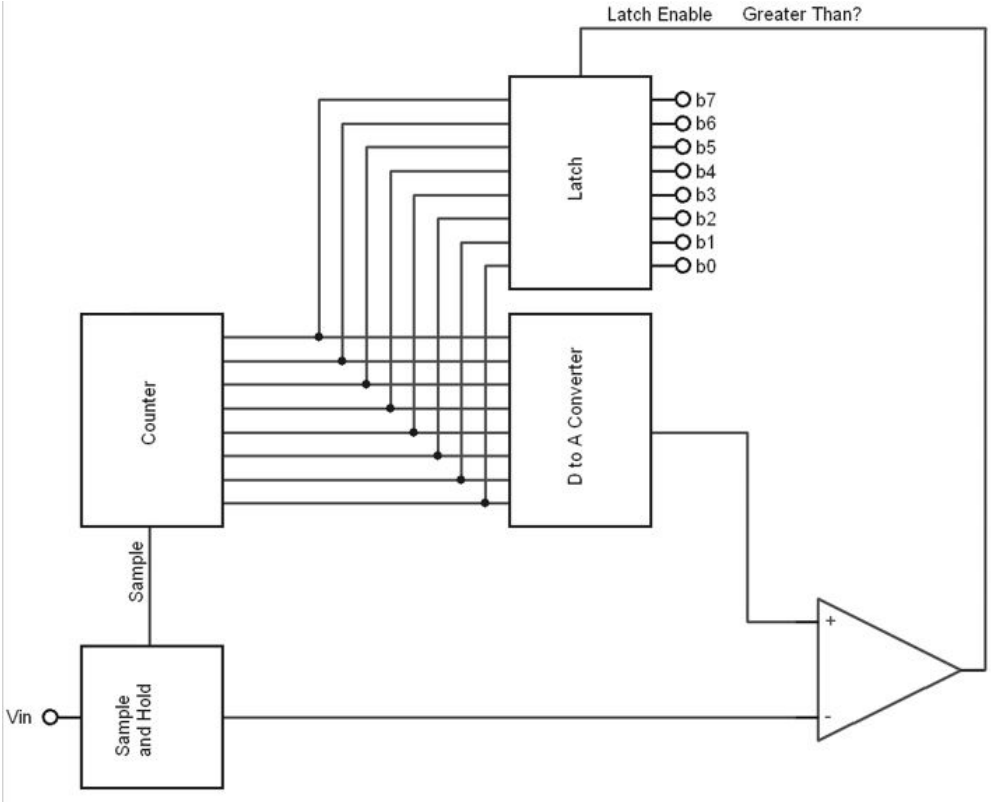
So, clearly, Direct Conversion is fast -- just one clock cycle -- but incredibly hardware intensive; and we haven't even talked about the digital logic involved in creating a Priority Encoder!

Fast Ramp Conversion

Clearly, there must be less hardware-intensive ways of digitizing characteristics from the real world. The Fast Ramp Converter is actually really slow. The name means you have to have a really fast binary ramp counter to make this even feasible.

With the Fast Ramp Converter, a DAC driven by a binary counter generates a constanty ramping output voltage until it reaches the top, then starts over again. The analog input signal is presented to one input of a comparatar, and the ramp is presented to the other input. When the ramp passes the analog signal, the value in the binary counter is stored as the binary representation of the analog input.

This introduces the need for a circuit called "Sample and Hold". At the beginning of each new ramp, a circuit at the input of the A to D converter grabs the present value of the input and keeps that value until the end of the ramp -- essentially an analog memory device. This is usually a capacitor, and the "switch" that temporarily connects the analog signal to it is usually a FET. The signal to get a new sample could be generated using the "Carry Out" of the counter. Here's the resulting block diagram of a Fast Ramp Converter.



In order for the sample rate to be constant (a definite requirement for proper digitization and playback), the Fast Ramp Converter needs to go through the entire counter ramp for each sample.

Just to see how slow this system is, let's compare it to a Direct Converter. Let's say that the clock running each of these devices issues a pulse every nanosecond.

How many samples per second would an 16-bit Direct Converter be able to make, in megasamples per second? _____ MSa/s

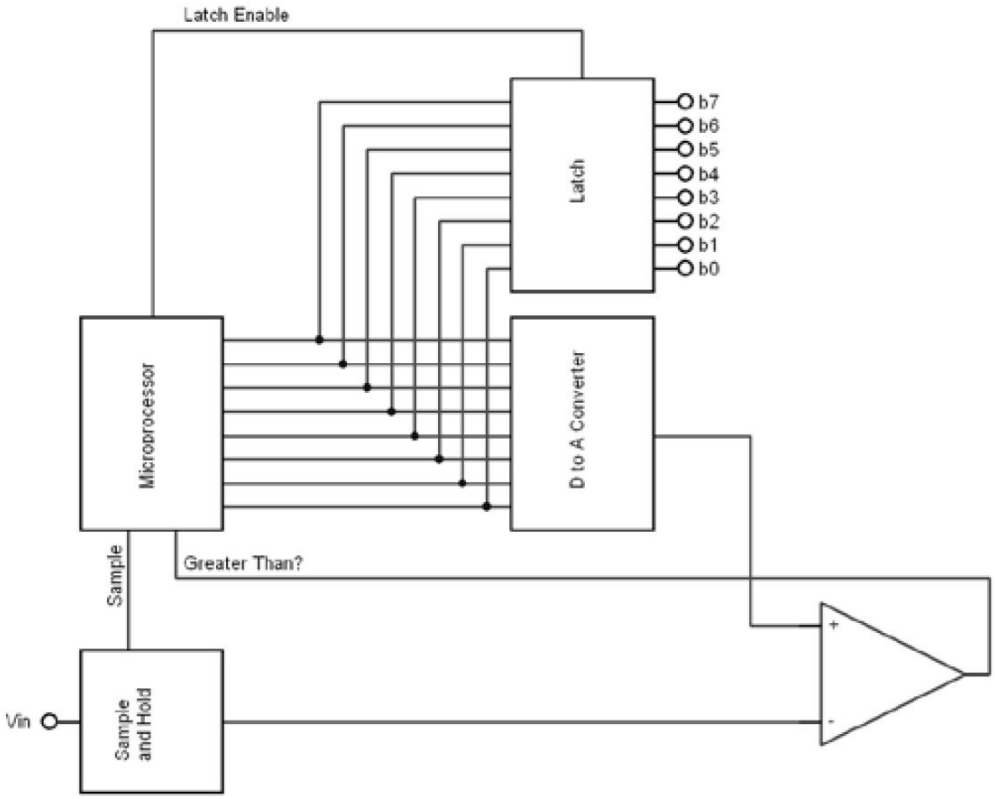
How many samples per second would an 16-bit Fast Ramp Converter be able to make, again in megasamples per second? (Start by determining how many different voltage levels there are in a 16-bit ramp.) _____ MSa/s

That's significantly slower.

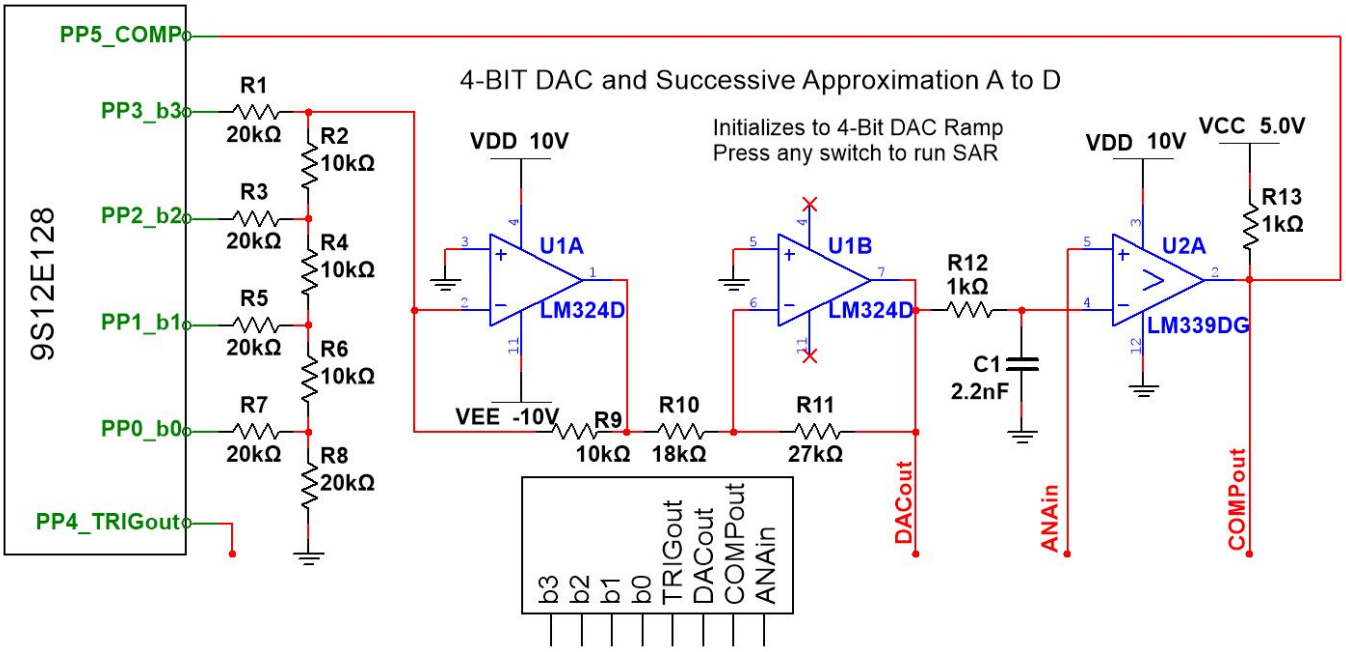
Successive Approximation

The happy medium between the two is a process called Successive Approximation, which is a smart guessing game. You could say that the Fast Ramp approach is a highly untelligent guessing game: Is it 0? No? Is it 1? No? Is it 2?, No? is it 3? Yes? Great; is it 4? No? is it 5? No? ....

The smarter way to go would be to split the field in half and pick the one with the answer in it, then split that half into quarters, etc. That's how a Successive Approximation A to D Converter works. The hardware looks pretty similar to the Fast Ramp, except for the addition of some "brains". By the way, a Successive Approximation A to D Converter is often referred to as an SAR, short for Successive Approximation Register, since the results are presented to the data bus for storage using a latching register.



Here's a 4-bit Successive Approximation DAC built up on one of the microcontroller boards from a few years ago.



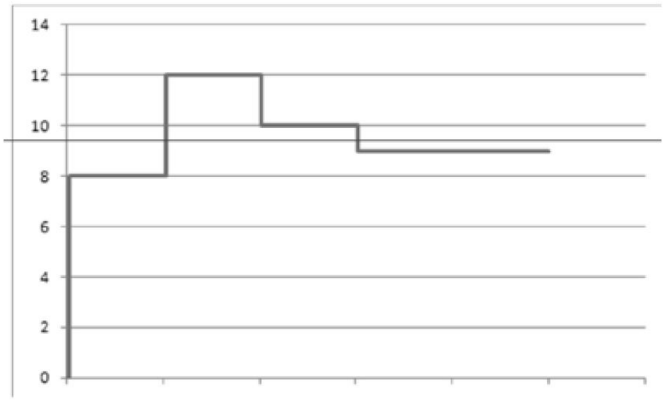
For this simple application, the Sample and Hold Circuit was left out, an omission which introduces significant error at higher frequencies.

The microprocessor on the left can generate any of the binary values from 0000 to 1111, which it sends into the R-2R ladder at the front end of the DAC. The R-2R ladder feeds into an inverting summing amplifier followed by a second inverting amplifier to generate a positive output. Next is a single-pole Low Pass Filter to reduce switching noise. After that comes the comparator. One of its inputs is the Analog signal, the other input is the DAC output. The comparator sends its binary output back to the microprocessor so it can make decisions based on whether the analog signal is greater or less than the DAC output.

For the fun of it, and for review, let's determine the step size. If all the outputs except the MSB are zero, then 5.0 V is presented to the summing amplifier through a 20 kΩ resistor. Since the feedback resistor is 10 kΩ, this means that the output of U1A will be -2.5 V. Multiplying that by the gain of the second amplifier, we calculate an output voltage of 3.75 V. Since this represents binary 1000 (only the MSB set), we divide by eight to get a step size of 468.75 mV/step. Bizarre value, but we'll live with it.

Successive Approximation Process

To simplify the analysis, let's instead start with an A to D converter with a step size of 1.0 V/step. The following picture shows the process of digitizing an input of 9.437 V.



To begin with, the microcontroller sets just the MSB to produce the binary code 1000 and, given a step size of 1 V/step, an output voltage of 8.0 V. Since this output is lower than the analog signal, the microcontroller keeps the MSB.

Now the microcontroller sets the next bit to produce the binary code 1100 and an output voltage of 12.0 V. Since this output is higher than the analog signal, the microcontroller clears this next bit.

Now the microcontroller sets the second last bit to produce the binary code 1010 and an output voltage of 10.0 V. Again, this output is higher than the analog signal, so the microcontroller clears this bit.

Finally, the microcontroller sets the LSB to produce the binary code 1001 and and output voltage of 9.0 V. Since this output is lower than the analog signal, the microcontroller keeps this bit, and presents its final guess as binary 1001. When played back by a DAC, this value will produce an output of 9.0 V instead of the original 9.437 V, again losing accuracy due to Quantization Error.

Let's compare the speed of a 16-bit Successive Approximation A to D Converter to the two previous converters, again assuming a clock pulse of 1 ns duration.

The Direct Conversion A to D could produce 1 billion samples in a second, or 1000 MSa/s

The Fast Ramp A to D took 65,536 clock cycles per sample, resulting in a pathetic 0.015 MSa/s

The Successive Approximation A to D takes _____ clock cycles for 16 bits, resulting in a rate of _____ MSa/s. It's not super-speedy like the Direct Converter, but also it doesn't need a circuit with over 60,000 comparators and over 60,000 logic inputs; and it's definitely much faster than the Fast Ramp,with hardly any more circuit complexity.

Here are a couple of questions to finish up.

Match each of the following descriptions to the most likely 8-bit A to D converter.

_____

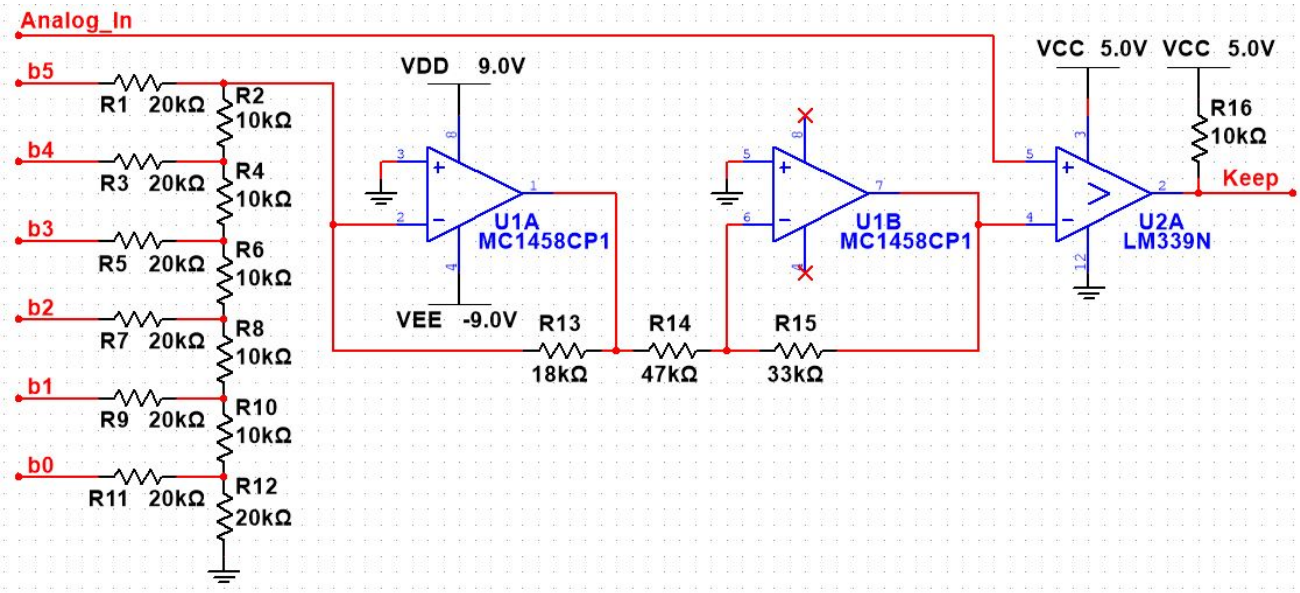
How many conversion steps would be required for a 12-bit A to D converter using each of the technologies listed?

Direct Conversion: _____

Fast Ramp Conversion: _____

Successive Approximation: _____

Worked Example -- Successive Approximation A to D



We'll start with an overview of the circuit:

- There are six digital inputs, all of which are driven by 3.3 V LVTTL signals from a microcontroller (not shown)
- With six digital inputs, there are 2^6-1 steps, or 63 steps
- The inputs are handled by an R-2R ladder DAC, which should therefore be a linear binary-weighted DAC, with b5 as the MSB
- The two op amps in the DAC are both inverting, so the output voltage will always be zero or positive; hence, there is no need to clamp the input to the comparator
- When the analog signal is greater than the DAC output, the most recent "guess" should be kept; given that the analog input is connected to the non-inverting input, this means that a high output from the comparator indicates "keep"

To determine the step size for an R-2R ladder DAC, we set the MSB and clear all the rest, giving us a binary 100000, or decimal 32. In this state, none of the lower bits contribute any current to the circuit's input, so we can determine the expected output for 32 using the gains of the two amplifiers:

$$V_{32} = 3.3\left(-\frac{18\ k\Omega}{20\ k\Omega}\right)\left(-\frac{33\ k\Omega}{47\ k\Omega}\right) = 2.085\ V$$

The step size, therefore, is

$$Q = \frac{V_{32}}{32} = 65.2\ mV/step$$

The maximum output for 63 steps (binary 111111) would be 4.105 V

It's likely that the intent was for this DAC to have a range from 0 V to 4.095 V, and a better design would include a potentiometer in the op amp feedback to allow for some adjustment. For simplicity, let's work with the ideal step size:

Q=65 mV/step

From this, the voltage for binary 100000 would be 2.080 V and the output for binary 111111 would be 4.095 V.

Let's watch the process for the A to D converter digitizing the analog value 1.8702 V:

Binary (Decimal)	Voltage	Comparator
100000 (32)	2.080 (too high)	Don't Keep
010000 (16)	1.040 (too low)	Keep
011000 (24)	1.560 (too low)	Keep
011100 (28)	1.820 (too low)	Keep
011110 (30)	1.950 (too high)	Don't Keep
011101 (29)	1.885 (too high)	Don't Keep

Therefore, the final result is binary 011100, or 28 decimal, which produced the value 1.820 V -- a voltage that's less than one step below the analog input value of 1.8702 V.

In this example, it's fairly clear that 011101 or 29 produces 1.885 V which is actually closer to the analog input than the final result arrived at by this A to D converter. It's for this reason that a more sophisticated A to D converter would add half a step to the input voltage, bumping it up to 1.903 V, in which case the last bit would have resulted in "Keep", and the final answer would have been binary 011101, or decimal 29.

Online Homework System

Assignment Worksheet
5/31/21 - 2:13:38 PM MDT

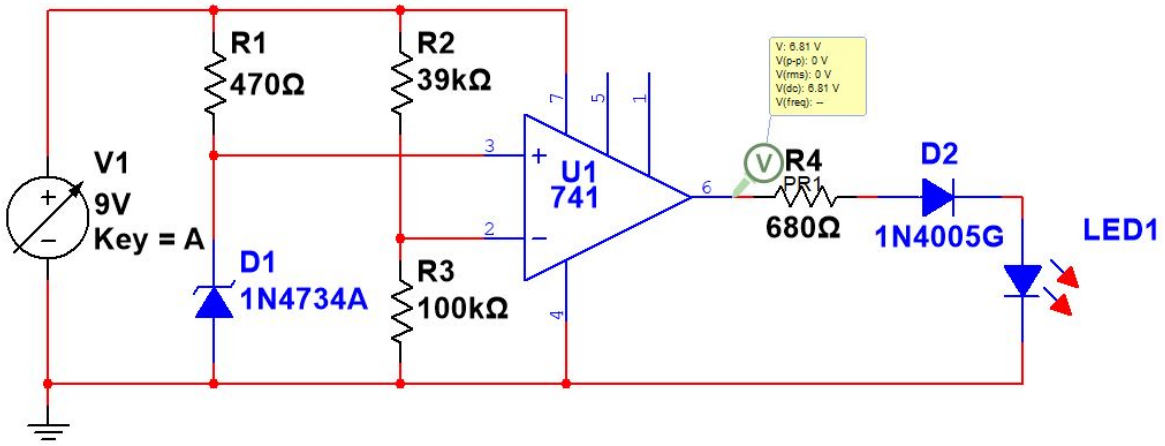
Name: _____ **Class:**

Class #: _____ **Section #:** _____

Instructor: Ross Taylor **Assignment:** SA18 Non-Zero Crossing Detector Activity

Question 1: (10 points)

Analyze the “Low Battery Indicator” design below according to the information that follows.



In a previous exercise, you had the opportunity to analyze a circuit like this using a dedicated comparator, the LM339. However, it may not always be the case that you have the "right" component available for the job. The 741 op amp is not a “rail-to-rail” device and is not intended for single-supply use as in this application, but it is readily available. With a few extra considerations, it can be used as a Low Battery Indicator. Since the output does not go to either the positive or negative rale, when the output is supposed to be “LOW”, it is likely to be more like about 1 or 2 V. Diode D_2 is installed to provide an additional voltage drop to prevent LED_1 from glowing dimly when it is supposed to be off.

From the data sheet for zener diodes, determine the reverse breakdown voltage for the 1N4734A zener diode, and from that predict the voltage expected at pin 3 of the op amp when the circuit is working properly: _____ V.

Determine the theoretical voltage of V_1 at the point at which the output of this circuit will change state (i.e. the "battery" voltage at the point when the inverting input's voltage is the same as the non-inverting input's voltage): _____ V.

Based on the configuration of the comparator, when the voltage is lower than what you calculated above, the LED with be:

(a) On

(b) Off

In Multisim, build the circuit. V_1 is a DC_INTERACTIVE_VOLTAGE source, and emulates a 9 V battery. Set this supply voltage initially to 9.0 V_{DC} and change its Increment to 1% to allow for finer control. Slowly decrease the supply voltage until the LED changes state as predicted above. Record this "dead battery" voltage: _____ V.

Verify that your circuit is working properly: When the "battery" is officially "dead", the LED is:

(a) On

(b) Off

Now, let's check the non-ideal output characteristics of the 741 op amp:

When the "battery" is at 9.0 V, the output, in volts, at pin 6 is _____ V

When the LED first lights, the output, in volts, at pin 6 is _____ V

Put a current probe on the output circuit. When the LED is OFF, the current is _____ mA

When the LED is ON, the current is _____ mA

One final check: A good battery monitor circuit shouldn't drain any current from the battery when it is "good". Put a current probe on the output of V1. How much total current does this circuit draw when the battery is at 9.0 V? _____ mA

Apparently, this circuit is not very impressive, particularly if the device for which it is checking the battery sits on the shelf most of its life. About half of the current draw is to keep the Zener diode reverse biased, and the other half is wasted by the 741 op amp, which has an unusually high "quiescent current". There are much more efficient op amps available for applications like this, but if you were picking a different IC, you might as well pick a dedicated comparator anyway!

Online Homework System

Assignment Worksheet
5/31/21 - 2:16:01 PM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA19 Comparators and AtoD Quiz

Question 1: (1 point)

When analyzing comparator circuits, it is important to use the op amp model which states that the voltage difference between the two input pins should be considered as zero at all times.

(a) True
(b) False

Question 2: (1 point)

A comparator circuit answers the question "Is the non-inverting input at a more positive voltage than the inverting input?"

(a) True
(b) False

Question 3: (1 point)

If the non-inverting input of a comparator is connected to a +1.05 V signal and the inverting input is connected to a +1.06 V signal,

(a) The output voltage will be at the maximum negative voltage.

(b) The output will be at the positive maximum voltage.

(c) The output with be at a positive voltage smaller than the maximum.

(d) The output will be at a negative voltage smaller than the maximun.

Question 4: (1 point)

If the inverting terminal of a comparator is connected to ground and a signal is connected to the non-inverting terminal,

(a) The circuit is a non-inverting non-zero crossing detector.

(b) The circuit is an inverting non-zero crossing detector.

(c) The circuit is a non-inverting zero-crossing detector.

(d) The circuit is an inverting zero-crossing detector.

Question 5: (1 point)

Which statement is true?

(a) Analog signals, unlike digital signals, can be effectively filtered to remove noise prior to re-transmission.

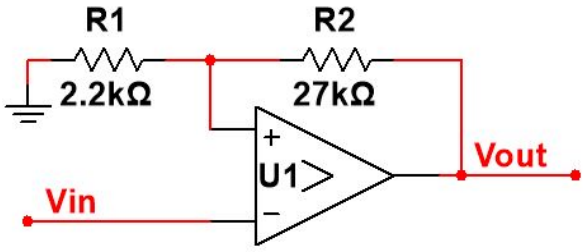
(b) Analog and digital signals can be equally regenerated and amplified for accurate re-transmission.

(c) Digital signals, unlike analog signals, can be accurately regenerated, removing noise prior to re-transmission.

(d) Digital signals and analog signals are equally affected by noise and cannot accurately be re-transmitted.

Question 6: (2 points)

Consider the following circuit for the questions below.



This circuit could be describe as

(a) A comparator with hysteresis for noise rejection.

(b) A non-inverting zero crossing detector.

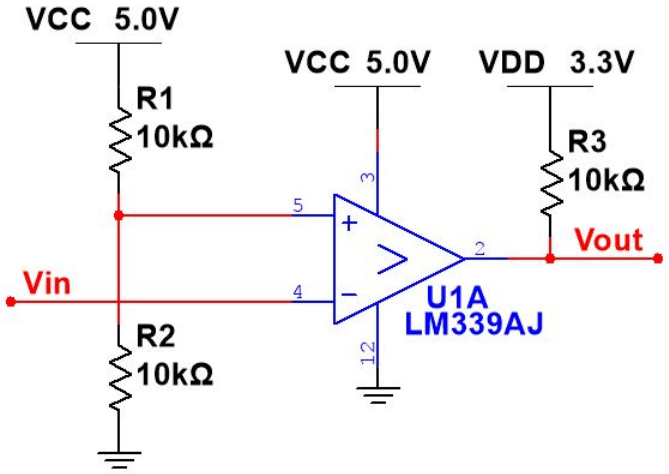
(c) An amplifier with a gain of +13.3.

(d) An amplifier with a gain of -12.3.

If V_{out} switches between +9 V and -9 V, how much additional noise suppression would this circuit demonstrate as a result of the resistor network? _____ $V_{p\text{-}p}$.

Question 7: (2 points)

Consider the following circuit to answer the question below:

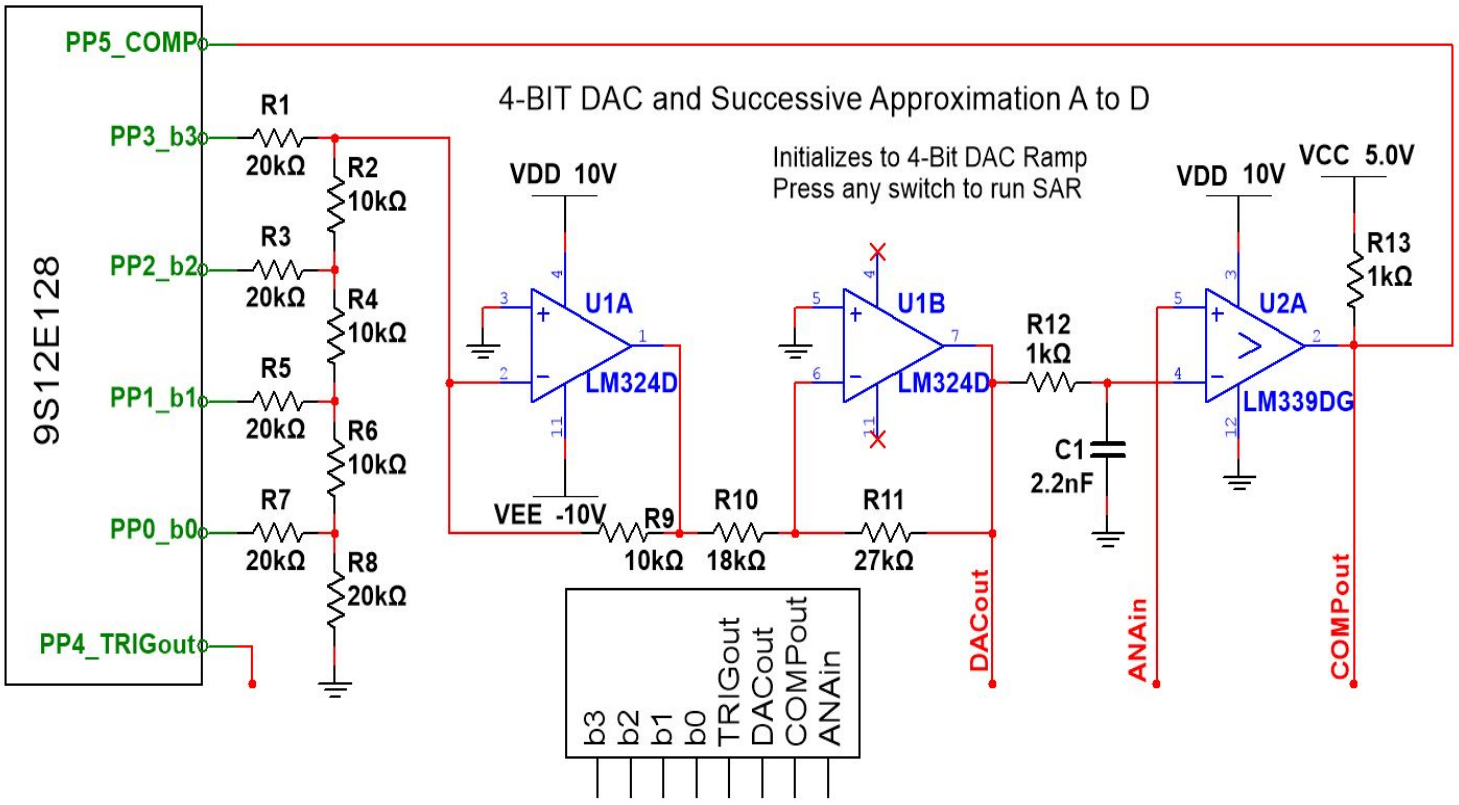


If V_{in} = +2.3 V, what voltage is expected at V_{out}? _____ V.

If V_{in} = +3.3 V, what voltage is expected at V_{out}? _____ V.

Question 8: (3 points)

Consider the following circuit for the questions below.



Determine the step size for the DAC component of this circuit, given that the digital outputs from the 9S12E128 switch between 0 V and +5 V. Provide your answer in millivolts. _____ mV.

What binary code would be expected for an input analog signal of 4.23 V? _____

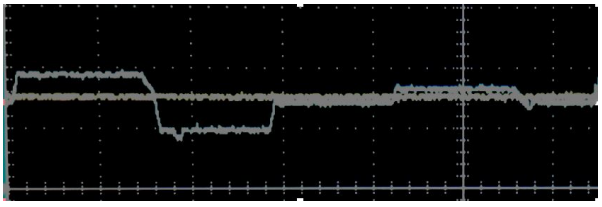
If the DAC output signal is smaller than the analog input, the comparator will indicate a HIGH to the microcontroller.

(a) True

(b) False

Question 9: (1 point)

Consider the following screen capture from a 4-bit Successive Approximation A to D converter to answer the question below.



Given that the fifth segment of the conversion indicates the decision regarding the fourth comparison, what digital value represents the voltage analyzed in this sample? _____

Question 10: (1 point)

How many processing steps would a 10-bit successive approximation A to D converter take to complete a sample? _____ .

Question 11: (1 point)

How many processing steps would a 10-bit fast ramp A to D converter take to complete a sample? _____ .

Online Homework System

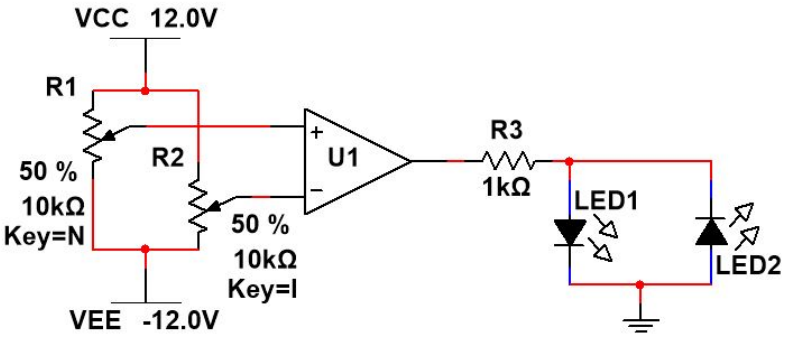
Assignment Worksheet
11/12/22 - 6:33:33 PM MST

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Lab08 Comparator Circuits

Question 1: (10 points)

Simple Comparator

Use the partial schematic below to answer the questions that follow.



When the voltage at the inverting pin is +1 V and the voltage at the non-inverting pin is -2 V, which of the LEDs will glow?

(a) LED1

(b) LED2

(c) Both

(d) Neither

When the voltage at the inverting pin is -10 V and the voltage at the non-inverting pin is -8 V, which of the LEDs will glow?

(a) LED1

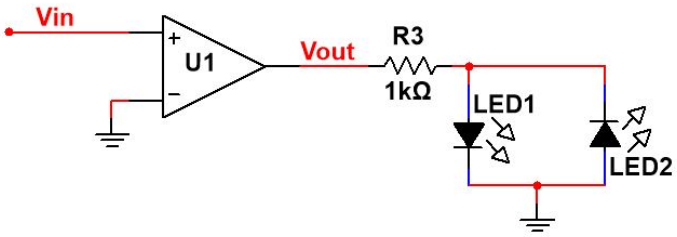
(b) LED2

(c) Both

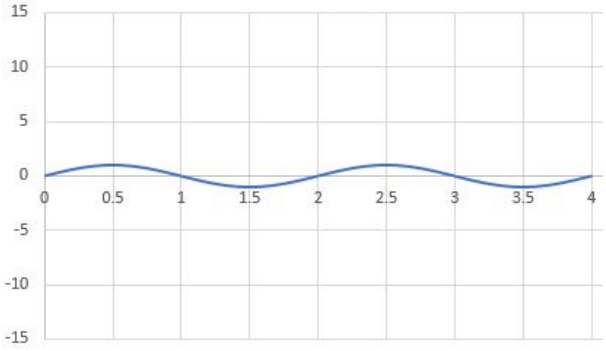
(d) Neither

Zero Crossing Detector

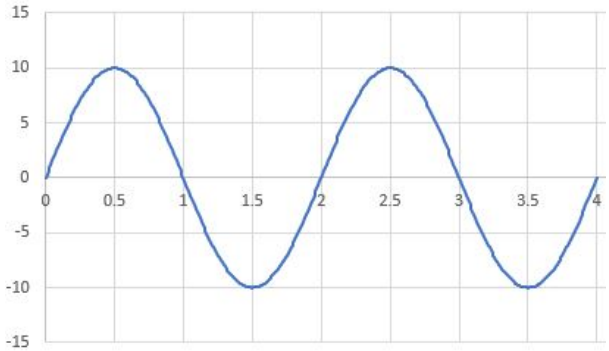
Use the partial schematic below to answer the questions that follow.



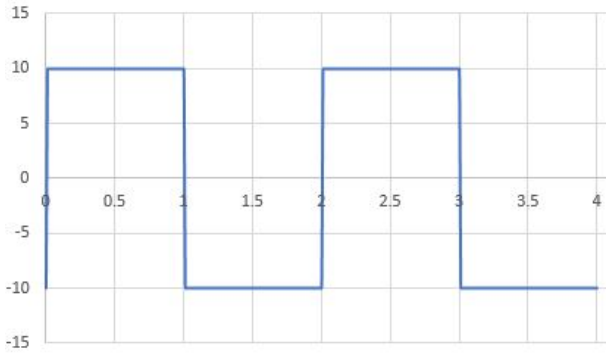
If the input signal, V_{in}, looks like the following, what do you expect to see at V_{out}?



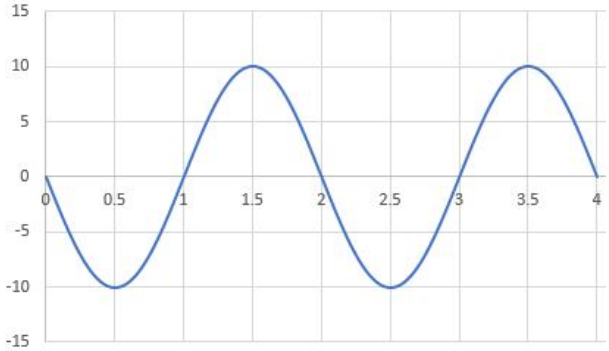
(a)



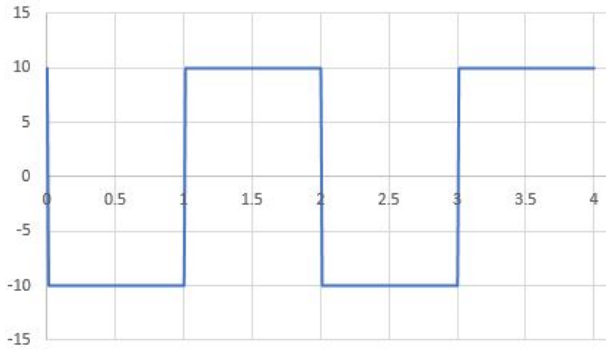
(b)



(c)



(d)



When V_{in} is positive, which of the LEDs will glow?

(a) LED1

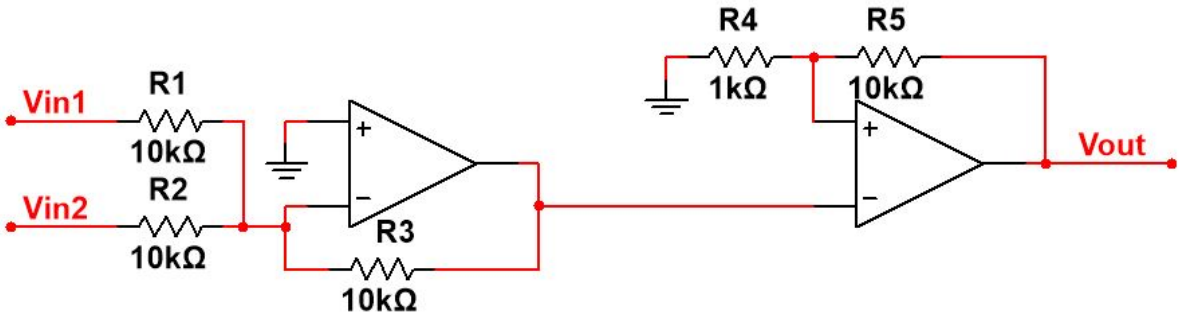
(b) LED2

(c) Both

(d) Neither

Zero Crossing Detector with Hysteresis

Use the partial schematic below to answer the questions that follow. In this circuit, the first op amp stage is a summing amplifier, allowing us to combine a "digital pulse" with "noise" to simulate a binary signal degraded from transmission over a distance.



If the output switches from +11 V to -11 V, what is the positive threshold voltage expected at the non-inverting input of the second op amp? _____ V

Again, if the output switches from -11 V to +11 V, what is the negative threshold voltage expected at the non-inverting input of the second op amp?

_____ V

What improvement in noise rejection would you expect from this circuit, as compared to a simple zero crossing detector? Give your answer in peak-to-peak volts. _____ $V_{p\text{-}p}$

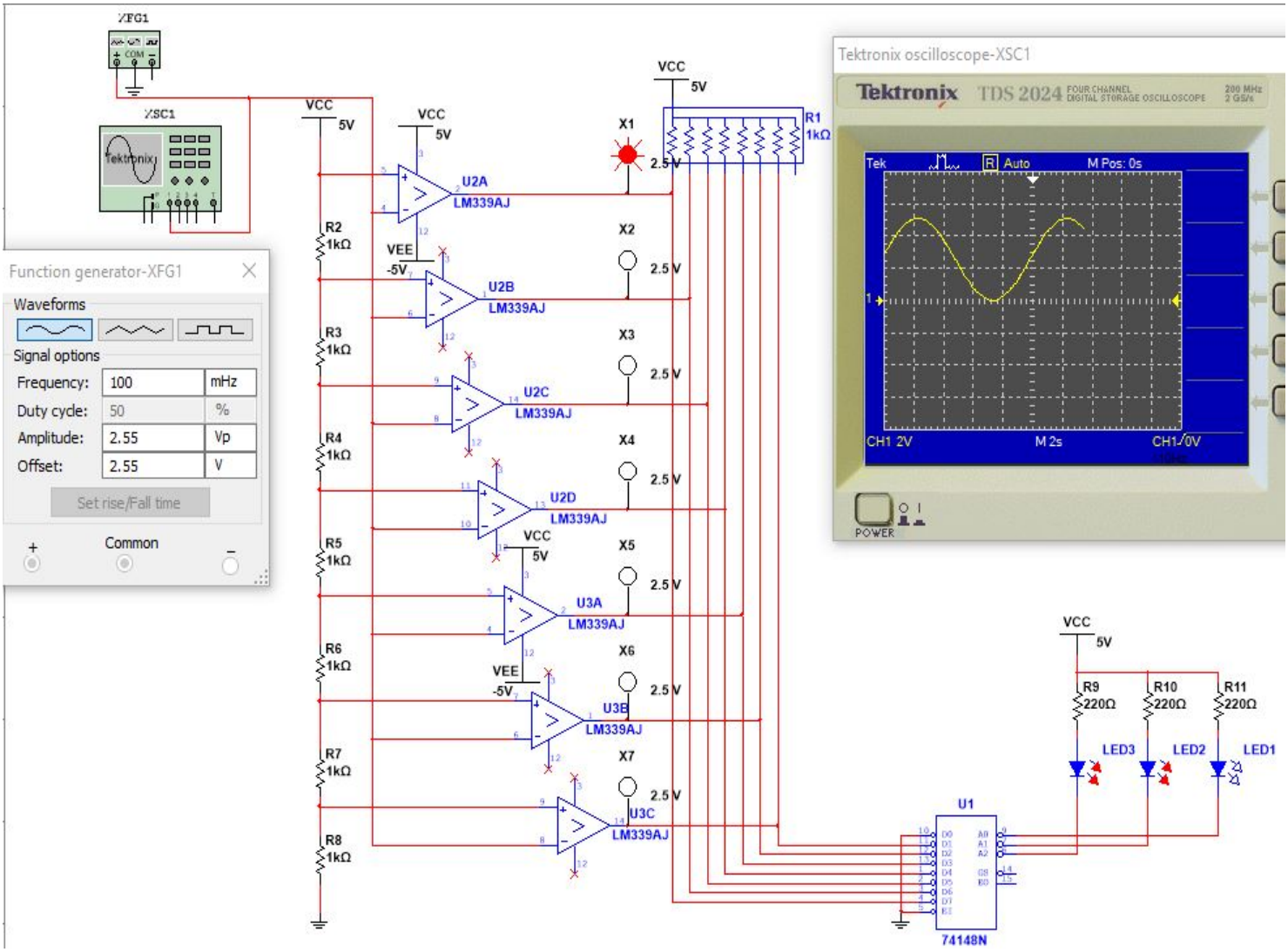
Direct Conversion A to D

The circuit below is a 3-bit Direct A to D Converter -- a reminder of the hardware complexity of Direct Converters. If this is a 3-bit converter, imagine what an 8-bit converter would look like, with 255 comparators!

The 74148 is a Priority Encoder, which generates a binary code to indicate the highest valued active input. For example, if bit 5 is active, it doesn't matter what combination of bits 0 to 4 are active, the output will represent 5.

The complication with the 74148 is that it is "inverse logic". "Active", both for inputs and outputs, means "LOW", so a string of "HIGHs" is the equivalent of 00000000 at the inputs or 000 at the outputs. As long as we're aware of this oddity, we can use the IC. We just need to drive things LOW when we want them to be "1", and use LOWs to generate "1s" when we need them.

Consequently, the comparators are all set up in inverting configuration, so that when they are inactive, their outputs will be HIGH, and when activated, their outputs will be LOW. At the output side, when a pin goes LOW, we've connected it to an LED that will come on to indicate we have a "1". That's NOT NOT NOT a problem, is it?



From the voltage divider at the inputs of the comparators, determine the step size, in millivolts per step: _____ mV/step

If the input signal is 3.2 V, what binary combination do you expect to see on the LEDs, with the MSB to the left? _____

The output of U2D when Vin = 3.2 V should be HIGH

(a) True

(b) False

You have now finished the Pre-Lab. Move on to the Lab Activities. Do not click "submit" yet!

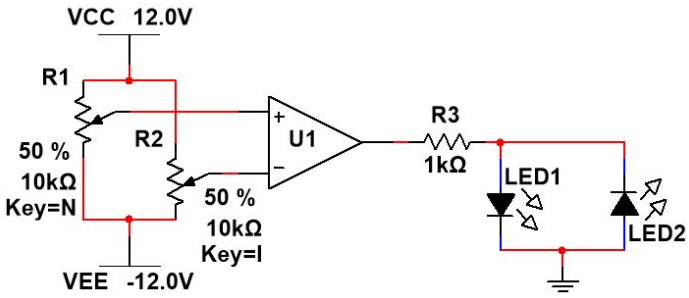
Question 2: (10 points)

Simple Comparator

On your breadboard, build a fully-working circuit based on the partial circuit from the Pre-Lab, shown below.

- Use half of a 1458 op amp.
- Power the op amp and the variable voltage dividers using a +/- 12 V_{DC} power supply.
- Use a GREEN LED for LED1 and a RED LED for LED2.
- Use single-turn (not multi-turn) potentiometers for R1 and R2 to save adjustment time.

Notice that, in this application, the potentiometers are configured as "Variable Voltage Dividers", with the centre sweeper as the output. You've previously used potentiometers as variable resistors (rheostats) by shorting one end to the sweeper.



Use the two channels of an oscilloscope (DC-coupled) to track the voltages on the inverting and non-inverting pins of the op amp. Set the potentiometers so that the input voltages are approximately as shown in the table below, and indicate which LED lights for each combination of inputs.

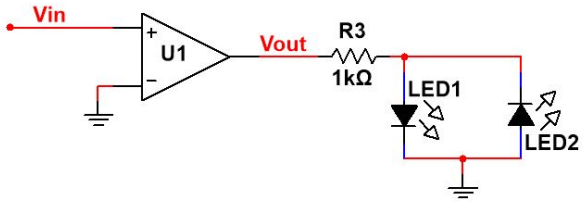
Inverting Pin Voltage	Non-Inv Pin Voltage	Which LED?
+1 V	-2 V	_____
+2 V	+3 V	_____

Zero Crossing Detector

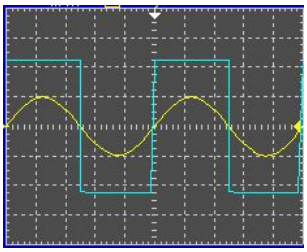
Modify your circuit so it matches the functionality of the following partial schematic. Use a signal generator to provide Vin, with the following initial settings:

- Sine Wave
- 1.0 V_p
- frequency 1.0 Hz (i.e. really slow, so you can see the activity on the LEDs)
- no DC offset

Use oscilloscope Channel 1 to observe V_{in} and Channel 2 to observe V_{out}.



Ask your instructor for a grade out of one mark. Make sure the function generator is set correctly and that your input and output signals are clearly visible on screen -- set them to the same vertical attenuation for good comparison. If you've adjusted the oscilloscope properly, you should see something like this on its display:



_____

Now, reduce the amplitude of the input signal to 50 mV_p. True or False: This comparator can still tell when the signal is positive and when it is negative.

(a) True

(b) False

Zero Crossing Detector with Hysteresis

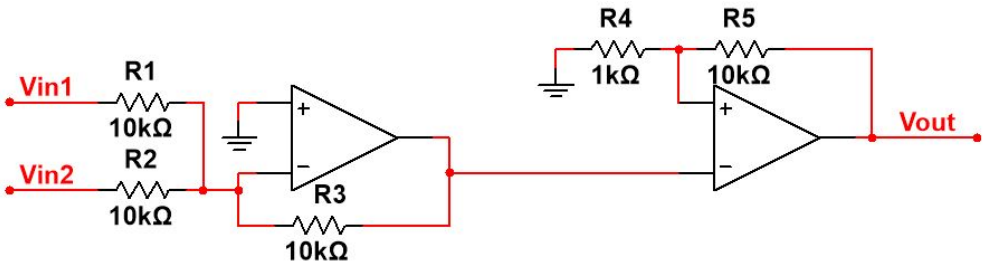
Modify your circuit as shown below, using the second op amp in the 1458 IC you installed earlier.

For V_{in1}, which represents a digital signal, set Channel 1 of the signal generator to produce a 1.0 kHz square pulse with an amplitude of 1.5 V_p (i.e. 3.0 $V_{p\text{-}p}$) and no DC offset.

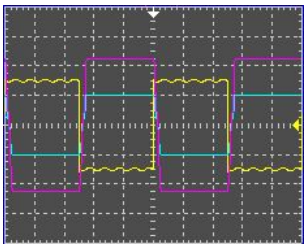
For V_{in2}, which represents noise, set Channel 2 of the signal generator to produce a 10 kHz sine wave, initially set to 100mV_{p-p} with an offset of 0 V.

Use oscilloscope channels to monitor the following:

- Channel 1 -- the output from the summing amplifier (i.e. the input to the comparator)
- Channel 2 -- the comparator output



Ensure that your circuit is working and you've adjusted the oscilloscope to adequately view both signals, but use the same vertical attenuation for both channels for best comparison. You should see something like the yellow and violet traces in the following screenshot (the blue trace is the threshold voltage, which unfortunately you won't be able to see simultaneously with only a two channel oscilloscope; later you will momentarily observe it using channel 2 to see its effect on noise immunity):



Set the oscilloscope trigger source to Channel 2 -- the output signal -- since the input signal is going to have a lot of "noise" on it eventually.

Now, slowly increase the "noise" signal until the circuit output starts to display unwanted transitions. Record the amplitude of the noise signal here, in peak-to-peak volts. _____ V_{p-p}

Temporarily move the oscilloscope Channel 2 probe to observe the threshold voltage on the non-inverting pin of the comparator (second op amp). With the input signal channel and the threshold channel set to the same vertical attenuation, you should see that the noise just "fits" inside the threshold signal -- in other words, the output starts to fail when the noise touches the threshold.

Disable the Hysteresis

To determine how much improvement this is over a simple zero crossing detector, we will now disable the hysteresis. To do this, simply ground the non-inverting terminal of the comparator -- now your circuit is a zero crossing detector.

Return oscilloscope Channel 2 to the output of the comparator.

Decrease the noise until the output signal just returns to being a clear square pulse again.

The noise should be just touching the zero line, as would be expected for a simple zero crossing detector.

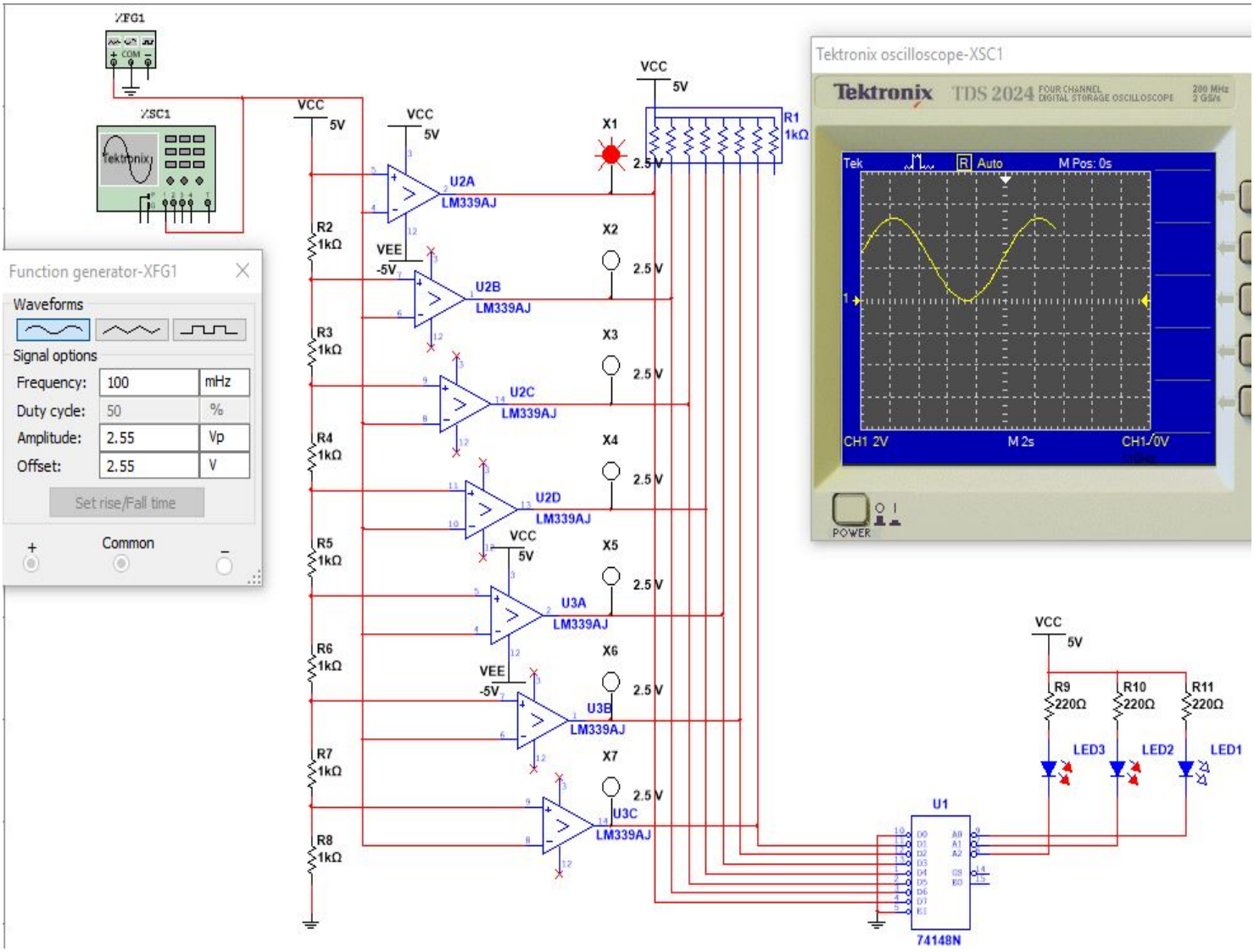
Record the amplitude of the noise signal in peak-to-peak volts. _____ V_{p-p}

The improvement in noise rejection, in peak-to-peak volts, for the circuit with hysteresis is, therefore, _____ V_{p-p}.

Direct Conversion A to D

Using Multisim, build and test the following circuit. Note the following:

- The LM339 is a quad comparator, so there are only two ICs -- make sure you power them both. If all goes well, the other comparators in the IC will show a red 'x" on each power and ground pin.
- The resistor 8-pack is available under Basic->RPACK. It is an 8Line-Bussed, meaning that internal to the IC, each resistor is connected at one end to a bus wire, as shown in the schematic symbol.
- The 74148 is available from TTL. Note that all the inputs and regular outputs have bubbles.
- Select the three LEDs at the output from Diodes->LED to ensure they work properly -- other indicators may not work.
- Set up the generic function generator as shown in the screen-shot below, to produce a very slow sine wave with a DC offset that makes it all positive.
- The logic indicators on the comparator outputs are from "Indicators -> PROBE -> PROBE_DIG_RED".
- Use the Tektronix Oscilloscope to observe the input analog signal. Adjust it so you can see the sine wave clearly (if you want, you can use the settings seen on the screen, but it's a good challeng to see if you can get this to work on your own).



Watch the input signal while observing the logic probes and the LEDs. Once you are satisfied that the binary output represents the input signal voltage adequately, record the following sample for grading. Replace the function generator with a DC_INTERACTIVE_VOLTAGE set to make V_{in} = 3.2 V. (Note that the LSB of the 74148 is connected to ground. Also recall that "active" means LOW for the 74148.)

V_{in}, V	Highest Active Input Bit	Binary output
3.2 V	_____	_____

Adjust the input voltage until the output just switches from 000 to 001 (i.e. find the first step). From this, what is the step size, in mV/step? _____ mV/step

You have now completed this Lab. Click "Submit" to send out your work for grading.

Online Homework System

Assignment Worksheet
6/7/22 - 1:53:12 PM MDT

Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** SA20 Comparators Pump Control Activity

Question 1: (20 points)

Pump Control using Comparators and R-S Flip-Flop

This exercise will be somewhat challenging from the point of view of circuit building, so the analysis of it will be kept to a minimum. However, you should make sure you understand the logical development of the various aspects of this circuit.

Pump operation typically involves a certain amount of "hysteresis", or a difference in either level or pressure between when the pump turns on and when it turns off. Without this hysteresis, the pump would likely burn out at the set point, as tiny differences in level would start and stop the pump endlessly. So, whether it's a sump pump that comes on when the sump reaches a certain level then turns off when the sump is nearly empty, or whether it's a pressure tank pump that comes on when the level is low and shuts off when the tank is full, there will be a considerable difference between the settings to turn on and turn off the pump. In this exercise, we will emulate a pressure tank pump.

From a logical perspective, there are some obvious settings: when the pressure is equal to or greater than the upper set point, the pump must be OFF; when the pressure is equal to or less than the lower set point, the pump must be on.

However, in between those two settings, the condition of the pump depends upon its previous setting: if the tank was previously full and is now below its upper set point, it must remain OFF; however, if the tank was previously empty and is now above the lower setpoint, it must remain ON.

There are also impossible conditions, which would be "don't care" states, since the tank can't be both Full and Empty at the same time.

Here's a Truth Table for the pump motor. It would be wise of you to analyze this to see why the motor conditions, M(t), are what they are.

M(t-1)	F	E	M(t)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	X
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	X

From this, we can build a Karnaugh Map, making use of the "don't care" states to produce the simplest result. Again, take the time to arrive at this solution yourself.

	FE			
	00	01	11	10

M(t-1)	0	0	1	X	0
	1	1	1	X	0

The resulting expression for M(t) is:

$$M_{(t)} = E + M_{(t-1)} \cdot \bar{F}$$

In your Digital Logic course, you discovered that the only way to maintain a previous condition in memory was to use some form of Flip-Flop. The simplest of these is the R-S Flip-Flop, the Truth Table of which is shown below:

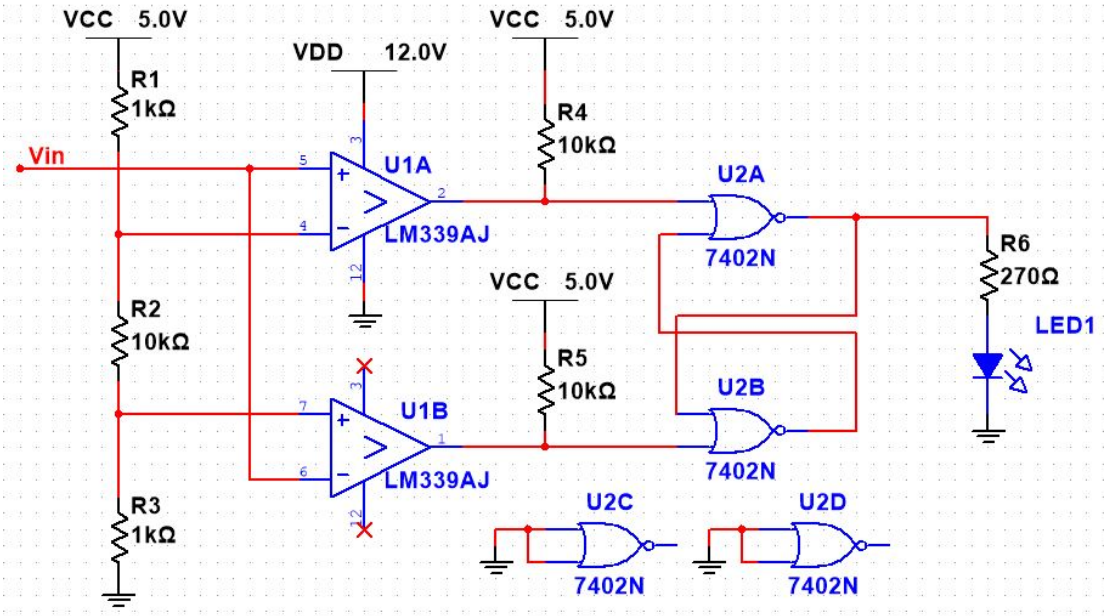
R	S	Q(t)
0	0	Q(t-1)
0	1	1
1	0	0
1	1	X

The first condition, where neither Reset nor Set are active, is the "Memory" condition, as the output will stay HIGH if it was previously HIGH, and will stay LOW if it was previously LOW. The second condition is the "SET" condition, the third is the "RESET" condition, and the last is the "ILLEGAL" condition, as it is impossible for the circuit to be both SET and RESET at the same time.

If, from our previous analysis and from the R-S Flip-Flop Truth Table we make S = E and R = F, we discover that the R-S Flip-Flop generates our desired M(t) functionality. In other words, if we can determine when the tank is Empty, we can use that sensor to drive the SET pin of the R-S Flip-Flop; if we can determine when the tank is Full, we can use that sensor to drive the RESET pin of the R-S Flip-Flop.

If the tank is empty, the motor will come on to fill the tank. If the tank is full, the motor will be off. If the tank is neither empty nor full, the previous condition comes into play: if the motor was previously off, it will remain off; and if the motor was previously on, it will remain on. Since it is impossible for the tank to be both full and empty at the same time, the "illegal" condition of the R-S Flip-Flop will never occur.

Consider the schematic diagram below to answer the questions that follow.



1. Using the voltage divider formula (or basic Ohm's Law principles), determine the voltage presented to Pin 4 of U1: _____ V

2. Also determine the voltage presented to Pin 7 of U1: _____ V
3. When Vin drops below the voltage on Pin 7 of U1, the R-S Flip-Flop will _____
4. When Vin rises above the voltage on Pin 4 of U1, the R-S Flip-Flop will _____
5. When the R-S Flip-Flop is SET, the LED, indicating the condition of the pump motor, will be _____

Circuit Build

Use a power supply to generate VCC.

With a circuit like this one, it is best to build it in stages to verify that each section works before adding more components.

Start with the Voltage divider.

6. Record the voltage between R1 and R2: _____ V
7. Record the voltage between R2 and R3: _____ V

Now, build the comparator circuit. The LM339 is in your CNT Year 1 Kit.

- Be really careful with the power pins -- they are in rather non-traditional locations!
- The pullup resistors must be installed before the "open collector" outputs of the LM339 will do anything. (If you want to prove this to yourself, after the comparators are working properly, temporarily remove the pullup resistors and see what happens.)
- Use a variable power supply to provide Vin. (If you use the Analog Discovery 2, use the "Basic" menu rather than the "Simple" menu to allow you better control of the voltage using the slider.)

8. Fill in the following table by setting the input to the desired voltages:

Vin, V	U1 Pin2 (RESET)	U1 Pin 1 (SET)
4.7	_____	_____
2.5	_____	_____
0.3	_____	_____

Next, build the R-S Flip-Flop. The schematic shows generic 7402 parts, but your kit contains 74HC02 parts, which you will use here.

- Look up the pinout -- Multisim doesn't include either the pin numbers or the power pins. Print out the schematic, and write suitable pin numbers on the inputs and outputs, and note the power and ground pins.
- Connect power and ground, and wire up the two gates in the R-S Flip-Flop.
- Notice that the two unused gates are also shown, with their inputs tied to ground. This is to meet the requirements of CMOS circuit design: never leave CMOS inputs floating, or they may rise to a voltage which will turn on both transistors in the output, thereby burning out the IC. Do NOT connect their outputs to anything!

You may wish to check the operation of the R-S Flip-Flop as you did the comparator earlier; however, the LED circuit is sufficiently simple that you should be able build it and use it to test the Flip-Flop.

So, add the LED circuit and check the operation of your entire circuit.

9. Fill in the following table:

Input condition	LED
Below the "Empty" voltage	_____
Between "Empty" and "Full", rising from "Empty"	_____
Above the "Full" voltage	_____
Between "Empty" and "Full", falling from "Full"	_____

Your circuit will be graded out of three marks. If you do this exercise at home, take a picture of your circuit board on the breadboard and upload it here. Do not use any spaces or special characters in the filename, but personalize it for easy identification as belonging to you. Document Upload (Direct) In the lab, ask your instructor to grade your work.

Online Homework System

Assignment Worksheet
4/19/23 - 1:01:24 PM MDT

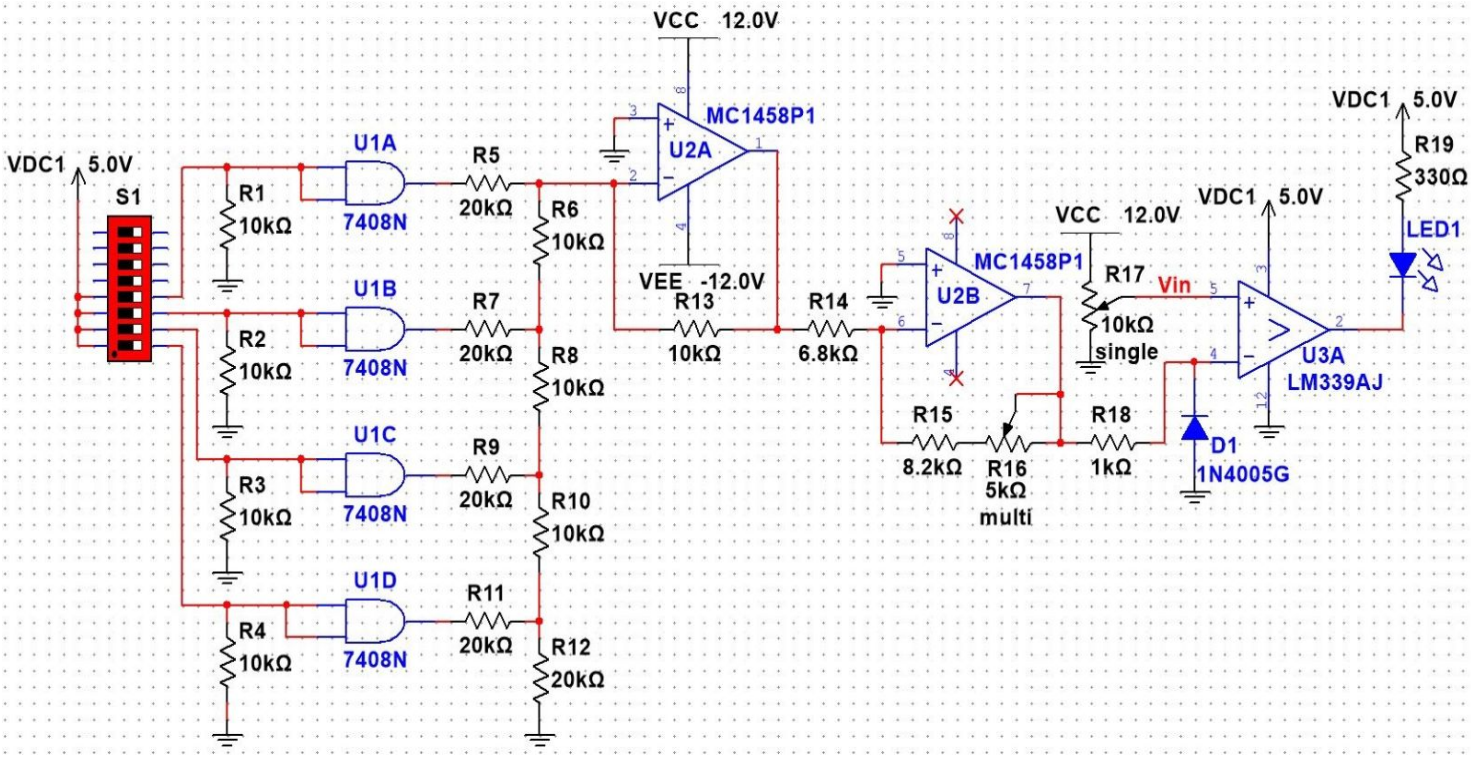
Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Lab09 SAR R-2R

Question 1: (10 points)

Lab 9 Pre-Lab

The circuit in this particular exercise is quite complex, so in the actual activity, the focus will be upon building and testing the circuit in stages to ensure that it is working properly. In the Pre-Lab, you will analyze the basic functionality so that you will know if your circuit is working correctly in the activity component.

Here is the completed schematic circuit for you to analyze.



Logic Inputs

To generate logic levels, we will be using the DIP switch from your CNT Year 1 Kit. In order to make a "Logic Switch" using a single-pole single-throw (SPST) switch, we can go two ways: an inverting configuration, in which the switch shorts the input to ground and, when the switch is open, a pull-up resistor raises the level to a Logic HIGH; or a non-inverting configuration, in which the switch shorts the input to Vcc and, when the switch is open, a pull-down resistor pulls the level to a Logic LOW.

1. By inspecting the circuit diagram above, it can be seen that the logic switch configuration chosen is _____

Unfortunately, for the type of DAC chosen for this exercise, it is important that the impedance between the ladder and ground for each input be a particular value -- in this case, 20 kΩ. Having an additional logic switch pull-down resistor between this input impedance and ground would make the DAC non-linear. In order to isolate the input from the pull-down resistor, a Buffer is required. We could use op amp Unity Gain Buffers for each channel (which would be a bit of overkill for this exercise), we could use Logic Buffer ICs (but you don't have any in your kits), or we could make our own logic-level buffers out of readily-available ICs, such as the 74HC08 AND gate.

2. If the two inputs to an AND gate are both LOW, the output will be _____ ; if the two inputs to an AND gate are both HIGH, the output will be _____ . Therefore, tying the inputs of an AND gate together turn it into a buffer.

The AND gate output impedance is sufficiently low that it will appear as an ideal voltage source, and will not affect the DAC inputs.

In your kits, you have a 74HC08 quad AND IC. There are a couple of issues you will have to deal with to use it in your circuit:

- Multisim doesn't include pin numbers in its schematic symbols for standard Logic Gates -- you will have to use the printable version of the schematic and write in the correct pin numbers for each of the gates.
- Multisim doesn't include the power and ground pins, but all ICs require power in order to operate; make sure you add these to your printable version.

Digital to Analog Converter (DAC)

This four-bit R-2R Ladder DAC uses the four highest inputs of the 10-pin SIP 10kΩ/20kΩ R-2R ladder used in a previous exercise -- you don't need to try to build up the R-2R ladder yourself; besides, you don't have any 20 kΩ resistors.

The intent is to produce a step size of 0.5 V/step for easy verification that the system is working. This is a fairly large step size, so the resolution of our DAC won't be very good.

We'll analyze the DAC as we did previously for the R-2R Ladder DAC when it was introduced in the course material, but working in reverse to determine the desired feedback resistance for U2B.

3. For the step size to be 0.500 V/step, with only the Most Significant Bit set, what is the expected output voltage at the output of the DAC, Pin 7 of U2B? _____ V. What is the gain for U2A, for just the MSB? (Don't forget the polarity!) _____ . What gain is required of U2B to produce the desired DAC output for just the MSB? (Don't forget the polarity!) _____ To achieve this gain, what should be the calibrated setting of the R15 + R16 gain-setting resistor pair? _____ kΩ. From this analysis, you should have proved that the chosen values of R15 and R16 place the desired resistance somewhere within the available range of resistance.

Comparator Circuit

The output of the DAC will be compared to the analog input, Vin, which is generated by the variable voltage divider potentiometer R17. Recall that the LM339 is an Open Collector device, meaning that its output is a transistor that needs to be pulled up by a resistor in order to establish a clear logic level. Instead, we will use the internal transistor as an LED driver to provide us with "Keep/Don't Keep" information about the bit we're checking.

4. The LED will glow when the LM339 output goes _____ . This means that the LED will glow when the DAC output is _____ than the Analog Input. Consequently, it probably makes sense to use a RED LED as the indicator to tell you the bit you've set shouldn't be kept for the final result.

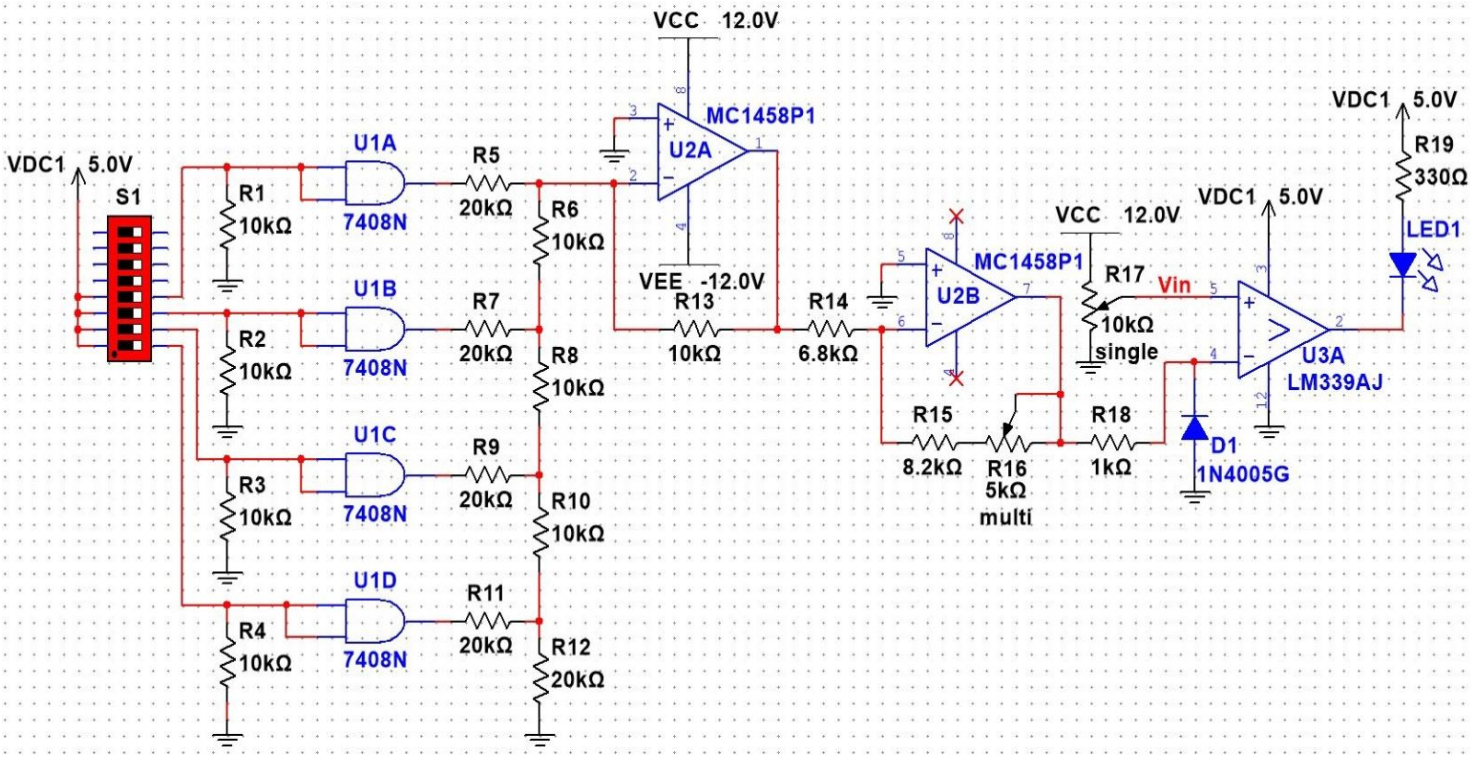
The Big Picture

5. Given the step size and the number of bits available, this Successive Approximation A to D Converter can handle analog input voltages up to _____ V.

You have now finished the Pre-Lab. Move on to the Lab Activities. Do not click "submit" yet!

Question 2: (10 points)

The Successive Approximation circuit for this Lab Activity is fairly complex, and should be built up in sections to ensure that each stage works properly. Here is the nearly-complete schematic for you to work from.



Logic Inputs

Begin by building and testing the binary Logic Input circuitry.

- Use the 8-position DIP switch found in your CNT Year 1 Kit
- Use the benchtop power supply to provide all three supply rails -- +/-12 VDC and +5 VDC; outside of the lab, a +/-12V PowerBRICK could be used, along with a +5 VDC source
- Use a single quad 74HC08 AND gate from your ETC Kit to create the logic buffers; as mentioned in the Pre-Lab:
  - You will need to assign pin numbers to the inputs and outputs according to the 74HC08 datasheet
  - You will need to power the 74HC08 from VDC1 (+5 VDC) to ground, using the pins indicated on the datasheet

1. Use your DMM to verify that each of the outputs of the 74HC08 is working as expected in response to changes in the DIP switch: When each switch is closed, the corresponding output voltage is _____ V; when each switch is opened, the corresponding output voltage is _____ V.

Successive Approximation R-2R Ladder DAC

This part of the circuit is difficult to break into smaller parts, so pay special attention to component selection and wiring.

- Use the **top** four inputs of the 4610X-R2R-103LF 10kΩ/20kΩ R-2R ladder SIP
  - Use Pin 1 as the output
  - Use Pins 2 through 5 as the inputs
  - Ground all the rest of the pins! This is necessary in order to create the final 20 kΩ connection to ground (you can verify that this works by doing a series-parallel analysis of the remaining resistor network with all inputs grounded)
- As an intermediate step, you can check the output of the first op amp (pin 1) as you try different combinations of the switches
- Once you have built up both op amp circuits, set all the inputs (i.e. all HIGH) and adjust the gain so that the output voltage at pin 7 is what you expect it to be for that particular input value.
- fill in the following table of sample values to demonstrate that the DAC circuit is working:

2. Sample DAC values

Digital input, Binary Notation	DAC Output, V
0000	_____
1000	_____
1101	_____

Analog Input

This one is simple -- it is being highlighted here so you don't miss it. Use a single-turn 10 kΩ potentiometer (a multiturn potentiometer would just slow you down unnecessarily).

Verify that its centre-tap can produce a suitable range of voltages (approximately 0 V to over 7.5 V).

Comparator and Indicator

Use the LM339 from your CNT Year 1 Kit and a RED LED

- Power both the LM339 and the LED circuit from VDC1 (+5 VDC)
- Pay careful attention to the pins used to power the LM339 -- this is not the most typical pinout, and incorrect power supply wiring will burn out the IC
- Verify that, by manipulating the DIP switches and the R13 potentiometer, you can turn the LED on and off

Final Test

Using your DMM and the special trim-pot screwdriver, use R17 to set the analog input, Vin, to approximately 4.7 V.

3. Fill in the following table to show how you arrive at the correct Successive Approximation of the digital representation of this voltage. If you need to, consult the associated Online Lesson to help you with the process.

Digital Input, Binary representation	LED	Keep/Don't Keep
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____

Final Digital Result, in binary representation: _____

5. Repeat this process for the following Analog Input voltages, and record the final Digital Results as Binary Representations:

Analog Input, V	Digital Result, Binary Representation
0.60	_____
3.75	_____
6.12	_____
7.39	_____

6. For a grade out of three marks, take a picture of your circuit with the switches set to show the LED glowing. Upload the picture here. Don't use any spaces or special characters in the filename, but personalize it for easy identification as belonging to you. If your instructor grades this in class, upload a text file indicating the grade assigned instead. Document Upload (Direct)

You have now finished this Lab. Once you submit your results, you will not be able to return to either this page or the Pre-Lab!

Online Homework System

Assignment Worksheet
11/22/22 - 8:45:37 PM MST

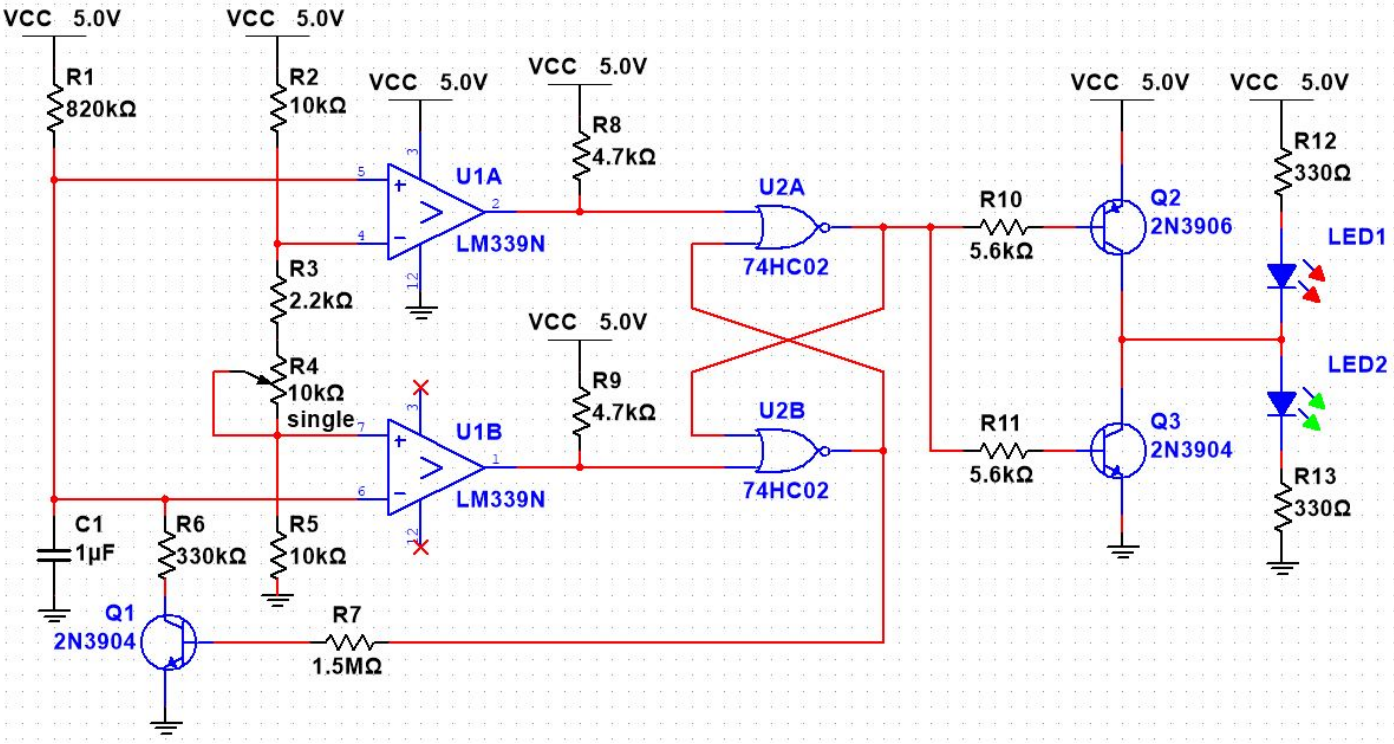
Name: _____ **Class:**
Class #: _____ **Section #:** _____
Instructor: Ross Taylor **Assignment:** Project 8 Comparators and A to D

Question 1: (50 points)

Circuit Analysis

Comparator Circuit

Everyone loves flashing lights, especially if they don't require software to make them run! In a previous exercise, you created a free-running oscillator with cross-coupled transistors that blinked a pair of LEDs. The following circuit does much the same thing, but this time using comparators and an R-S Flip-Flop. As an added feature, the frequency of oscillation is adjustable using a potentiometer. (Incidentally, this is a variation on a circuit used as a soldering practice board in another course. If you're interested, you might also want to compare this circuit to the functional components of an old standby IC that was used in the final project of the soldering course -- the 555 Timer.)



We'll analyze the various components of this circuit, based upon your current knowledge of electronics, then we'll build and test it.

1. ***Time setting R-C circuit:*** When Q1 is turned off, R1 charges C1, generating an approximation of a ramp (of course, it's really an exponential curve, but we'll use a simple straight-line approximation of the charging process). The average voltage at the node between R1 and C1 is 2.5 V under normal operation. What's the average current through R1, in microamps? _____ μA
2. Using $V_C = \frac{I \cdot t}{C}$, determine the charging rate in volts per second: _____ V/s
3. R2, R3, R4, and R5 make up a variable voltage divider. At each setting of R4, this voltage divider provides two different voltages to the two comparators -- one at the top of R3, the other at the bottom of R4.
    1. When the R4 sweeper is all the way to the bottom in the schematic, (i.e. when R4 is fully present in circuit), what voltage is applied to U1A Pin 4? _____ V. What voltage is applied to U1B Pin 7? _____
    2. When the R4 sweeper is all the way to the top in the schematic, (i.e. when R4 is shorted), what voltage is applied to U1A Pin 4? _____ V. What voltage is applied to U1B Pin 7? _____ V.

4. The timing for this circuit is based upon the time it takes to charge between the voltages in the ranges above, then to discharge back down.
    1. How long, in seconds, would it take to charge between the voltages expected when R4 is fully present (sweeper at the bottom), using the charging information determined above? _____ s
    2. How long, in seconds, would it take to charge between the voltages when R4 is shorted (sweeper at the top)? _____ s
5. When Q1 turns on, current flows through R6. Notice that R6 is approximately half the size of R1 -- when Q1 turns on, the discharge current from the capacitor and the continuous flow of current from R1 flow through R6, so at approximately half the size, R1 will conduct approximately twice the current -- all the current from R1 and an equal current from C1. That means that the discharge time should be approximately equal to the charge time. (The actual math for that is horrendous, so let's use this simple model!)
    1. Given that a full cycle is one charge and one discharge, what is the expected frequency of oscillation, in hertz, when R4 is fully present? _____ Hz
    2. What is the expected frequency of oscillation, in hertz, when R4 is shorted? _____ Hz

6. Now for the operation of the ***comparators***:
    1. When the capacitor voltage is less than the voltage on U1B Pin 7:

(a) The U1A output will be HIGH, and the U1B output will be LOW

(b) The U1A output will be LOW, and the U1B output will be HIGH

(c) Both the U1A output and the U1B output will be LOW

(d) Both the U1A output and the U1B output will be HIGH

    2. When the capacitor voltage is between the voltages of U1A Pin 4 and U1B Pin 7:

(a) The U1A output will be HIGH, and the U1B output will be LOW

(b) The U1A output will be LOW, and the U1B output will be HIGH

(c) Both the U1A output and the U1B output will be LOW

(d) Both the U1A output and the U1B output will be HIGH

    3. When the capacitor voltage is above the voltage of U1A Pin 4:

(a) The U1A output will be HIGH, and the U1B output will be LOW

(b) The U1A output will be LOW, and the U1B output will be HIGH

(c) Both the U1A output and the U1B output will be LOW

(d) Both the U1A output and the U1B output will be HIGH

7. Now for the ***R-S Flipflop memory cell:***

    1. When both of the inputs to the gates in U2 are LOW, the NOR R-S flipflop is in

(a) Set condition

(b) Reset condition

(c) Memory condition

(d) Illegal condition

2. When the output of U1A is HIGH and the output of U1B is LOW,

(a) the output of U2A will be HIGH and the output of U2B will be LOW

(b) the output of U2A will be LOW and the output of U2B will be HIGH

(c) both outputs of U2 will be HIGH

(d) both outputs of U2 will be LOW

3. When the output of U1A is LOW and the output of U1B is HIGH,

(a) the output of U2A will be HIGH and the output of U2B will be LOW

(b) the output of U2A will be LOW and the output of U2B will be HIGH

(c) both outputs of U2 will be HIGH

(d) both outputs of U2 will be LOW

4. Overall picture: When the capacitor voltage is greater than the inverting input of U1A, the output of U2A will be _____ , the output of U2B will be _____ , transistor Q1 will be _____ , and the capacitor will be _____ . When the capacitor voltage is less than the non-inverting pin of U1B, the output of U2A will be _____ , the output of U2B will be _____ , transistor Q1 will be _____ , and the capacitor will be _____ .

8. Finally, for the ***Totem pole LED driver:*** When the output of U2A is HIGH,

(a) LED1 will glow but LED2 will not glow.

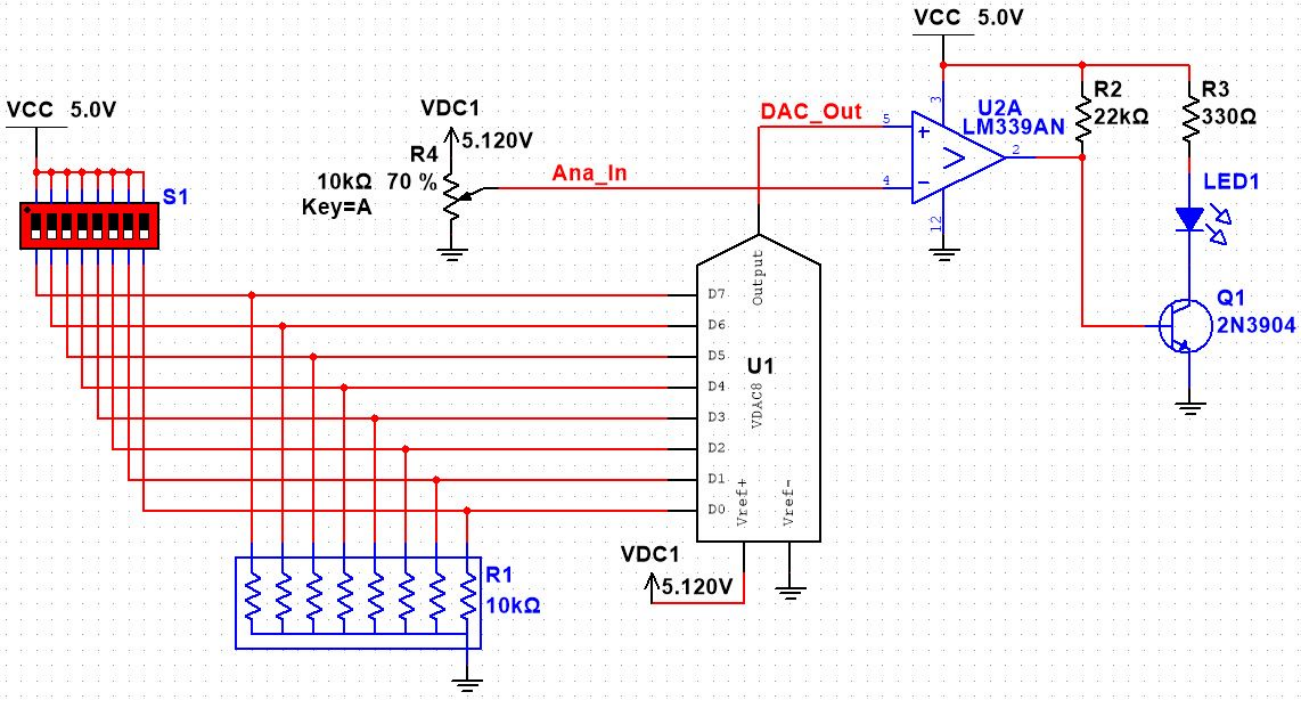
(b) LED1 will not glow but LED2 will glow.

(c) both LEDs will glow.

(d) neither LED will glow.

Analog to Digital Converter

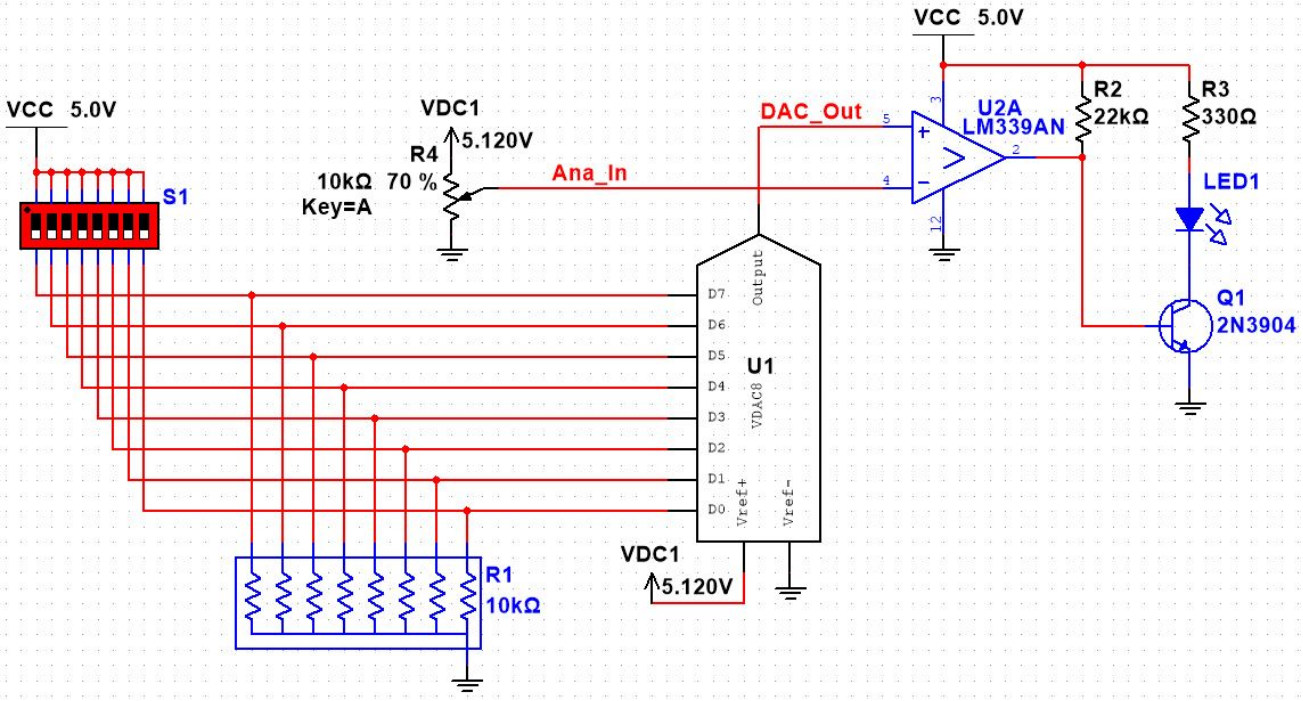
Consider the following schematic diagram for the questions below.



9. Given that the reference voltage, VDC1, is shown as 5.120 V, what is the step size for the DAC in this circuit. in millivolts per step? _____ mV/step.
10. When DAC_Out is less than Ana_in (the analog input voltage), the output of U2A will be _____ .
11. When the output of U2A is LOW, the LED will _____ .
12. Based upon the above, as the successive approximation algorithm for Analog to Digital Conversion progresses, a glowing LED means that the bit under test should be _____
13. CHALLENGE QUESTION: When the LED is glowing, the voltage expected at the Base of Q1 is _____ V.

Simulation

In Multisim, build the A to D converter you've just analyzed, reproduced below for easy access.



Notes:

- The potentiometer is "Basic --> POTENTIOMETER --> 10 k"; set it initially to 70% as shown
- The DIP switch is "Basic --> SWITCH --> DSWPK_8"

- The 10 kΩ R-pack is "Basic --> RPACK --> 8Line_Bussed"; change its value to 10 kΩ
- VDC1 is "Sources --> V_REF1"; change its value to 5.120 V
- The DAC is "Mixed --> ADC_DAC --> VDAC"
- Pick an LED colour that matches the functionality above -- RED if it means "Don't Keep", GREEN if it means "Keep"

1. Proceed through the successive approximation algorithm to determine the A to D output for a setting of 70% and fill in the following table as you do:

Digital input (record as 8-bit binary values)	Keep/Don't Keep
_____	_____
_____	_____
_____	_____
_____	_____
_____	_____
_____	_____
_____	_____
_____	_____

Final digital representation of the input voltage (as an 8-bit binary value): _____

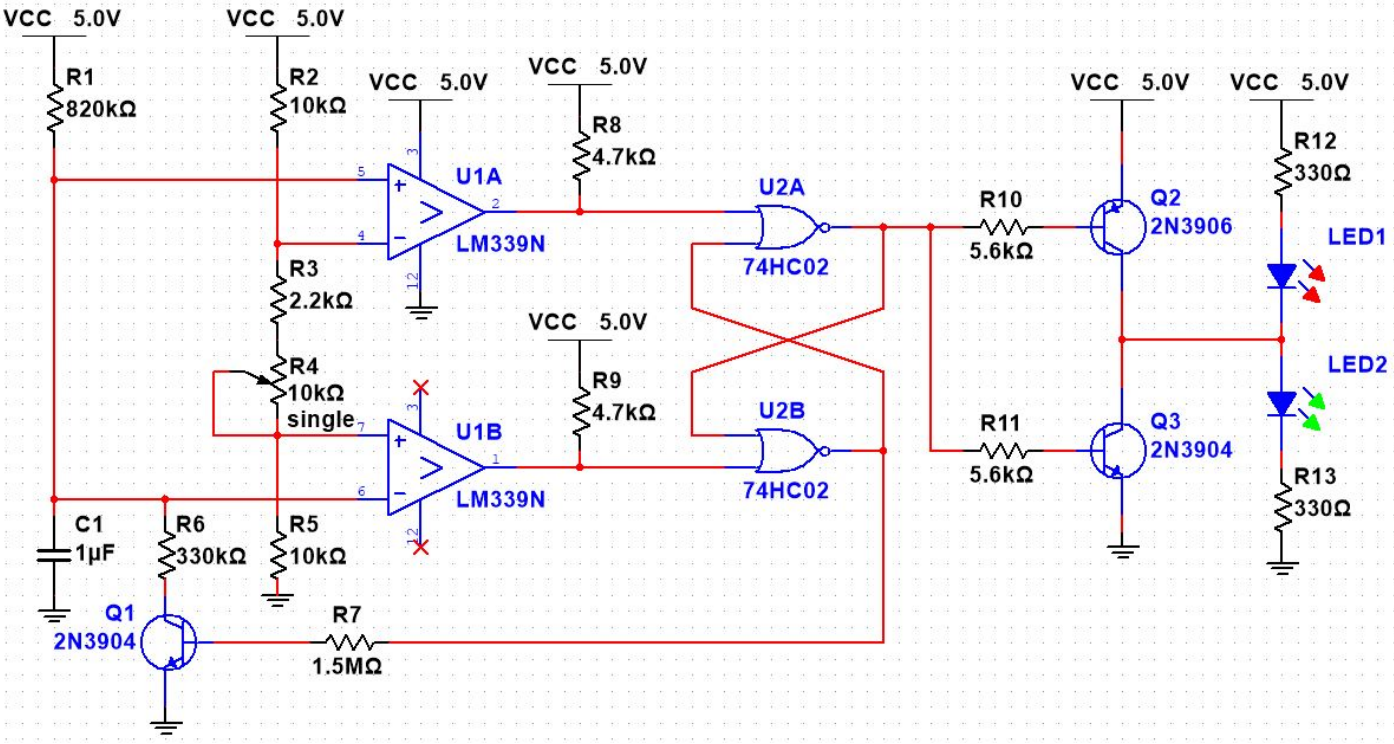
2. Put "Voltage probes" on Ana_In and DAC_Out, and verify for yourself that the successive approximation algorithm has arrived at the correct digital representation. For a grade out of three marks, upload a screen shot of your circuit, with the potentiometer set to 70%, the switches set for the final digital representation, and voltage probes on the two comparator input voltages. If your instructor grades this in class, upload a text file with the grade assigned instead.Document Upload (Direct)

You have now completed the Preparation and Simulation component of this project. Move on to the Circuit Build and Test section. Don't "Submit" yet!

Question 2: (50 points)

Comparator-Based Oscillator

On your breadboard, build the circuit below. Further instructions to follow.



Like most oscillators, this is a difficult circuit to build in stages, since the output feeds back to control the input. We will start with the oscillator section, which includes all components up to and including U2.

- One problem that needs to be addressed is the pin-out for the 74HC02. On a writable surface (paper or digital) add the power pins and their pin numbers for the NOR gate, choose appropriate pins for the gates, and add their pin numbers.
- Also pay special attention to the unusual power pin locations on the LM339 when wiring up the circuit.
- Don't build the Totem Pole and LED section yet.
- To verify that the oscillator is working, put one oscilloscope probe at the top of the capacitor and the other probe at the output of the upper NOR gate in the schematic. You should see a slightly curved "triangle" wave at the capacitor and a square pulse at the upper NOR gate.
- Try adjusting R4. It should speed up the oscillation as you turn it clockwise and slow it down as you turn it counter-clockwise; if you get the reverse action, turn the potentiometer around on your breadboard.

1. With the potentiometer set for the slowest speed of oscillation, measure and record the following:
    1. Maximum voltage on the capacitor: _____ V
    2. Minimum voltage on the capacitor: _____ V
    3. Frequency of the pulse, in hertz: _____ Hz
    4. With a DMM, measure the voltage at Pin 4 of U1: _____ V
    5. With a DMM, measure the voltage at Pin 7 of U1: _____ V
2. With the potentiometer set for the fastest speed of oscillation, measure and record the following:
    1. Maximum voltage on the capacitor: _____ V
    2. Minimum voltage on the capacitor: _____ V
    3. Frequency of the pulse, in hertz: _____ Hz
    4. With a DMM, measure the voltage at Pin 4 of U1: _____ V
    5. With a DMM, measure the voltage at Pin 7 of U1: _____ V

- Hopefully, you've noticed a close correlation between the upper and lower voltages on the capacitor and the voltages on the other pins of the comparators, which should confirm for you that the comparators in this circuit are behaving as predicted.
- Add the Totem Pole; make sure you know which pins are which on the two transistors, and that they are connected correctly!
- With the second channel of the oscilloscope, check the signal at the junction of the two Collectors. You should see a square pulse somewhat like the one at the output of the upper NOR gate.

3. The pulse at the Collectors of the Totem Pole is _____ the signal at the output of the upper NOR gate.

- Add the LED network, and check to see that the LEDs behave as expected.
- Watch to see what relationship exists between the output of the upper NOR gate and the LEDs.

4. When the output of the upper NOR gate is HIGH,

   (a) LED1 is ON and LED2 is OFF

   (b) LED1 is OFF and LED2 is ON

   (c) Both LEDs are ON

   (d) Both LEDs are OFF

5. For a grade out of eight marks (four for the oscillator, two for the Totem Pole, two for the LEDs), upload a picture of your breadboard. If your instructor grades your work in class, upload a text file with the grade assigned instead. Document Upload (Direct)

You have now completed this Project. Once you submit your work, you will not be able to return to any of these questions!

$$I = \frac{Q}{t}$$

$$G = \frac{1}{R}$$

$$V = IR$$

$$P = \frac{W}{t}$$

$$P = IV = \frac{V^2}{R} = I^2 R$$

$$\eta = \frac{P_{useful}}{P_{total}} \times 100\%$$

$$V_{R_1} = V_s \left(\frac{R_1}{R_1 + R_2} \right)$$

$$I_{R_1} = I_T \left(\frac{R_2}{R_1 + R_2} \right)$$

$$a(t) = A_o + A\sin(\omega t + \theta)$$

$$\omega = 2\pi f$$

$$A_{RMS(\sin)} = \frac{|A_p|}{\sqrt{2}}$$

$$C = \frac{\Delta Q}{\Delta V}$$

$$I = C\frac{\Delta V}{\Delta t}$$

$$i_C = C\frac{dV}{dt}$$

$$W = \frac{1}{2}CV^2$$

$$\tau = RC$$

$$V_L = L\frac{\Delta I}{\Delta t}$$

$$v_L = L\frac{dI}{dt}$$

$$W = \frac{1}{2}LI^2$$

$$\tau = \frac{L}{R}$$

$$a(t) = a_{final} - \left(a_{final} - a_{initial}\right)e^{-\frac{t}{\tau}}$$

$$\Delta P_{db} = 10\log\left(\frac{P_2}{P_1}\right)$$

$$\Delta P_{db} = 20\log\left(\frac{V_2}{V_1}\right)$$

$$f_c = \frac{1}{2\pi RC}$$

$$X_C = \frac{-j}{2\pi fC}$$

$$f_c = \frac{1}{2\pi L/R}$$

$$X_L = j2\pi fL$$

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

$$Q = \frac{f_o}{BW} = \frac{|X_L|}{R} = \frac{1}{R}\sqrt{\frac{L}{C}}$$

$$\frac{V_s}{V_p} = \frac{n_s}{n_p}$$

$$\frac{I_s}{I_p} = \frac{n_p}{n_s}$$

$$\frac{R_s}{R_p} = \left(\frac{n_s}{n_p}\right)^2$$

$$e_{\max} = 2n^2$$

$$r'_D = \frac{\Delta V}{\Delta I}$$

$$V_{DC(HWR)} = \frac{V_p}{\pi}$$

$$V_{RMS(HWR)} = \frac{|V_p|}{2}$$

$$V_{DC(FWR)} = \frac{2V_p}{\pi}$$

$$V_{RMS(FWR)} = \frac{|V_p|}{\sqrt{2}}$$

$$V_{r(p-p)} = \frac{I_L T}{C}$$

$$V_{DC(fil)} = V_P - \frac{V_{r(p-p)}}{2}$$

$$V_{r(p-p)} \approx \frac{V_p T}{R_L C}$$

$$1.25 = V_{out}\frac{R_1}{R_1 + R_2}$$

$$RR = 20\log\left(\frac{V_{r(in)}}{V_{r(out)}}\right)$$

$$I_E = I_C + I_B$$

$$\alpha = \frac{I_C}{I_E}$$

$$\beta = \frac{I_C}{I_B}$$

$$\alpha = \frac{\beta}{\beta + 1}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$A_v = \frac{v_{out}}{v_{in}}$$

$$A_{vo} = \frac{v_{oc}}{v_{in}}$$

$$r_{in} = R_S\frac{v_{in}}{(v_s - v_{in})}$$

$$r_{out} = R_L\frac{(v_{oc} - v_o)}{v_o}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GSoff}}\right)^2$$

$$A_v = A_{vo}\left(\frac{R_L}{r_{out} + R_L}\right)$$

For properly designed amplifiers only:

$$V_E = \frac{V_{CC}}{10}$$

$$V_{CE} = \frac{V_{CC}}{2}$$

$$R_{B2} = 10R_E$$

$$R_{E1} \geq \left| \frac{R_C}{2V_{CC}} \right|$$

$$A_{vo} \approx -\frac{R_C}{R_{E1}}$$

$$r_{in} \approx (\beta R_{E1}) \| R_{B1} \| R_{B2}$$

$$r_{out} = R_C$$

$$V_E = \frac{V_{CC}}{2}$$

$$R_{B2} = 10R_E$$

$$A_{vo} \approx +1$$

$$r_{in} \approx R_{B1} \| R_{B2}$$

$$r_{out} \approx \left| \frac{R_E}{20V_{CC}} \right|$$

$$A_{vCS} = \frac{v_{oCS}}{v_{iCS}}$$

$$A_{vDS} = \frac{v_{oDS}}{(v_{i2} - v_{i1})}$$

$$CMRR_{dB} = 20\log\left(\frac{A_{vDS}}{A_{vCS}} \right)$$

$$A_v = -\frac{R_f}{R_i}$$

$$A_v = \frac{R_f}{R_i} + 1$$

$$\beta = \frac{R_i}{R_f + R_i}$$

$$A_v = \frac{A_{vol}}{1 + A_{vol}\beta}$$

$$r_{in} = (1 + A_{vol}\beta) r_{id}$$

$$r_{out} = \frac{r_o}{1 + A_{vol}\beta}$$

$$A_v = 1 - \frac{A_{vol}}{1 + A_{vol}\beta}$$

$$r_{in} = R_i \| [(1 + A_{vol}\beta) r_{id}]$$

$$BW = \frac{GBP}{A_v}$$

$$BW_{circuit} = BW_{stage} \sqrt{2^{\frac{1}{n}} - 1}$$

$$f_{PBW} = \frac{SR}{2\pi V_p}$$

$$V_{out} = -R_f \left(\frac{V_{in1}}{R_{i1}} + \frac{V_{in2}}{R_{i2}} + \frac{V_{in3}}{R_{i3}} + \ldots \right)$$

$$V_{step} = \frac{V_{range}}{2^n - 1}$$

$$V_{step} = \frac{V_{ref}}{2^n}$$

$$V_{out}(t) = \frac{1}{R_i C} \int_0^t v_i(t) dt$$

$$v_{out} = R_f C \frac{dV_{in}}{dt}$$

$$f_c = \frac{1}{2\pi R_f C}$$

$$f_c = \frac{1}{2\pi R_i C}$$

$$A_v = 3 - 2\zeta$$

$$f_c = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

$$f_c = \frac{1}{2\pi RC}$$

$$v_o = \frac{R_f}{R_i} (V_{in+} - V_{in-})$$

$$A_v = \frac{2R}{R_G} + 1$$

$$v_o = A_v (V_{in+} - V_{in-}) + V_{off}$$

n	Normalized Butterworth Polynomial	Stage Gains
1	$s+1$	(x)
2	$s^2 + 1.414s + 1$	(1.586)
3	$(s+1)(s^2 + s + 1)$	(x)(2.000)
4	$(s^2 + 0.765s + 1)(s^2 + 1.848s + 1)$	(2.235)(1.152)
5	$(s+1)(s^2 + 0.618s + 1)(s^2 + 1.618s + 1)$	(x)(2.382)(1.382)
6	$(s^2 + 0.518s + 1)(s^2 + 1.414s + 1)(s^2 + 1.932s + 1)$	(2.482)(1.586)(1.068)

Typical Component Values

Typical Component Values		
5%	10%	20%
10	10	10
11		
12	12	
13		
15	15	15
16		
18	18	
20		
22	22	22
24		
27	27	
30		
33	33	33
36		
39	39	
43		
47	47	47
51		
56	56	
62		
68	68	68
75		
82	82	
91		

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