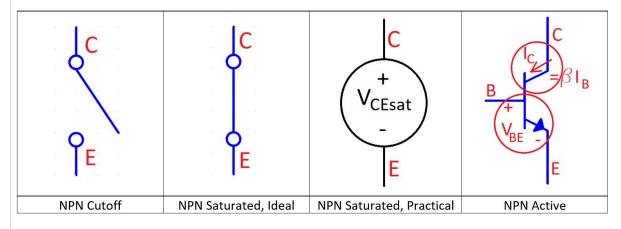
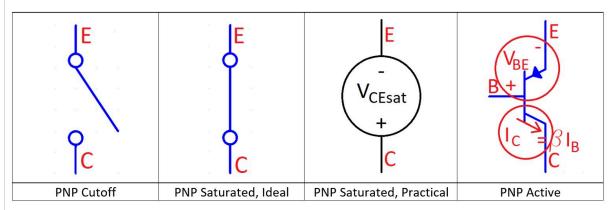
## **BJT Models**

Since transistors are fairly complex devices with lots of characteristics we haven't discussed (temperature dependency, internal capacitance, saturation storage time, differences in DC and AC characteristics, etc.), there are quite a few models around. This author has developed his own models to help with a basic understanding of transistors to help predict reasonably accurately how they will behave in the circuits you are likely to encounter. You won't see these models in any other textbooks.





These models help with the analysis of DC biasing circuits for transistors.

Since there are three distinct modes of operation, there are three distinct models -- Cut-off, Saturation, and Active. There are times when the small voltage drop for a saturated transistor is significant, so we have two saturation models -- Ideal and Practical.

*Cut-off* should be the easiest one to spot and to use. If there is no way of generating Base current, there will be no Collector current, and the transistor will behave as an open in the circuit -- hence the open switch model.

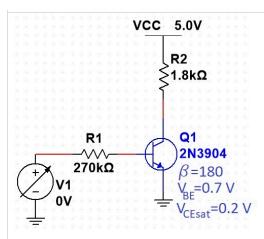
**Saturation** isn't as easy to spot, but it's fairly easy to use. It's analysis is essentially like that of a forward-biased diode, except that  $V_{CEsat}$  is typically much smaller than the diode's barrier potential.

*Active* -- in the Active region, the transistor is treated as an Ideal Current source, in which  $I_C = \beta I_B$ . If we can determine  $I_B$  we can analyze the output. To help us determine  $I_B$ , the model reminds us that there is a forward-biased P-N junction between the Base and the Emitter when the transistor is conducting. The only other thing to remember is the the Collector current and the Base current combine to become the Emitter current.

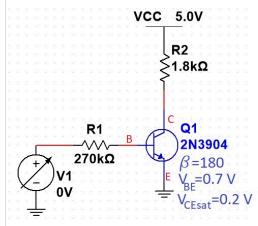
The problem comes in trying to determine if a transistor that's conducting is in the Active mode or in Saturation. The best we can do to distinguish these is to analyze the circuit as if it were in the Active mode, and if the answers don't make sense (i.e. if they go off the Saturation end of the DC Load Line), then the transistor must be saturated; throw away the Active model results and use the Saturation model instead.

Here are a few worked examples and questions to get you used to applying these models.

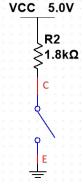
We'll start with an easy one.



Always start by labelling the pins on the transistor -- this will prevent you from confusing the Collector and Emitter if you're in too much of a hurry.



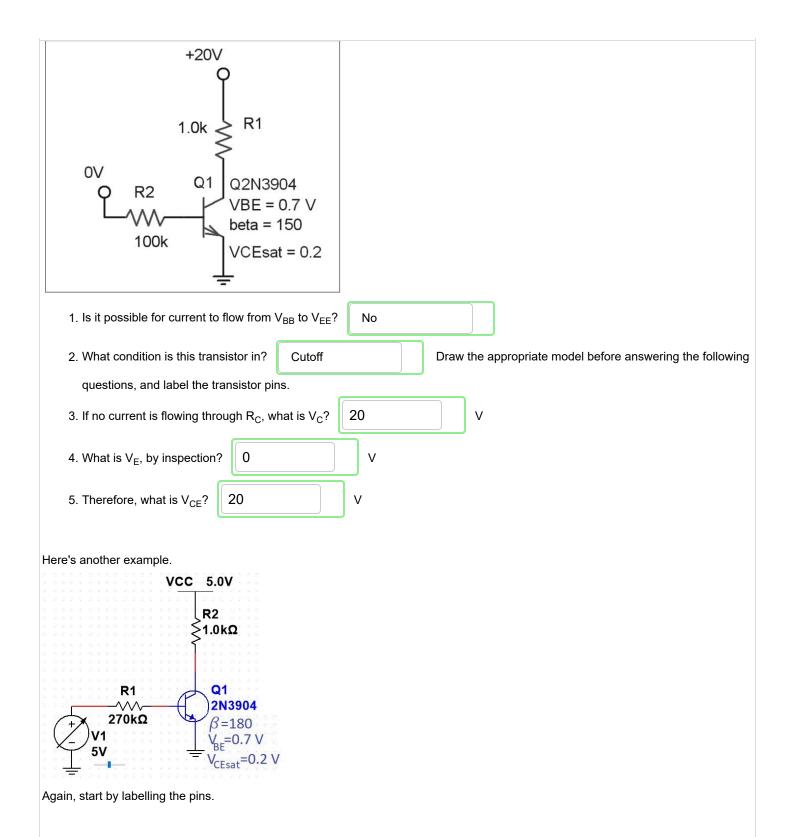
The first thing to notice about this circuit is that  $V_{BB} = 0$  V and the Emitter is grounded. With no potential difference between these two voltages, there is no chance of current flowing through R1. This means that the transistor is in Cutoff. We immediately replace the transistor with the Cutoff Model, and proceed.

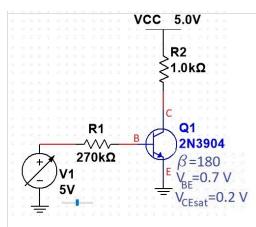


From this, we can answer all the necessary questions about this circuit:

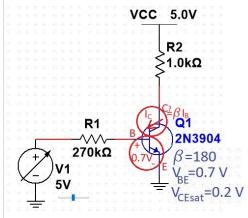
- I<sub>B</sub> = 0 mA (that was the basis for choosing this model)
- I<sub>C</sub> = 0 mA (open switch)
- $I_E = 0 \text{ mA} (I_C + I_B)$
- $V_B = 0 V$  (no drop across  $R_B$  because there's no  $I_B$ )
- V<sub>E</sub> = 0 V (connected directly to ground)
- $V_C = 5 V$  (no drop across  $R_C$  because there's no  $I_C$ )
- V<sub>CE</sub> = 5 V (V<sub>C</sub> V<sub>E</sub>)

Give it a try!





This time,  $V_{BE}$  is higher than  $V_{EE}$ , so current will flow through the forward-biased B-E junction. Since the transistor isn't in cutoff, we start with the Active Model, but keep an eye open for indications that it may not be the correct model. Notice the question mark over the '=' sign -- put it there to remind yourself that this may not be the right model.



The Current Source in the Collector is a good thing -- ideal current sources have infinite internal impedances, so, for all intents and purposes, the circuit involving the Base and Emitter is isolated (effectively disconnected) from anything on the Collector side of the circuit. That means we can just use KVL to determine what the Base current will be:

$$I_B=rac{\varDelta V_{R_B}}{R_B}$$
 = (5 - 0.7)/270 k $arOmega$  = 15.9  $\mu$ A

Now, we can use the transfer function to determine what Collector current is predicted using the Active Model:

$$I_C=eta I_B$$
 = 180\*15.9  $\mu$ A = 2.87 mA

We're still not sure if this is the correct model, but we can check now. The maximum current that could flow in this circuit would exist if the transistor was completely shorted. In this case, the entire  $V_{CC}$  would appear across  $R_C$ :

$$I_{Cmax}=rac{V_{CC}}{R_C}$$
= 5.0/1.0 k $arOmega$  = 5.0 mA

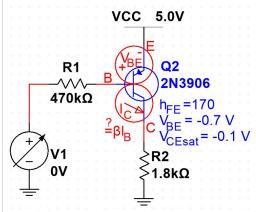
Since the predicted  $I_C$  is less than the maximum  $I_C$ , the model has predicted a reasonable value. Therefore, the Active Model was the right choice. We'll continue on with the analysis. We now have enough information to determine all of the characteristics of this circuit:

- V<sub>E</sub> = 0 V (connected to ground)
- V<sub>B</sub> = 0.7 V (V<sub>E</sub> + V<sub>BE</sub>)
- $V_C = V_{CC} I_C R_C = 2.13 V$  (\*\*watch this one! Make sure you're clear that  $V_C$  is referenced to ground!)
- V<sub>CE</sub> = 2.13 V (V<sub>C</sub> V<sub>E</sub>)
- $I_E = 2.89 \text{ mA} (I_C + I_B)$

Your turn.

$\begin{array}{c} +20V \\ 1.0k \\ +10V \\ 0 \\ R2 \\ 100k \\ 100k \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ $			
6. Is it possible for current to flow from $V_{BB}$ to $V_{EE}$ ? Yes			
7. Following the discussion above, draw the model needed to continue the analysis of this circuit. What would the voltage at the			
Base, V <sub>B</sub> , be?			
8. What current would flow through the Base resistor? 93 $\mu$ A			
9. What does the model you've chosen predict as the Collector current? 13.95 mA			
10. If the transistor was shorted (0 V drop), what is the maximum current that could flow through R1? 20 mA			
11. Has the model you chose predicted a possible result for the Collector current? Yes			
12. Assuming your answer was "Yes", what voltage drop would appear across R <sub>C</sub> ? 13.95 V			
13. What, then, would the Collector voltage be? 6.05 V			
14. What would V <sub>CE</sub> be? 6.05 V			
15. Looking back, what condition is this transistor in?			
Let's try a couple with PNP transistors. VCC 5.0V R1 Q2 2N3906 $h_{FE} = 170$ $V_{BE} = -0.7 V$ $V_{CEsat} = -0.1 V$ R2 1.8k $\Omega$			

Notice that  $V_{BB}$  is considerably less than  $V_{EE}$ , (make sure you know which pin is the Emitter -- label them right away, as in the diagram below) so current can flow through the forward-biased Emitter to Base junction. Therefore, the transistor is not in Cutoff, so we'll start with the Active Model, again checking to see if anything we discover indicates otherwise. In the following diagram, the labels have been added and the Active Model has been drawn over the transistor. Notice that the Emitter is at the top -- that establishes all the relationships we will be investigating. Also notice the use of  $h_{FE}$  -- that's just  $\beta$ .



Notice that the power supply is labelled " $V_{CC}$ ". It should, strictly speaking, be " $V_{EE}$ ", because it's powering the Emitter. However, in a schematic package, it's not possible to use different labels for the same power supply, so, if other components in the circuit are using " $V_{CC}$ ", we have to live with it even for PNP devices.

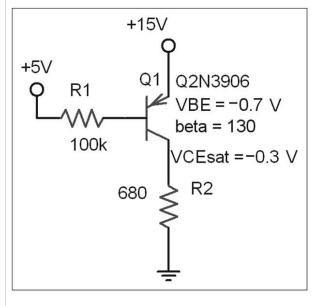
The negative sign on  $V_{BE}$  indicates that the Base voltage is below the Emitter voltage. That also shows up in the orientation of the signs in the  $V_{BE}$  symbol in the model. All it means is the Base voltage is less than " $V_{CC}$ ", or maybe better put, less than " $V_{E}$ ".

- $V_E = 5.0 \text{ V}$  (directly connected to " $V_{CC}$ ")
- V<sub>B</sub> = 4.3 V
- $I_B = V_B/R_B = 9.15 \ \mu A$  ( $R_B$  is connected to ground, so  $V_B$  appears across it)
- I<sub>C</sub> is predicted to be 1.56 mA by the Active Model. It's time to check to see if this is the right model.

If the transistor was completely shorted, we'd be left with 5.0 V across  $R_C$ , so  $I_{Cmax} = 5/1.8 \text{ k}\Omega = 2.78 \text{ mA}$ . So, since the Active Model predicted a current that's less than the maximum current, that's a reasonable result, confirming that the Active Model is the right choice. So we can continue with the results we've gotten so far.

- V<sub>C</sub> = I<sub>C</sub>\*R<sub>C</sub> = 2.80 V (R<sub>C</sub> is connected to ground this time, so V<sub>C</sub> appears across it in this example)
- $I_E = I_C + I_B = 1.56$  mA (rounds to the same value as  $I_C$  because  $\beta$  is so big)
- $V_{CE} = V_C V_E = -2.2 V$  (because the Collector voltage is less than the Emitter voltage)

Your turn again.

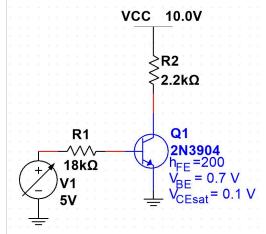


16. Is it possible for current to flow between  $V_{BB}$  and  $V_{EE}?$ 

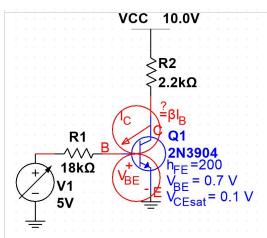
Yes

17. If so, in which direction?	Out of the Base		
18. Replace the transistor with the appropriate model, and determine the magnitude of I <sub>B</sub> . 93 $\mu$ A			
19. What does your chosen model predict for the magnitude of the Collector current? 12.09 mA			
20. Which direction does the Collector current flow? Out of the Coll			
21. If the transistor were shorted out, what is the maximum current that could flow in the circuit? [22.1 mA			
22. Is the Active Model the correct choice? Yes			
23. What is V <sub>E</sub> ? 15	V		
24. What is V <sub>B</sub> ? 14.3	V		
25. What is V <sub>C</sub> ? 8.22	v		
26. What is V <sub>CE</sub> ?	6.7	8 V	
27. What is the magnitude of I <sub>E</sub> ? 12.18 mA			
28. Looking back, what condition is this transistor in? Active			

So far, the examples have been either in Cutoff or in the Active Linear Region of operation. Let's check out the following circuit.



To begin, V<sub>BB</sub> is higher than the Emitter voltage, so current can flow. That means it's not in Cutoff, so we start with the Active Model, again keeping in mind that it might be the wrong model.



We can get some of the basics down right away:

- V<sub>E</sub> = 0 V (connected to ground)
- $V_B = 0.7 V (V_E + V_{BE})$

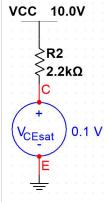
Using KVL, we determine I<sub>B</sub>:

•  $I_B = \Delta V_{RB}/R_B = (5 - 0.7)/18 \text{ k}\Omega = 239 \ \mu\text{A}$ 

Now we move over to the collector side, and check to see if the prediction made by the Active Model makes sense:

- The model says  $I_C = \beta I_B = 47.8 \text{ mA}$
- $I_{Cmax} = 10 \text{ V}/2.2 \text{ k}\Omega = 4.55 \text{ mA}$

The Active Model is clearly wrong, because it predicted a current that's much higher than the maximum current that could flow in this circuit. So, we toss out the Active Model and use the Saturated Model instead. For this course, we'll usually use the Practical Model, but in the future, you'll probably discover that the Ideal Model is usually good enough.

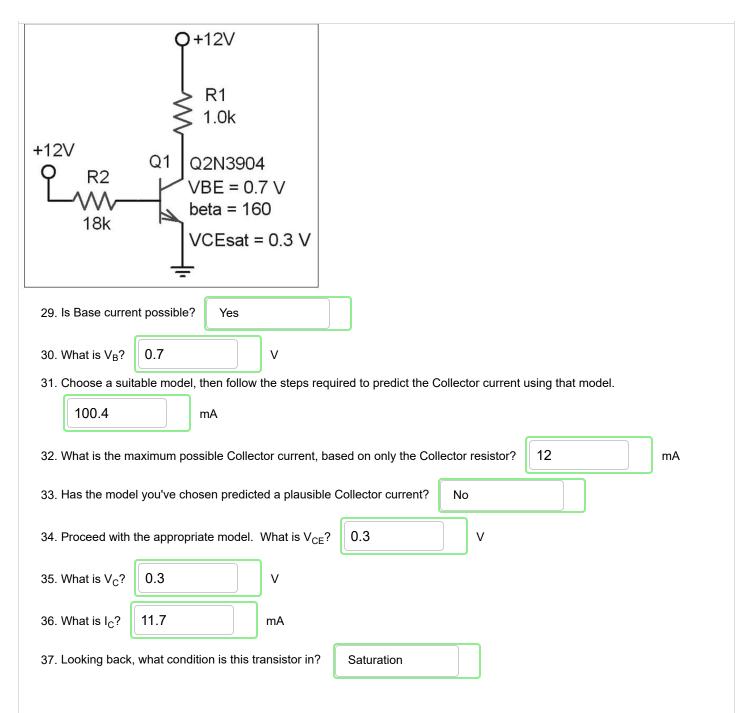


From this, we can determine the rest of the circuit's characteristics:

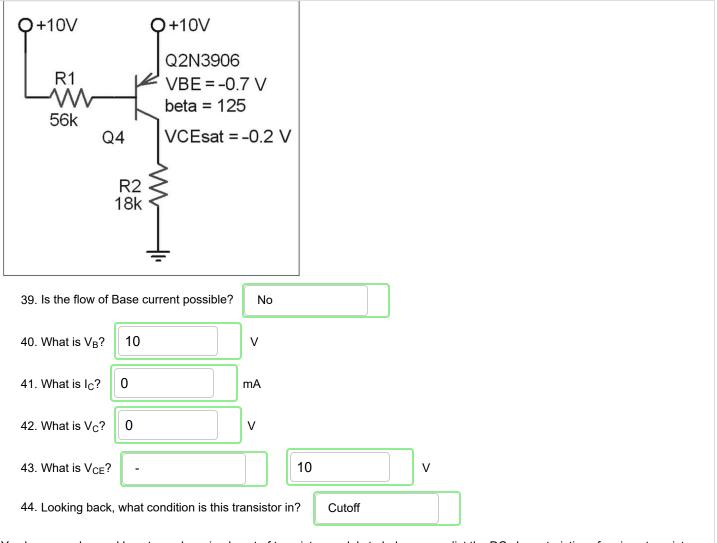
- V<sub>CE</sub> = V<sub>CEsat</sub> = 0.1 V
- $V_{C} = 0.1 V (V_{E} + V_{CE})$
- I<sub>C</sub> (which can also be called I<sub>Csat</sub>) =  $\Delta V_{RC}/R_{C}$  = (V<sub>CC</sub> V<sub>C</sub>)/R<sub>C</sub> = 4.50 mA
- $I_E = 4.74 \text{ mA} (I_C + I_B)$

The Saturation Model predicts a reasonable current, since I<sub>C</sub> is slightly less than I<sub>Cmax</sub>.

Your turn.



By now, you should be getting familiar with using the models, so try this one on your own.



You have now learned how to apply a simple set of transistor models to help you predict the DC characteristics of various transistor circuits. What you have learned here will continue to be useful to you as you learn how to make simple transistor logic switches, transistor current switches, and transistor amplifier biasing circuits.