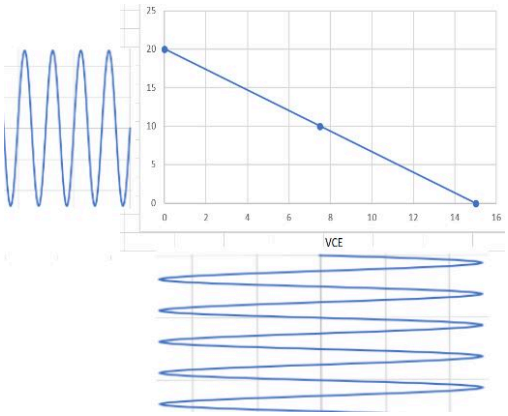
Transistor Amplifier Biasing

In the previous topics, we needed to design our switch circuits to switch from Cut-off to Saturation, completely avoiding the Linear Active Region. However, when it comes to Linear Amplifiers, we need to be in the Active Region, and preferably pretty close to the middle of the Active Region so that we can vary the output in both directions without hitting the non-linearity of either Saturation or Cutoff.



The point in the middle of the Load Line above is called the "Quiescent Point" or "Q-Point". It would be the actual DC conditions for the biased circuit. If it is designed to be in the middle, as shown, then if we superimpose an AC signal on top of the DC Q-Point, as the Collector current drops V_{CE} rises, and as the Collector current rises, V_{CE} drops. In the example shown, the current and voltage both vary sinusoidally, which turns this into a linear amplifier.

If the Q-point was too close to either Saturation or Cutoff, the sinewave would end up being truncated or "chopped off", resulting in a distorted signal.

1. If the Q-point was too close to Saturation, V_{CE} would be distorted at the low voltage end. If the Q-point was too close to Cut-off, V_{CE} would be distorted at the high voltage end.

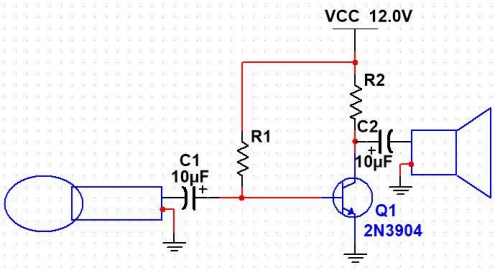
So, it is important to be able to carefully control the Q-point conditions by choosing the correct resistors and, as you will see, picking the best biasing circuit.

Base Bias or Fixed Bias

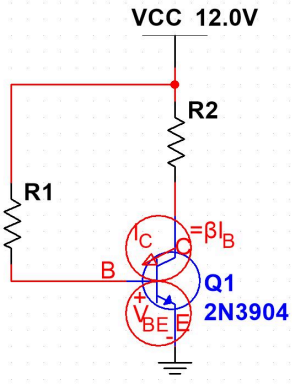
The simplest Biasing arrangement is one we've been using, but as a switch by forcing it into Saturation or Cut-off. Here, we will attempt to put the Q-Point in the middle of the DC Load Line.

Here's a worked example to show you how the analysis goes, then we'll do one to investigate the beta dependency of this biasing arrangement.

In one (fairly poor) system, the following amplifier circuit was used as an interface between a microphone and a powered speaker (i.e. containing its own power amplifier).



The microphone and the speaker are "AC-Coupled" to the amplifier by two capacitors which block the DC levels seen at the Collector and Base of the transistor. This means we can ignore the microphone, speaker, and capacitors when we're doing an analysis of the biasing arrangement. Here's just the DC biasing part of the circuit, with the pins labelled and the Active Model imposed on it.



For this design, R2 was chosen to be 560 Ω to match the input impedance of the powered speaker.

Since we want V_{CE} to be $V_{CC}/2$, and since V_E is ground (0.0 V), that means that V_C should be 6.0 V.

To find I_C, we calculate using the voltage across R_C: $I_C = (V_{CC} - V_C)/R_C$ = 10.7 mA.

Using the Transfer Function, we determine that $I_B = I_C/\beta$. The Data Sheet for the 2N3904 tells us that beta could be anywhere from 100 to 300, so we'll assume β = 200. That means that I_B = 53.6 μA.

Since V_E = 0.0 V, $V_B = V_{BE}$. Our experience in the lab indicates this is probably going to give us V_B = 0.7 V. So, R_B would need to be as close as possible to R_B = (12 - 0.7)/53.6 μA = 211 kΩ. The closest 10% standard value to this is 220 kΩ, so we pick that for R_B. Notice we pick the ***closest***, not half or anything else -- we want the current to be as close as possible to the desired value so that the Q-Point is as close as possible to the middle of the DC Loadline.

Since our chosen resistor isn't the Ideal value, we need to do a Theoretical prediction to see how our actual circuit will behave.

I_B = (12 - 0.7)/220 kΩ = 51.4 μA

$I_C = \beta I_B$ = 200 * 51.4 μA = 10.3 mA

$V_C = V_{CC} - I_C R_C$ = 12 V - 10.3 mA * 560 Ω = 6.25 V

Since V_E = 0.0 V, $V_{CE} = V_C - V_E$ = 6.25 V.

Let's see where that puts us on the DC Loadline.

If the transistor was "open" the current would be zero and the voltage across it would be V_{CEmax} = 12 V.

If the transistor was shorted, the voltage across it would be zero and the current would be at a maximum: I_{Cmax} = 12/560 = 21.4 mA. This gives us the following DC Loadline, with two Q-Points on it: The Ideal (exactly in the middle) and the Theoretical (based upon the actual resistors chosen).

	A	B	C	D	E	F	G	H	I	J
1		VCE	IC							
2	VCEmax	12	0							
3	ICmax	0	21.4							
4	Ideal	6	10.7							
5	Theoretical	6.25	10.3							
6										
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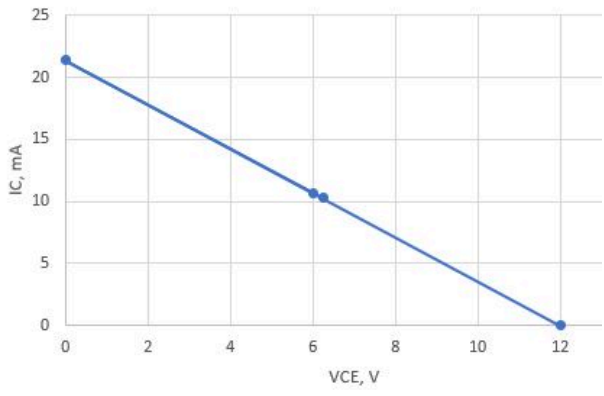
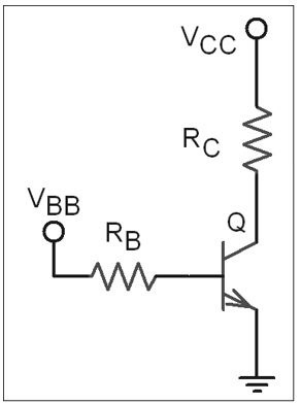


This shows us that our circuit's predicted Q-Point is close to the middle of the DC Loadline, where we want it to be. It's slightly toward the Cutoff end. In reality, it would be better if it were closer to the Saturation end, but we won't go into the reasons for that.

Let's now investigate a similar circuit, and in the process discover the reason why we consider Self Bias or Fixed Bias not to be a good biasing arrangement.



Assume that V_{BB} and V_{CC} are the same supply, +10 V_{DC}, that V_{BEon} is 0.7 V, and that β ranges from 100 to 300.

2. To put the Q-Point in the middle of the DC Load Line, V_{CE} should be [5] V_{DC}
3. If the Q-Point current is to be 10 mA, what should R_C be, ideally? [500] Ω
4. Pick the ***closest*** 5% resistor value. [510] Ω
5. Use the average value for β, 200, to determine the Base current required. [50] μA
6. Determine the ideal value for R_B [186] kΩ, the pick the ***closest*** 5% resistor value [180] kΩ

Since the resistors chosen aren't exactly what we wanted, we need to determine the actual theoretical circuit characteristics for our circuit.

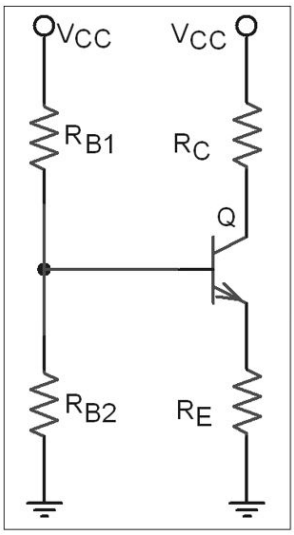
7. What is the theoretical value of the Collector current? [10.3] mA
8. What is the theoretical value of V_{CE}? [4.73] V (Remember to subtract the voltage across the resistor from the supply to get the voltage across the transistor.)

The problem with this circuit is that it is highly β***-Dependent***, which means that variations in transistor characteristics affect it significantly.

9. Using the same circuit components but using the worst transistor available -- β = 100 -- recalculate the Collector current [5.17] mA and V_{CE} [7.36] V
10. Using the same circuit components but using the best transistor available -- β = 300 -- recalculate the Collector current [15.5] mA and V_{CE} [2.09] V
11. On a piece of paper, draw the DC Load Line: V_{CEmax} = [10] V and I_{Cmax} = [19.6] mA. Plot the three Q-points for the three transistors on your DC Load Line.
12. This transistor circuit is highly dependent on the β of the transistor. (●) True ( ) False

BJT Voltage Divider Bias

To deal with the problem of β-Dependency, a circuit with ***negative feedback*** has been designed. This is a surprisingly difficult circuit to design and analyze completely accurately, so in this course we will provide some limits to the design characteristics which will give us a good approximation of the actual performance of the circuit. Here's the circuit:

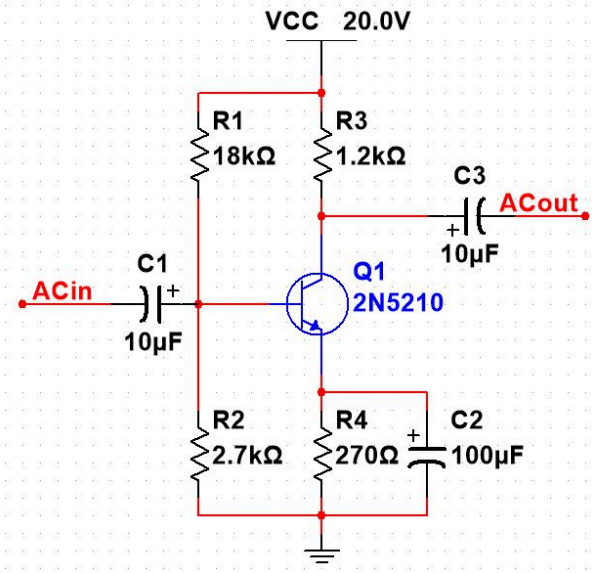


Here are the guidlines for a suitable design, and the results expected.

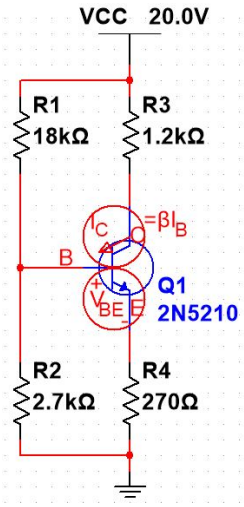
- Pick a transistor with a β greater than 100.
- Choose a value for R_E that will make V_E approximately 1/10th of V_{CC}.
- Make $V_{CE}=V_{CC}/2$.
- Choose a value for $R_{B2} = 10R_E$.
- Calculate a value for R_{B1} that will set V_B to $V_E + V_{BE}$.

The results should be within 10% of the actually-measured (empirical) values.

We'll start with a quick worked example in which we will analyze an existing circuit, then we'll move into a design-oriented question. The following schematic is a workable amplifier, again with DC-blocking capacitors C1 and C3 to isolate the AC signals at the input and output from the DC biasing voltages at the Base and Collector. C2 actually provides an AC short to ground which removes the negative feedback but only for the AC signal, allowing this "Common Emitter" amplifier to have a fairly large signal gain. But you don't need to know any of that, because we don't do transistor amplifiers in the course. All you need to know is the DC biasing part, which exists inside the big capacitors.



Here's just the DC-biasing part of the circuit, again labelled and with the Active Model superimposed over it. We'll discover that the only part of the Active Model we need in our simplified analysis is V_{BE}.



Let's check to see that the circuit meets the requirements specified above:

- The Data Sheet (https://media.digikey.com/pdf/Data%20Sheets/ON%20Semiconductor%20PDFs/2N5210,MMBT5210.pdf) for the 2N5210 says that beta ranges from 250 to 900 -- that's much greater than 100
- R_{B2} is ten times the size of R_E

We'll have to do some calculations to check the other conditions.

Assuming that the current through R_{B2} is much greater than the Base current, we can treat R_{B1} and R_{B2} as a simple voltage divider: $V_B = 20(2.7k)/(18k + 2.7k) = 2.61$ V. Now we can determine V_E and see if it's close to ideal:

- $V_E = V_B - V_{BE} = 2.61 - 0.7 = 1.91$ V, which is pretty close to one tenth of V_{CC}.

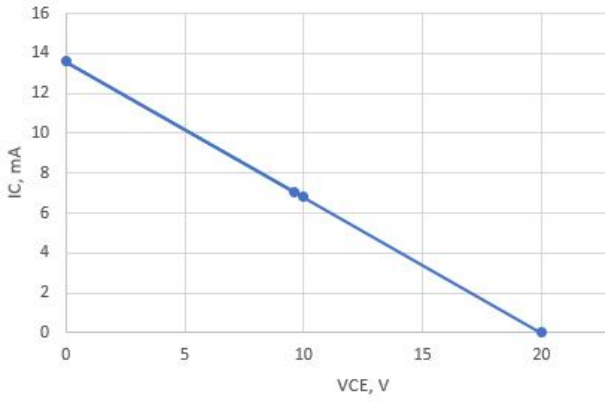
Again, we'll need to do some calculations to determine V_{CE}. $I_E = V_E/R_E = 1.91/270 = 7.07$ mA. Since we assume there's no appreciable Base current, we can say that $I_C = 7.07$ mA. That means that $V_C = V_{CC} - I_C R_C = 20 - 7.07$ mA*1.2 kΩ = 11.5 V. So...

- $V_{CE} = V_C - V_E = 11.5 - 1.91 = 9.6$ V, which is about one half of V_{CC}.

Now for the DC Loadline analysis.

When the transistor is "open", the voltage across it will be 20 V. When it is shorted, the current will be $I_{Cmax} = 20/(1.2\ k\Omega + 270\ \Omega) = 13.6$ mA.

	VCE	IC
VCEmax	20	0
ICmax	0	13.6
Ideal	10	6.8
Theoretical	9.6	7.07



Now for a design-oriented question.

For the circuit given, let V_{CC} = +15 V_{DC}, and the transistor characterics be those of the 2N3904 we've been working with. Again, work towards having a quiescent Collector current of 10 mA.

13. Determine an ideal value for R_E. 150 Ω

14. Assuming the Collector and Emitter currents are basically the same, determine an ideal value for R_C.

600 Ω

15. Determine an ideal value for R_{B2}. 1.5 kΩ

16. Determine an ideal value for R_{B1}. 8.73 kΩ

17. Now pick the closest 5% resistor values for each of these: R_E = 150 Ω, R_C = 620 Ω, R_{B2} = 1.5 kΩ, and R_{B1} = 9.1 kΩ.

Again, since the chosen resistors are not exactly the ideal values, we need to analyze the theoretical conditions of our actual circuit.

18. V_B = 2.12 V

19. V_E = 1.42 V

20. I_E = 9.48 mA

21. Assuming I_C and I_E are the same, what is V_{CE}? 7.7 V

22. Check back: did you use β in any of your calculations? No

This circuit is not β-Dependent, so picking different transistors will have very little effect on the circuit biasing characteristics.